Design of a Programmable Gain Amplifier (PGA) for Bluetooth Low Energy (BLE) in 0.13 μm CMOS

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***Abstract*— Programmable Gain Amplifiers (PGA's) are circuits capable of conveniently changing their gain to address various levels of amplification. Knowing this, the topology proposed in this work takes a source degenerated first stage, a common-source with resistive load second stage, and a gm boosting circuit interface to realize a PGA that has low power consumption and low area. The design developed was able to achieve a maximum power dissipation of 103.1 μW, a minimum bandwidth of 5.59 MHz, a maximum noise of 32.01 nV/$\sqrt{Hz}$, and a gain range of 2.31 - 19.84 dB. Each differential output of the circuit is loaded with either 700 fF or 2 pF, which is the estimated load for the hypothetical following block, the Analog-to-Digital Converter (ADC). Furthermore, the supply voltage of the circuit is 1 V and the design was undertaken on Global Foundrie's 130 nm technology. The phase margin of the core circuit is no greater than 100.3° and no less than 49°. The circuit which design is described in this work is intended to be within the receiver (RX) sub-domain of a Bluetooth Low-Energy (BLE) system, which finds applications on the IoT and healthcare industries, for instance.**

***Index Terms*— Amplifier; CMFB; Low power; PGA; Receiver.**

I. Introduction

Bluetooth Low Energy (BLE or Bluetooth Smart) is well-defined on the Bluetooth 5 Core Specification. BLE is a standard that has as main goals the design of a radio standard with ultra low power consumption, low bandwidth, low cost and that can be simple enough, system-wise. Furthermore, this special kind of Bluetooth uses the 2.4 GHz Industrial Scientific Medical (ISM) band, which ranges from 2400 MHz to 2483.5 MHz [1], [2].

This standard specifies that the Physical Layer (PHY) must have 40 channels, which must have a space of 2 MHz between each other. Furthermore, the modulation that must be used is the Gaussian Frequency Shift Keying (GFSK) one and the range that the device with BLE must reach is up to 150 m, although for most applications the effective range required is less than 10 m. The main applications of BLE rely on IoT, healthcare, mobile devices, chipsets and others [2].

In this work, the objective is to design a fully-differential Programmable Gain Amplifier (PGA), which is part of a BLE's typical receiver, which sub-block is depicted in Fig. 1. The receiver is the sub-block responsible for the conversion of the input RF signal (low power) to a baseband signal that will be taken as input of an Analog-to-Digital Converter (ADC). The structure of this sub-block consists of a low-IF architecture, which comprises the following building blocks:

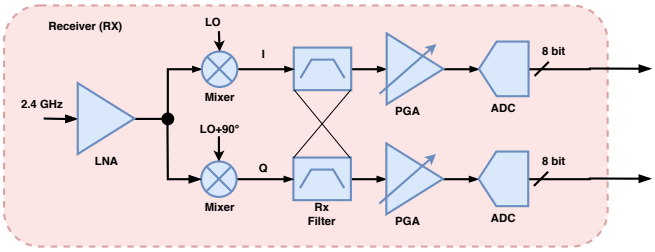

Fig. 1 Low-IF Receiver for a BLE System.

Low Noise Amplifier (LNA), down-converter mixer (quadrature modulation), polyphase filter (complex filter), PGA, and ADC.

The PGA is a kind of fully-differential amplifier largely used in receivers, for instance, as part of the conditioning domain of an Analog Mixed-Signal (AMS) or analog system. It has the faculty of having its gain changed digitally. Such digital control of the PGA is realized by means of a digital input bus [3]. As stated earlier, the modulation defined by the BLE standard is the GFSK one, which suggests, respective to Intermediate Frequency (IF), either a zero-IF or low-IF architecture. Given that the spectrum of this kind of modulation has reasonable energy at zero-IF, being potentially influenced by DC offset and flicker noise in a significant amount, it is more reasonable to use the low-IF architecture for the receiver. This way, in the low-IF range, the intermediate frequency of 2 MHz is chosen for it positions the desired signal in a safe margin beyond flicker noise corner. A lower IF than this would make more difficult to eliminate DC offset, while a higher IF would be more power hungry [4]. Finally, the amplifier must be tuned, by means of a digital word, to the correct gain, depending on the signal level. Regarding the bandwidth of the amplifier, the solution presented in this paper has a variable one, depending on the gain level, but no less than 5 MHz. The organization of this work accounts for design considerations, described in section II, implementation, which corresponds to section III, results and discussion, described in section IV, and conclusion, described in section V.

II. Design Considerations

A. PGA

As briefly discussed on Section I, the PGA is a kind of differential amplifier that has the capability of changing gain by means of a digital word. The importance of this type of circuit in a receiver is linked to the voltage levels that must be

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provided to the ADC. This way, the PGA circuit is responsible for amplifying the voltage levels it gets in its inputs in order to feed the ADC with detectable signals. There are plenty of topologies of PGA, each one tailored to a set of applications.

In [5] a three stage PGA topology is presented, in which the buffer stage has the role of AC coupling, preventing the amplification of offset voltage. The circuit of the first stage is a differential amplifier with source degeneration and resistive load; second stage (buffer) is a Miller single-ended amplifier (with nulling resistor) and the third stage is a differential amplifier (Miller) with nulling resistor fed back by a Common-Mode Feedback Amplifier (CMFB), which is an Operational Transconductance Amplifier (OTA). The target application of this topology is ZigBee protocol, which has operation frequency of 2.4 GHz, such as BLE, and this topology is also designed for a low-IF receiver.

In [6] a topology with offset cancellation capability and enhanced Miller compensation is presented. This design is targeted to IEEE 802.11 b/g zero-IF (direct conversion) receivers, which also supports 2.4 GHz RF frequency at RX front-end.

In [7] a modular PGA topology is presented. Each module corresponds to an OTA with two particularities: two pMOS load pairs, in which one of them is biased at V_{DD} and the other uses substrate biasing. It is called modular because the OTA modules can be cascaded in order to increase gain. This series connection of modules is realized by analog switches.

In [8] the authors propose a three stage topology: the first stage is a differential amplifier with source degeneration, the third stage is a common-source amplifier with resistive load and the intermediate stage works as a feedback interface that increases transconductance and, consequently, the gain of the amplifier. Furthermore, this topology has two pairs of pMOS loads, in which one of them operates as a constant current source and the other one operates as a variable current source. The bias voltage of these pMOS pairs is the output of the CMFB (OTA) designed along with this circuit.

In [9] a ultra low-voltage (ULV) and ultra low-power (ULP) topology is designed. It makes use of a simple OTA and a negative transconductor in order to realize the PGA, which is targeted to RF receivers.

Finally, in [10] a new class discrete receiver is realized. It is based in a discrete-time superheterodyne architecture and designed aiming a decrease in circuits' supply voltage proportional to technology node decrease. This architecture is realized by using transconductors based on inverters and switched capacitors. Such architecture is targeted at IoT applications.

In the present work, a topology based on the Variable Gain Amplifier (VGA) presented on [8] is designed due to its performance on gain, bandwidth (BW) variation and 2 MHz intermediate frequency support.

B. Basic Theory

The topology adopted in order to design the PGA described in this work was a combination of common-source with source degeneration first stage, a common-source with resistive load second stage, and a gm boosting circuit. At the cost of gain, the first stage of the amplifier is chosen to be in a degenerated configuration in order to enhance linearity [11]. To compensate for the loss in gain of the first stage, the boosting circuit is introduced in between first and second common-source gain stages. Furthermore, the chosen topology configures the so called pseudo fully-differential amplifier, which means that there is no tail current being supplied to it, as depicted on Fig. 2. Instead, the bias currents of the first stage are supplied by two symmetric pMOS current sources (T2/T11) connected to the transistors related to the input differential pair (T0/T1). Such bias currents are variable and depend on signal V_{fb} that comes from the CMFB, as depicted on Fig. 3. The PGA circuit is a combination of the topologies reported in [12] and [13], taking advantage of bandwidth's reasonable constancy in the former and good gain range in the latter.

For the selection of gains of the circuit, there are two different parts of the circuit to operate in order to change the value of gain. The first part is linked to the degeneration resistor value, which effective resistance can be changed by turning the switch T3 ON or OFF leading to R_S or $R_S/2$, respectively. The second part corresponds to the symmetrical resistors' matrix associated with switches T4, T5, T10, T21, T22, T24, T25 and T26, which by means of states' combination of these switches produces several pairs of gain and bandwidth, as shown in section IV. The states of these switches are controlled by the Digital Signal Processor (DSP) of the BLE system, not shown here.

The output common-mode of a fully-differential amplifier is variable due to device intrinsic values and mismatches [14]. Thus, a CMFB needs to be designed to correct such problem and for this case a simple OTA that takes a bias current of 10 μA (SIGNAL_AMS_IBIAS_SRC_10U) was developed to address this issue. Along with the CMFB, fixed resistances R4 and R5 are connected to the second stage of the main amplifier, defining the expected common-mode level

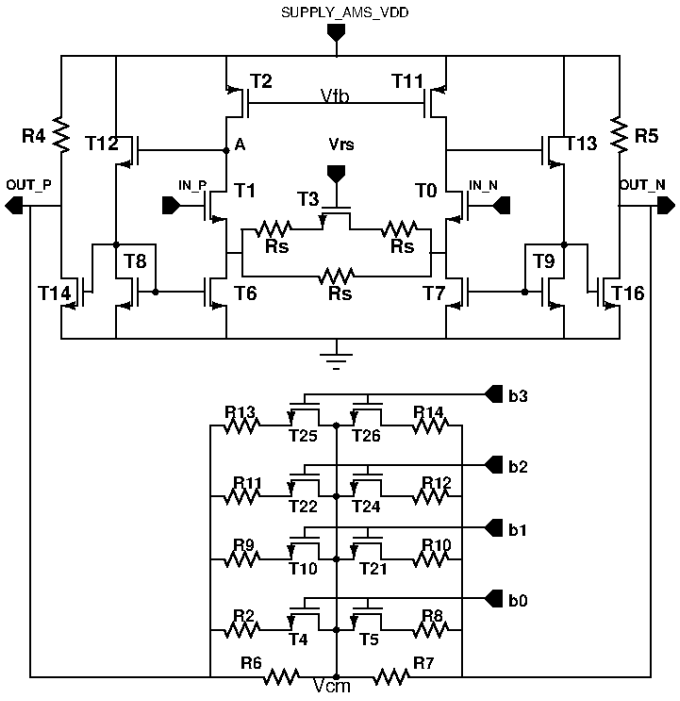

Fig. 2 PGA Topology.

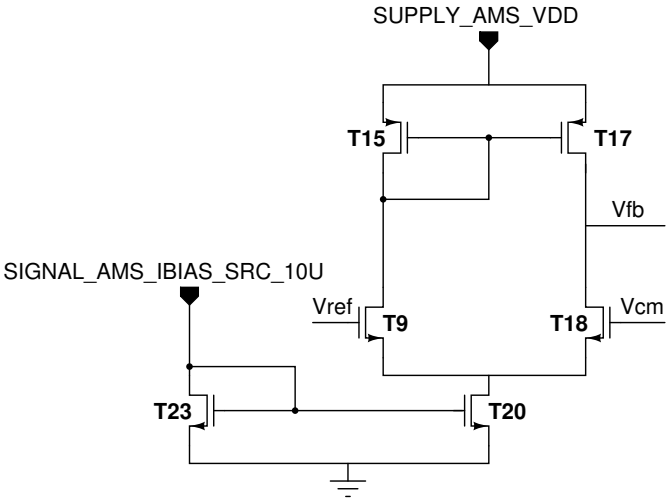

Fig. 3 CMFB Topology.

at the output. Furthermore, this OTA stage is the same first stage used in the classical implementation of the Miller amplifier with nMOS input differential pair. It takes two inputs, V_{cm} and V_{ref} , in which V_{cm} is a signal taken from the interface of the switchable resistances of the PGA (R2/R8, R6/R7, R9/R10, R11/R12, and R13/R14) and which should be stabilized to a value of 500 mV (SUPPLY_AMS_VDD/2) and V_{ref} is the signal that should be compared against V_{cm}. At the output of the transconductance amplifier, a signal V_{fb} must be feedback to the pLoad current sources of the PGA itself (T2/T11), as already stated.

However, for generating V_{ref} for the non-inverting input of the CMFB, it will be needed a circuit that just does that. Such a circuit is illustrated on Fig. 4. Notice that the circuit for generating the voltage reference is composed of two pMOS active load transistors (T31/T34), one nMOS current sink (T32) and the nMOS device that is connected to the right side of the pMOS current mirror, from where the V_{ref} voltage is taken (which corresponds to the V_{DS} voltage of T33).

Finally, the gm boosting circuit serves the purposes of enhancing the gain and the performance of the PGA. Such circuit is represented by transistors T8, T9, T12, and T13 (Fig. 2). Notice that this circuit constitutes a loop along with the first stage amplifier and by means of strenuous calculations it is possible to derive the expression for the effective gm of

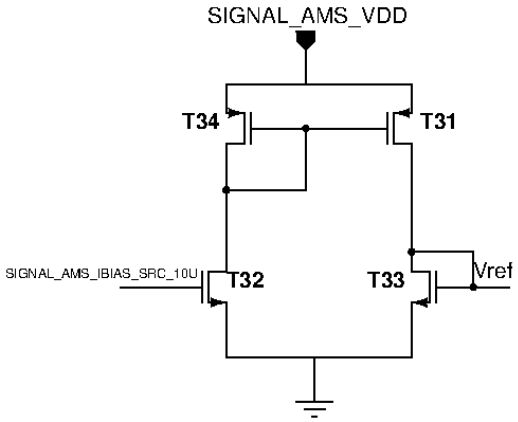

Fig. 4 V_{ref} Topology.

the circuit, which is denoted by

$$g_{meff} = g_{m1}(1 + g_{m6}R_{oA}), \tag{1}$$

in which R_{oA} stands for the output impedance on node A (refer to circuit on Fig. 2) [12], [15].

For the case of the common-source stage with source degeneration, the higher the effective transconductance, the less the gain of the amplifier will depend on the transconductance of the input transistors, placed on the first stage of the circuit. Thus, the gain of the circuit on Fig. 2 is denoted by the expression in [8]

$$A_v = N \times \frac{R_L // R_{Ld}}{R_S/2}, \tag{2}$$

in which R_L is represented by the resistors R4/R5, R_{Ld} is assigned for the resistors of the matrix (R2/R8, R6/R7, R9/R10, R11/R12, and R13/R14), and N is the aspect ratio between transistors T14/T16 and T6/T7. It is highlighted that, for small-signal analysis, resistors R4/R5 are in parallel with the ON resistors of the matrix, contributing to the gain obtained.

C. *Specifications*

In order to design the PGA described in this work and its auxiliary circuits, several steps were taken. First one of those was to derive the specifications of the block, based on the application technology standard (BLE) [16]. As already explained in detail on Section I, as the PGA is a baseband block in a low-IF receiver architecture, the central frequency chosen for the intermediate frequency is 2 MHz with a bandwidth of 1 MHz, conforming the request for BLE. The gain of the circuit must be able to magnify the signal that comes from the complex filter, but must not be too high, at the price of saturating the signal level that is delivered to the ADC. This way, the gain range chosen for the pseudo fully-differential amplifier designed is 2.5 - 20 dB [17]. When it comes to noise, the Bit Error Rate (BER) must be translated to noise requirement. For the Bluetooth 5.0 standard, BER required is 10^{-3}, value that translated to minimum output Signal-to-Noise Ratio ($SNR_{out,min}$) is equivalent to 12 dB [18]. Also, for the calculations of the Noise Figure (NF) of the receiver of the Bluetooth, it is needed to be taken into consideration the sensitivity required by the standard ($S_{in|dBm}$ = -70 dBm for BLE, which it was added a safe margin of -10 dBm, summing up -80 dBm of sensitivity), and the in-band noise source ($N_{s|dBm}$ = -114 dBm). Thus, the NF of the receiver can be derived as in [19]

$$\begin{aligned} NF &= S_{in|dBm} - N_{s|dBm} - SNR_{out,min}, \\ NF &= -80\,dBm - (-114\,dBm) - 12\,dB = 22\,dB. \end{aligned} \tag{3}$$

If it is wished to compute the noise at the output of the IF system, in the shape of noise density, the conversion from NF to noise density can be done as in [20]

$$NF = 1 + \frac{\overline{V_{n,out}^2}}{A_O}\frac{1}{4kTR_S}, \tag{4}$$

in which A_O is the chain of gains from the LNA to the PGA (Fig. 1), k is the Boltzmann constant, T is the room temperature (in kelvin) and R_S is input resistance (50 Ω).

Recent works show that the gain of LNA is generally around 15 dB [21], [22], [23]. Thus, considering that for the receiver depicted on Fig. 1, down converter mixer and filter have zero or negligible gains, then A_{OdB} = 35 dB. Finally, knowing that $\overline{V_{n,out}^2}$ is the noise density at the output of the IF domain of the receiver, then the input referred noise (IRN) can be obtained as in [14]

$$\overline{V_{n,in}} = \frac{\overline{V_{n,out}}}{A_V}, \tag{5}$$

in which A_V is the gain of the PGA. Thus, $\overline{V_{n,in}}$ = 196.4 nV/$\sqrt{Hz}$. A summary of the requirements for the PGA can be seen on Table I.

Finally, the load at the output of the amplifier is assumed to be 700 fF - 2 pF, which refers to the hypothetical input capacitance loading of the ADC. As for power dissipation, recent works show that the range of this requirement in a receiver of a BLE device is up to 1 mW [10].

III. Implementation

The pseudo fully-differential amplifier needs the CMFB for common-mode output stabilization (which is done by means of feedback) and the latter needs a reference voltage circuit. This way, the first thing that was realized on this design was the CMFB, which uses an OTA topology. Its gain, phase margin, bandwidth, power, and gain-bandwidth product (GBW) are shown on Table II.

In order for the CMFB correctly stabilizes the common-mode output of the fully-differential amplifier in case of any surge on the common-mode DC level, its GBW must be higher than the GBW of the differential mode of the fully-differential amplifier, i.e. $GBW_{CMOL} > GBW_{DM}$. This seems intuitive, once that for having time to settle the biasing level, V_{fb}, without driving the devices of the circuit out of saturation, the CMFB must be faster than the fully-differential amplifier itself [24]. For the circuits designed, GBW_{CM} = 209.73 MHz and the highest gain-bandwidth product for differential mode is GBW_{DM} = 67.78 MHz. In order to obtain the aforementioned results, the aspect ratios of the transistors of the CMFB were designed as in Table III.

Notice that the phase margin and bandwidth of the amplifier are already taking into account the loading due to the PGA at CMFB's output.

Going further on the design of the subcircuits of the PGA, the next one that was designed was the circuit for reference voltage, which is responsible for supplying a reference voltage (Vref) of 500 mV to one of the inputs of the CMFB. Such circuit is shown on Fig. 4 and the aspect ratios that lead to the supplying of the correct reference voltage are portrayed on Table IV.

Finally, it is possible to proceed to the design of the core of the PGA itself, which is the pseudo fully- differential amplifier. As already hightlighted in this document, the PGA core is a common-source with source degeneration as first stage, a gm boosting circuit, and a common-source amplifier with resistor load second stage, as depicted in Fig. 2. In order for the fully-differential amplifier to be programmable, a matrix of resistors was arranged in a symmetrical fashion and connected to simple nMOS switches so they can be associated in parallel (small-signal analysis) with the resistor loads of second stage of the common-source amplifier. In order to achieve the desired specifications, the aspect ratios on Table V were used.

The designs for the CMFB, reference voltage circuit, first and gm enhancement stages of the main amplifier were done by considering that all transistors should be in saturation region. Then, the tendencies of the aspect ratios were estimated by using 6 and some of its derived relations, which gives the behaviour of current when the transistor is operating in saturation as seen in [14]

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{th})^2. \tag{6}$$

Specifically, for transistors T0/T1 it was used Eq. 7, in which GBW_{DM} was first specified to be 200 MHz (GBW_{DM} = $A_{dB}\times$ BW = 20 dB $\times$ 10 MHz) and C_L was specified to be 700 fF. Notice that the BW is initially arbitrated in 10 MHz so that the operation frequency (2 MHz) has a tolerance of five times. As seen in [17],

Table I. Specifications for the design of the PGA .

Specification	Definition	Expected value
IRN	Input Referred Noise (PGA)	$\leq$ 196 nV/$\sqrt{Hz}$
$A_v@f_c$	Voltage gain at the central frequency	2.5 - 20 dB
C_L	Load capacitance	700 fF - 2 pF
I_{bias}	Bias current	10 μA
V_{DD}	Power supply voltage	1V
Power	Power consumption of device (receiver)	$\leq$ 1 mW

Table II. Met Specifications of CMFB.

Specification	Definition	Value
A_{VOL}	DC Gain	25.45 dB
A_{VCL}	Closed-loop Gain	36.70 dB
PM_{OL}	Phase Margin (Open-loop)	71.82°
PM_{CL}	Phase Margin (Closed-loop)	17.85°
BW	Bandwidth	13.75 MHz
GBW_{OL}	Gain-bandwidth Poduct (Open-loop)	209.60 MHz
GBW_{CL}	Gain-bandwidth Poduct (Closed-loop)	32.09 MHz
P_{av}	Power Consumption	18.4 μW

Table III. Aspect Ratios of CMFB.

Devices	Definition	Aspect Ratio (W/L) μm
$(W/L)_{20,23}$	Tail current, Bias	1.3/0.19
$(W/L)_{18,19}$	Diff. Input Pair	2/0.4
$(W/L)_{15,17}$	Active Load pMOS	9/0.4

Table IV. Aspect Ratios of Reference Voltage Circuit.

Devices	Definition	Aspect Ratio (W/L) μm
$(W/L)_{34}$	pMOS Current Source	9/2
$(W/L)_{31}$	pMOS Diode Connected Load	4.5/2
$(W/L)_{32}$	nMOS Sink	1.2/0.4
$(W/L)_{33}$	nMOS Reference Voltage Transistor	1.9/2

Table V. Aspect Ratios of PGA.

Devices	Definition	(W/L) μm
$(W/L)_{0,1}$	Diff. Input Pair	2.72/0.4
$(W/L)_{2,11}$	pMOS Mirror	3/0.4
$(W/L)_{6,7}$	nMOS sinks	2/0.4
$(W/L)_{8,9}$	gm-boosting nMOS	2/0.4
$(W/L)_{12,13}$	-	4/0.9
$(W/L)_{14,16}$	nMOS Amplifier	2/0.4
$(W/L)_{3,4,5,10,21,22,24,25,26}$	nMOS Switches	0.68/0.4
R_S	Degeneration Resistors	0.74/3.29 = 6.56 kΩ
$R_{4,5}$	Resistor Loads of CS Second Stage	0.74/18.78 = 45.92 kΩ
$R_{6,7}$	Matrix's Resistor	0.74/54.92 = 137.76 kΩ
$R_{2,8}$	Matrix's Resistor	0.74/23.94 = 59.04 kΩ
$R_{9,10}$	Matrix's Resistor	0.74/11.03 = 26.24 kΩ
$R_{11,12}$	Matrix's Resistor	0.74/8.45 = 19.68 kΩ
$R_{13,14}$	Matrix's Resistor	0.74/2 = 3.28 kΩ

$$gm_{01} = 2\pi \times GBW_{DM} \times C_L, \quad (W/L)_{01} = \frac{gm_{01}^2}{2 \times K_n \times I_D}, \tag{7}$$

in which $K_n = \mu C_{OX}$ and $I_D = SR \times C_L$, being SR the slew-rate and first calculated to be 11.5 V/μs, denoted by

$$SR = 2\pi \times f \times V_{peak}, \tag{8}$$

in which f is signal's highest frequency and V_{peak} is the maximum peak voltage of the signal [26].

In this design, the signal frequency is the intermediate frequency (2 MHz) and V_{peak} is limited by the saturation voltage, V_{DSAT}, of the first stage, which can be obtained according to:

$$V_{DSAT} = SUPPLY\_AMS\_VDD - V_{fb} - |V_{THp}| = \frac{V_{diff}}{2} - V_{THn} \tag{9}$$

and

$$V_{diff} = 2 \times (SUPPLY\_AMS\_VDD - V_{fb} - |V_{THp}| + V_{THn}), \tag{10}$$

in which V_{diff} is the input peak voltage ($V_{peak} = V_{diff}$) and equivalent to 918.8 mV. This way, $I_D = SR \times C_L = 8.05$ μA.

The aspect ratio of transistors T6/T7 can be obtained by using Eq. 7, with the difference that g_{m67} is obtained by doing

$$g_{m67} = \frac{2 \times I_D}{V_{OV}}, \tag{11}$$

in which V_{OV} is the voltage overdrive ($V_{OV} = V_{GS} - V_{THn}$) of transistors T6/T7.

Transistors T2 and T11 were designed taking as starting point their saturation voltage, as denoted by

$$V_{DSAT211} = SUPPLY\_AMS\_VDD - V_{fb} - |V_{THp}|. \tag{12}$$

Once $V_{DSAT211}$ is calculated, this result is then plugged into Eq. 13 and the aspect ratios for T2/T11 are obtained.

$$(W/L)_{211} = \frac{2 \times I_D}{K_p \times V_{DSAT211}^2}. \tag{13}$$

It is considered that the current mirror composed by transistors T6, T7, T8 and T9 should make copies of the current in the first stage of the main amplifier, i.e. $(W/L)_{67} = (W/L)_{89}$.

Transistors T12 and T13 were designed considering that $V_{DSAT1213} = (V_A - V_{THn})/2$, in which 188 mV $< V_A <$ 810.9 mV. Then, the aspect ratio of these transistors is calculated according to

$$(W/L)_{1213} = \frac{2 \times I_D}{K_n \times V_{DSAT1213}^2}. \tag{14}$$

Finally, the design of transistors T14 and T16 is made by assuming that $g_{m1416} = 10 \times gm_{01}$ and then this result is plugged into Eq. 7 in order to obtain the aspect ratio of T14/T16 [25].

It is important to highlight that for sub-micron technologies ($< 1\mu$m), second-order effects (body effect, channel modulation, etc.) are not taken into account by the modeling on Eq. 6, although they play a big role in such technologies. Thus, in order to refine the results obtained with the so called quadratic model, parametric analysis was performed and returned the aspect ratios used in this design.

IV. Results and Discussion

A. Schematic

With the circuit all set, several simulations were run in order to first determine the digital words that would be used to tune the gain of the PGA. Since there are 4 bits on the digital word that sets the convenient gain for the amplifier at a given moment, plus the bit of the switch of the degeneration resistors (V_{rs}), that means that there are 32 possibilities of gain for this PGA. However, only 8 values of gain were chosen using the criteria of achieving the most constant step of gain possible (2.5 dB) and which are represented on Table VI. Notice that the format of the digital word is 'b[3:0] - Vrs.' The plot of the gains vs. frequency is as depicted on Fig. 5.

Table VI. Gains and their Respective Digital Words (Schematic).

Digital Word	Gain	Bandwidth
0000-1	19.69 dB	7.56 MHz
0000-0	17.41 dB	7.56 MHz
0100-1	14.52 dB	13.71 MHz
0100-0	12.24 dB	13.73 MHz
1010-0	9.73 dB	18.36 MHz
1110-0	7.21 dB	24.48 MHz
0011-0	4.77 dB	31.91 MHz
1111-0	2.56 dB	40.96 MHz

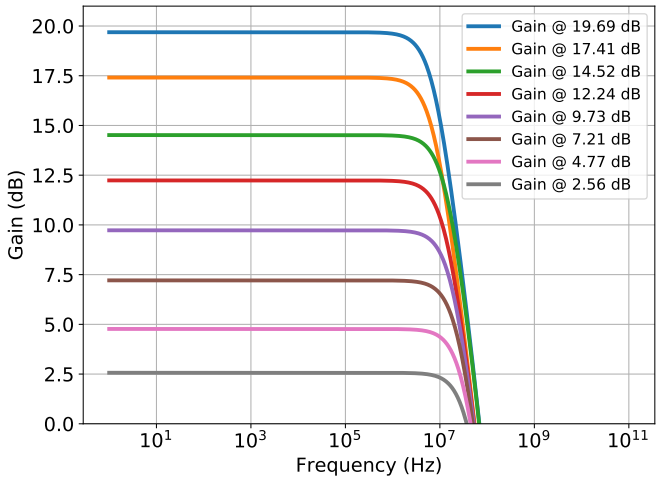

Fig. 5 AC Analysis - Schematic

The highest phase margin (@ 19.69 dB) is 104.8° and the lowest (@ 2.56 dB) is 50.88°. The main results for the simulations performed on the schematic of the PGA can be consulted on Table VII.

Furthermore, considering a pace of variation of gain equivalent to 2.5 dB, the maximum gain error found for this implementation was 0.5 dB.

B. *Corners*

To analyze the robustness of the design developed in this work it is fundamental that the design is put under non-ideal/extreme conditions. That means that the transistors and other devices involved in the design will be tested under conditions other than nominal for voltage supply, temperature and speed of transistors. What motivates such kind of test is the variability connected to these parameters of technology process.

Variability and mismatch rise from unbalanced parameters from device to device, or even from different operation than expected in the level of circuit design. Also, the measure of the driving current, which can either be I_{Dsat} or any other operating/biasing point, invokes a deterministic point of operation. However, when measuring real devices, the results will most likely deviate by a small amount of the operation point. In order to estimate these deviations, it is introduced the concept of weak and strong models respective to drive current, which synonyms are slow and fast, respectively. These deviations happen in a continuum of possible values, producing a classic Gaussian distribution [27].

In order to analyze the PGA designed under severe conditions, it is presented in Table VIII the setup of Process, Voltage and Temperature (PVT) variations to read the corners of the design.

Table VII. Results Summary of the PGA (Schematic).

Specification	Definition	Value
IRN @ 2.5 dB	Input referred noise @ 2.5 dB	32.14 nV/$\sqrt{Hz}$
IRN @ 20 dB	Input referred noise @ 20 dB	27.12 nV/$\sqrt{Hz}$
$A_v@f_c$	Voltage gain at the central frequency	2.56 - 19.69 dB
C_L	Load capacitance	700 fF
P_{av} @ 2.5 dB	Average Power @ 2.5 dB	101.9 μW
P_{av} @ 20 dB	Average Power @ 20 dB	103.1 μW
BW @ 2.5 dB	Bandwidth @ 2.5 dB	40.96 MHz
BW @ 20 dB	Bandwidth @ 20 dB	7.56 MHz

Table VIII. Corners Setup.

Parameter	Minimum	Typical	Maximum
Temperature (°C)	-40	27	125
Speed of Transistors	ss	tt	ff
Power Supply (V)	0.9	1	1.1

As for process variations, the weak and strong parameters of current drive respective to devices can be represented as: typical (tt), slow-slow(ss), slow-fast (sf), fast-slow (fs), fast-fast (ff). On Table IX the corner results for the specifications of the design when set to a gain of 2.56 dB are portrayed, while the results for a gain of 20 dB are presented on Table X.

Interpreting the corners results on Tables IX and X, it is noticeable that the specification that most suffer from severe conditions is the gain. The worst case is when the gain is in its minimum nominal value (2.56 dB) for this design, presenting a variability that even surpasses the actual nominal gain, as highlighted by the bold cells on Table IX. As for the nominal gain of 20 dB, this variability for severe conditions is meaningless for maximum condition (21.54 dB, $< 10\%$) and marginal for the minimum condition (16.72 dB, = 15%), as highlighted in *italic* on Table X.

Apart from the pronounced deviations on gain depicted on Table IX, the other specifications were within the spec-

Table IX. Corner Results for Typical Gain at 2.5 dB.

Specification	Min.	Typ.	Max.
Gain (dB)	**-710.90 m (ff, 125 °C, 0.9 V)**	2.56	**7.96 (ss, -40 °C, 1.1 V)**
Bandwidth (MHz)	26.14 (ss, -40 °C, 1.1 V)	40.96	55.13 (ff, -40 °C, 0.9 V)
IRN (nV/$\sqrt{Hz}$)	26.96 (ss, -40 °C, 1.1 V)	32.14	40.82 (ff, 125 °C, 0.9 V)
Power (μW)	76.22 (ss, -40 °C, 0.9 V)	101.90	137.5 (ff, 125 °C, 1.1 V)

Table X. Corner Results for Typical Gain at 20 dB.

Specification	Min.	Typ.	Max.
Gain (dB)	*16.72 (ss, -40 °C, 0.9 V)*	19.69	21.54 (ss, -40 °C, 1.1 V)
Bandwidth (MHz)	6.89 (ss, -40 °C, 0.9 V)	7.56	8.30 (ff, 125 °C, 1.1 V)
IRN (nV/$\sqrt{Hz}$)	22.64 (ss, -40 °C, 1.1 V)	27.12	35.32 (ss, 125 °C, 0.9 V)
Power (μW)	76.68 (ss, -40 °C, 0.9 V)	103.10	138.30 (ff, 125 °C, 1.1 V)

ified values on Table I, Section II.C. As a future enhancement of this design, in order to cover the deviations on minimum nominal gain corners, calibration transistors should be added. Also, as a suggestion for future work, a better circuit of voltage reference should be designed, such as the solution presented in [28]. This suggestion is made because it is considered that the circuit shown in Fig. 4 is most likely a source of considerable temperature variation, impacting on the performance of both the main amplifier and the CMFB.

C. *Layout (Extracted View)*

Once the design is performed, the following steps involve everything related to the layout (physical implementation of the design): floorplan, layout, Design Rule Checking (DRC), Layout versus Schematic (LVS), and parasitic extraction (QRC). The first step was to realize a previous sketch for the floorplan of the layout of the circuit and after some iterations it was possible to get to the final version of the floorplan, which is represented along with the actual layout of the circuit designed and represented on Fig. 6.

When performing the parasitics extraction and running the same simulations that were run to achieve the results that are detailed on Section IV.A, it was possible to obtain the results of the extracted view, which are expected to be more realistic than the schematic results. Such extracted view results are portrayed on Table XI and compared with measured results (post-fabrication) of two state of the art designs of a PGA, while the digital codes for the gains are shown on Table XII.

The maximum gain error found for the extracted view was 0.6 dB and the collection of gain plots for the extracted view is depicted on Fig. 7. Furthermore, the highest phase margin (@ 19.84 dB) is 100.3° and the lowest (@ 2.31 dB) is 49.00°.

The results on Table XI also indicate that the worst bandwidth of the PGA (Gain = 19.84 dB, BW = 5.59 MHz) is less than the worst bandwidth when only the schematic view is simulated (Gain = 19.69 dB, BW = 7.56 MHz). This happens because when the extracted view is analyzed or a fabricated circuit is measured, the parasitic capacitances and resistances introduced by routing, pads and signal coupling are considered, changing both the value of bandwidth and gain, as can be intuitively inferred from Eq. 7. The transconductance (g_m) and the output resistance are related to the gain, while the capacitance and output resistance are related to the time constant, which is related to the frequency.

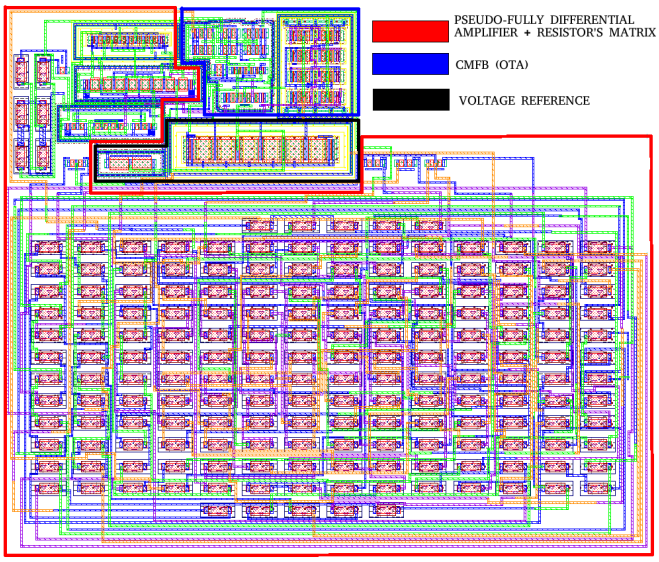

Fig. 6 Layout of PGA

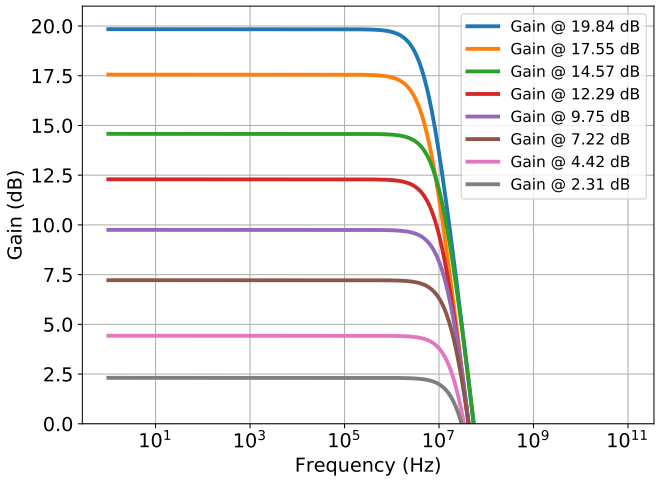

Fig. 7 AC Analysis - Extracted View

Table XI. Results Summary of PGA's Layout *vs.* State of the Art Designs.

Parameter	This work	[9][4]	[10][4]
Technology (nm)	130	180	28
Gain (dB)	2.31 - 19.84	0.20 - 18.40	34[1]
Bandwidth (MHz)	5.59	0.98	4[2]
IRN (nV/$\sqrt{Hz}$)	32.01 @ 2.31 dB	269 @ 12.8 dB	-
Supply voltage (V)	1	0.36	0.55
Power (μW)	103.1	15.4	900[3]
Area (mm^2)	0.004	0.0243	0.62[3]

[1] OTA + filter.
[2] Central frequency (f_c).
[3] Receiver (RX).
[4] Fabricated.

An important measure of this kind of circuit is the Common-Mode Rejection Ratio (CMRR), which is the rejection of common-mode signals for the benefit of differential mode signals. The common-mode voltage of a circuit can be disturbed by noise and mismatch, for instance, and disturb output swing. This way, the greater the CMRR, the lesser the influence of common-mode unbalance on the circuit. Such quantity can be expressed as seen in [14]

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|, \tag{15}$$

in which A_{CM} is the common-mode gain and A_{DM} is the differential mode gain. For the PGA, A_{CM} = -47.03 dB when A_{DM} = 20 dB and A_{DM} = 2.5 dB at the operating frequency (2 MHz). This way, the $CMRR_{20dB}$ = 2246.5 and $CMRR_{2.5dB}$ = 299.5 at 2 MHz. Thus, even in the worst situation (2.5 dB), the circuit provides a good CMRR.

It is noticeable that the design presented in this work outperforms the designs on [9] and [10] when it comes to maximum gain, bandwidth and area. Specifically, as for the maximum gain achieved in [10] it is important to highlight that the 34 dB gain presented is due to the contributions of gm-stage and filter designed, not the amplifier alone. This way,

Table XII. Gains and their Respective Digital Words (Layout).

Digital Word	Gain	Bandwidth
0000-1	19.84 dB	5.59 MHz
0000-0	17.55 dB	5.59 MHz
0100-1	14.57 dB	10.48 MHz
0100-0	12.29 dB	10.50 MHz
1010-0	9.75 dB	14.97 MHz
1110-0	7.22 dB	20.66 MHz
0011-0	4.42 dB	25.28 MHz
1111-0	2.31 dB	35.61 MHz

the gain due to the gm-stage itself is likely to be less than what is presented on Table XI. Furthermore, all the results in the present work are respective to a single stage of the PGA designed, while the results for what is depicted in [10] are due to the composition of four gm-stages and three filter stages. As for IRN, the present work outperforms what is seen on [9]. However, when it comes to power, this work outperforms what is presented on [10] and underperforms what is presented on [9]. The reason for the worst performance in power when compared to the latter has as main reason the reduced supply voltage (0.36 V) of [9]. Finally, the area achieved in the present work is 83.54% and 99.35% less than what is on [9] and [10], respectively.

Finally, it is important to highlight that this whole design was developed on Global Foundrie's 130 nm technology and the area occupied by the one cell of the PGA is equivalent to 0.004 mm^2 (68.61 μm $\times$ 57.53 μm). Lastly, the highest power dissipation of the PGA is equivalent to only 10.31 % (103.1 μW) of the total requirement for power dissipation of the receiver.

V. Conclusion

This work proposed the design of a Programmable Gain Amplifier (PGA) with 4 bits digital words and 8 out of 32 choices of gain for the system. Such circuit was designed based on a source degenerated topology for first stage (in a pseudo fully-differential fashion) and a common-source with resistive load for the second stage, with a gm boosting circuit in between these two stages. Given the variation of output common-mode, a common-mode feedback circuit (CMFB) was demanded, which was developed by realizing a simple OTA. In order to supply the reference voltage as one of the inputs of this CMFB, a reference circuit was also realized.

After defining the aspects ratios of the transistors of the circuits and the resistances, where necessary, a handful of simulations were performed. Once the specifications were met, it was proceeded to the physical implementation and after this stage passed the tests of DRC and LVS, the parasitics extraction could be realized. Again, the same tests that were run on schematic were also run on extracted view and put against. The results of the extracted view are the ones expected to be the closest to reality and are in conformance with the specifications. This whole design was developed on GF's 130 nm technology and takes an area of 0.004 mm^2, outperforming state of the work designs ([9] and [10]) when it comes to maximum gain, bandwidth, IRN and area. Finally, notice that the highest power dissipation of the extracted circuit is equivalent to 103.1 μW, representing 10.31 % of the total power dissipation required for the receiver.

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