Fabrication and electrical characterization of Ultra-Thin Body and BOX (UTBB) Back Enhanced SOI (^{BE}SOI) pMOSFET

Ricardo C. Rangel[1,2,*], Katia R. A. Sasaki[1], Leonardo S. Yojo[1] and João A. Martino[1]

[1] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[2] FATEC-SP, Faculdade de Tecnologia de Sao Paulo - Sao Paulo, Brazil
*e-mail: rrangel@lsi.usp.br

***Abstract*— This work analyzes the third generation ^{BE}SOI MOSFET (Back-Enhanced Silicon-On-Insulator Metal-Oxide-Semiconductor Field-Effect-transistor) built on UTBB (Ultra-Thin Body and Buried Oxide), comparing it to the ^{BE}SOI with thick buried oxide (first generation). The stronger coupling between front and back interfaces of the UTBB ^{BE}SOI device improves in 67% the current drive, 122% the maximum transconductance and 223% the body factor. Operating with seven times lower back gate bias, the UTBB ^{BE}SOI MOSFET presented more compatibility with standard SOI CMOS (Complementary MOS) technology than the ^{BE}SOI with thick buried oxide.**

***Index Terms* — ^{BE}SOI MOSFET, UTBB, fabrication and characterization.**

I. Introduction

In order to overcome the scaling limits, MuGFET (Multiple Gate Field-Effect-Transistor), UTBB SOI (Ultra-Thin Body and Buried oxide Silicon-On-Insulator), Tunnel-FET and stacked nanowires have been considered for current and future electronics [1-6]. Their performances are enhanced by a better electrostatic control of the gate on the channel or by changing the conduction mechanism. Another approach for a space saving is the concept of a reconfigurable device [7-15]. They have been developed for reprogrammable logic circuits [12-15], where, by changing the type of the transistors, a same wafer area can act for more than one function.

In 2015, the first generation of ^{BE}SOI (Back-Enhanced Silicon On Insulator) was developed [16] with a simpler CMOS (Complementary Metal-Oxide-Semiconductor) compatible fabrication process, with no doping process and fewer photolithography steps. It is a new kind of a reconfigurable device, i.e., it can work as an n-type or p-type transistor depending only on the back-gate bias (V_{GB}) [16-24]. Their working principle and electric characterization were explored for two electrodes material (Aluminum and Nickel), at room and high temperatures, including the influence of Schottky source and drain contacts [16-19]. In addition, some applications like inverter circuit, biosensor and light sensor were analyzed in [19-24].

The p-type ^{BE}SOI MOSFET works by accumulating the back interface (top silicon film/buried oxide) with a negative enough V_{GB}. The hole channel can be controlled by the front gate bias (V_{GF}). When the V_{GF} is higher than the threshold voltage (V_T), in case of p-type MOSFET, the depletion region reaches the back interface, ceasing the current flow [16-17].

However, a high V_{GB} value (magnitude higher than 15V) is needed for the ^{BE}SOI device with thick buried oxide. Therefore, a ^{BE}SOI MOSFET built on a UTBB wafer would allow its operation with a lower V_{GB} with a similar current. The reduction in V_{GB} is an important step towards its integration with CMOS, SOI CMOS and UTBB SOI CMOS technologies. Moreover, the hybrid technology, where there are UTBB and MOS devices on a same wafer [25], would facilitate the access to the back gate through an independent contact on top of the wafer.

This work focus on the new UTBB ^{BE}SOI MOSFET fabricated and measured at LSI/USP (Laboratório de Sistemas Integráveis da Universidade de São Paulo), analyzing its functionality and advantages/disadvantages over the ^{BE}SOI with thick buried oxide [16].

II. Fabrication Process

The first generation ^{BE}SOI MOSFET (Fig. 1a and b) starts with an SOI wafer with 200nm-thick buried oxide layer underneath a 100nm-thick and 10^{15}cm^{-3}, p-type top silicon layer. After a silicon thinning procedure, the active region is defined through a MESA isolation (first photolithography and reactive-ion etching, RIE). Then, a dry thermal oxidation, Al deposition and a second photolithography were done to form the gate stack, resulting in a front gate oxide thickness of 15nm and a final top-Si layer of 23nm. Finally, a third photolithography, another Al deposition, a lift-off and an annealing processes determine the contacts [16].

Differently, a SOITEC© UTBB wafer with 25nm-thick buried oxide and top silicon layer of 14nm-thick and 10^{15}cm^{-3} of boron (Si-P) was used for fabricating the UTBB ^{BE}SOI MOSFET (Fig. 1c and d). Here, the active region was also defined by a MESA isolation with a reactive-ion etching (RIE) adjusted for better selectivity to keep the buried oxide intact, followed by the front gate dry oxidation and the metal gate deposition and definition, resulting in 10nm of front gate oxide thickness on 9nm-thick of top silicon film. Then, a PECVD was done for the field oxide deposition. Finally, the contacts were opened through a third lithography and the electrodes were deposited, defined by a lift-off process (fourth lithography) and annealed [26]. Fig. 1e depicts a schematic cross-section of the ^{BE}SOI MOSFET and Table I gives us the final dimensions of the ^{BE}SOI and UTBB ^{BE}SOI MOSFET previously described.

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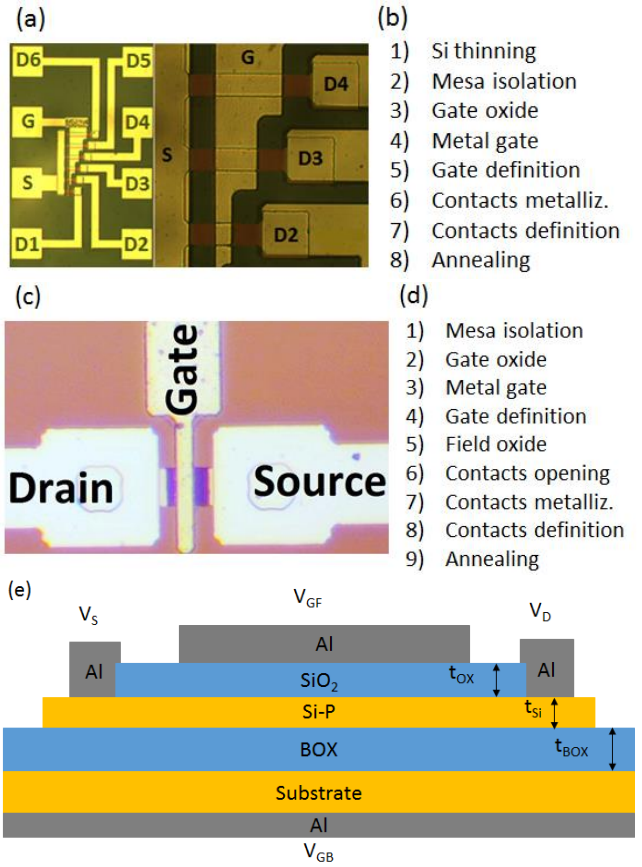

Fig.1 (a) Picture of an L-array and (b) its fabrication steps of the ^{BE}SOI MOSFET. (c) Picture of an isolated transistor and (d) its fabrication steps of the UTBB ^{BE}SOI MOSFET. (e) schematic cross-section of the ^{BE}SOI MOSFET

Table I. Final dimensions of the ^{BE}SOI and UTBB ^{BE}SOI.

	^{BE}SOI	UTBB ^{BE}SOI
t_{OX} (nm)	15	10
t_{Si} (nm)	23	9
t_{BOX} (nm)	200	25
L (µm)	50	
W (µm)	10	

III. Electrical Characteristics

In order to verify the proper functioning of the UTBB ^{BE}SOI, this section presents the main electrical characteristics, comparing it with the ^{BE}SOI with thick buried oxide. Figs. 2 and 3 show the transfer characteristics in linear and log scales of ^{BE}SOI and UTBB ^{BE}SOI, respectively, for various back gate bias (V_{GB}) and drain bias (V_D) of -100mV. The front and back gate biases were chosen in order to avoid damages to the buried oxide in both technologies. As the main goal of this work is to analyze the influence of the BOX thickness reduction, both devices have channel width (W) and length (L) of 10µm and 50µm, respectively, as well as for all the following analysis. 91 functional transistors were measured across the wafer with 87% yield, all of them with similar behavior.

Both transistors present an increased drain current and threshold voltage (V_T) for more negative V_{GB} (Figs. 2 and 3). The stronger electric field generated by the higher $|V_{GB}|$ induces more holes at the back interface, which raises the drain current and the front gate bias (V_{GF}) needed to block the drain current, i.e., the V_T [16-19].

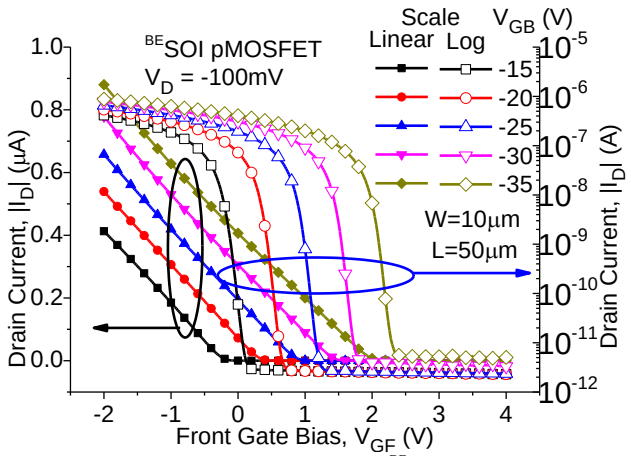

Fig.2 Transfer characteristics ($I_D(V_{GF})$) of the ^{BE}SOI transistor for different back gate bias (V_{GB}) in linear (left) and log-scale (right).

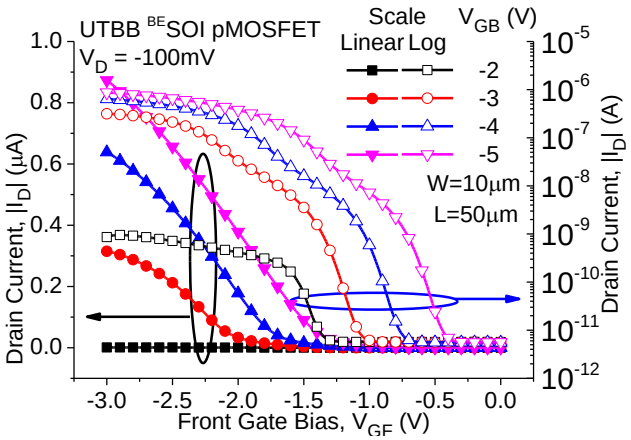

Fig.3 Transfer characteristics ($I_D(V_{GF})$) of the UTBB ^{BE}SOI transistor for different back gate bias (V_{GB}) in linear (left) and log-scale (right).

Looking at the differences, Fig. 3 clearly shows a reduction of the V_{GB} used to achieve the same drain current for UTBB ^{BE}SOI over the ^{BE}SOI with thick buried oxide (from 35V in Fig. 2 to 5V in Fig. 3), due to the stronger electric field caused by the thinner buried oxide (from 200nm to 25nm).

Fig. 3 (linear scale) also indicates a stronger I_D degradation caused by the V_{GF} for higher V_{GB} (discussion next to Fig. 7 and Table V).

Still in Fig. 3 (log-scale), it is noticeable an elevation of the drain current for two different V_{GF} values (for example, for V_{GB}=-4V, these V_{GF}'s are around -1V and -2V), mainly for $V_{GB} \leq$ -3V, which is not present for ^{BE}SOI with thick buried oxide (Fig.2). A first possible explanation for these two elevations is the edge transistor [27-28]. However, the influence of the V_{GB} on the drain current of the edge transistor is weaker than of the main transistor. The result is a smaller V_T shift with the V_{GB} in an $I_D(V_{GF})$ characteristics [28]. This hypothesis is refused by the close values of the coupling coefficients (slope of the $V_T(V_{GB})$ curve) extracted from both interfaces, using the transconductance change method [29] (Fig. 4, data on the left are for ^{BE}SOI with thick buried oxide [16] and on the right, for UTBB ^{BE}SOI).

Actually, these two conductions are related to the formation of the front and the back channel, a common phenomenon in UTBB devices [30]. Moreover, in a ^{BE}SOI de-

vice, the source and drain doping come from the accumulation provided by the V_{GB}, unlike the conventional MOSFET, whose source and drain is formed by a doping process. It means that the drain current from the back interface is raised earlier (Fig. 3) or, at the same time (discussion next to Figs. 5 and 6), than the one from the front interface. Therefore, following [17], the first elevation of the drain current observed in Fig. 3 is the back-channel conduction and then, for more negative V_{GF}, the front interface is accumulated.

Furthermore, Fig. 4 also presents the coupling coefficients (α) obtained through experimental results for ^{BE}SOI and UTBB ^{BE}SOI devices and Table II presents the coupling coefficients considering the conduction at the front (α_F) and back (α_B) interfaces given by the capacitance model of (1), (2) and (3), respectively [28].

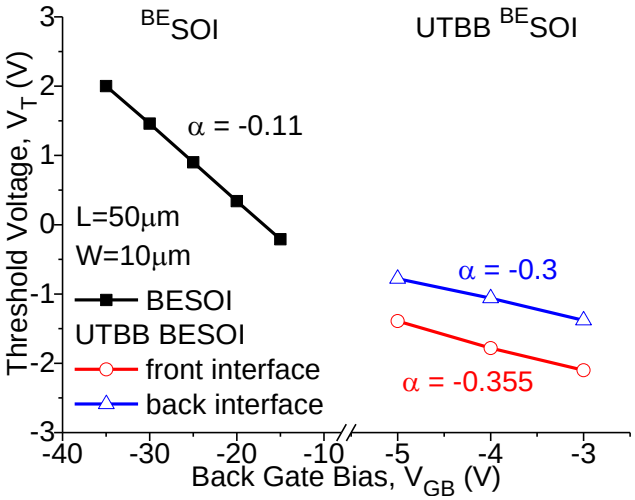

Fig.4 Threshold voltage as a function of the back gate bias of the ^{BE}SOI transistor (left) and UTBB ^{BE}SOI (right).

Table II. Coupling coefficients (α_F and α_B) of the ^{BE}SOI and UTBB ^{BE}SOI MOSFET, considering front and back interface conductions, respectively. Bold values are the ones closer to the experimental α.

Equation	^{BE}SOI	UTBB ^{BE}SOI
α_F given by (1)	0.072	**0.358**
α_B given by (2) for ^{BE}SOI [16] and (3) for UTBB ^{BE}SOI	**0.112**	0.288

Where:

- $\alpha_F = \frac{\left(\left(\frac{1}{C_{Si}}\right)+\left(\frac{1}{C_{BOX}}\right)\right)^{-1}}{C_{OX}}$ (1)
- $\alpha_{B,BESOI} = \frac{C_{BOX}}{\left(\left(\frac{1}{C_{Si}}\right)+\left(\frac{1}{C_{OX}}\right)\right)^{-1}}$ (2)
- $\alpha_{B,UTBB\ BESOI} = \frac{\left(\left(\frac{1}{C_{BOX}}\right)+\left(\frac{1}{C_{SUB}}\right)\right)^{-1}}{\left(\left(\frac{1}{C_{Si}}\right)+\left(\frac{1}{C_{OX}}\right)\right)^{-1}}$ (3)
- C_{Si}, C_{BOX}, C_{OX} and C_{SUB} are the capacitances per unit area of the silicon, buried oxide, gate oxide and the BOX-substrate depletion layers, respectively.

Table III. Subthreshold swing extracted from the I_D (V_{GF}) characteristics of the ^{BE}SOI and UTBB ^{BE}SOI MOSFET.

^{BE}SOI		UTBB ^{BE}SOI	
V_{GB} (V)	SS_F (mV/dec.)	V_{GB} (V)	SS_F (mV/dec.)
-15	83.5	-2	136.6
-20	81.9	-3	112.7
-25	81.0	-4	112.1
-30	81.7	-5	113.9

For ^{BE}SOI device, it is possible to observe that the experimental α (0.11) matches to the one calculated through equation (2) (0.112). It means that most of the drain current is flowing at the back interface. On the other hand, for UTBB ^{BE}SOI, the experimental α at the front interface (0.355) is close to the one obtained through equation (1) (0.358), indicating a main conduction at the front interface. In other words, the silicon thinning from 23nm to 9nm and buried oxide thinning from 200nm to 25nm favors the conduction at the front interface. It is important to mention that capacitance due to substrate depletion (C_{SUB}) is significant when the buried oxide is very thin (UTBB). But when the buried oxide is thick, this depletion layer is not relevant and equation (3) can be simplified to equation (2).

Looking at their values, (0.355 for UTBB ^{BE}SOI and 0.11 for ^{BE}SOI with thick buried oxide) a 217% higher is obtained for UTBB ^{BE}SOI device due to the stronger coupling provided by the thinner silicon layer and buried oxide. This stronger coupling also benefits the current drive (Fig. 3 when compared to the ^{BE}SOI with thick buried oxide) the subthreshold slope extracted from I_D (V_{GB}) (as can be seen in Figs. 5 and 6 and Table IV when different biases are analyzed) and the maximum transconductance (discussion next to Fig. 7). However, the higher coupling coefficient of the UTBB ^{BE}SOI also increases the subthreshold slope (38% higher) extracted from $I_D(\underline{V_{GF}})$ (SS_F) using its definition ($SS_F = (d(\log(I_D))/dV_{GF})^{-1}$) [28] and presented in table III together with the ones from ^{BE}SOI. Once the SS_F can be calculated by equation 4 [28], it is directly proportional to the coupling coefficient. Thus, a higher SS_F for UTBB ^{BE}SOI is expected.

$$SS_F = \frac{kT}{q}(1+\alpha)ln(10) \quad (4)$$

In order to analyze the origin of the conductions (front and back interfaces), Figs. 5 and 6 present the I_D (V_{GB}) characteristic, i.e., the drain current of the UTBB ^{BE}SOI previously described as a function of the back-gate sweep for different front gate biases. The subthreshold slope extracted from the $I_D(\underline{V_{GB}})$ ($SS_B = (d(\log(I_D))/dV_{GB})^{-1}$) is shown in Table IV.

For $V_{GF} \leq$ -2.5V, the accumulation of both interfaces is close enough to not be seen separately. In these cases, the drain current that is flowing at the back interface is raised at the same time as the one from the front interface. As explained before, in a ^{BE}SOI transistor, the source and drain regions are formed by the V_{GB} and not by a doping process. Therefore, there is no drain current if the front channel is accumulated but the source and drain is still depleted. On the other hand, once with source and drain accumulated, the drain current starts to flow at both interfaces at the same time and a lower subthreshold slope (SS_B) can be achieved (Table

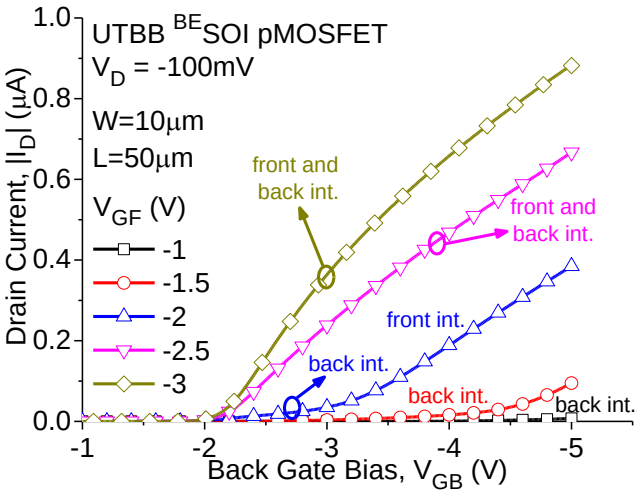

Fig.5 Drain current in linear scale as a function of the back gate bias ($I_D(V_{GB})$) of the UTBB ^{BE}SOI transistor for various front gate bias (V_{GF}).

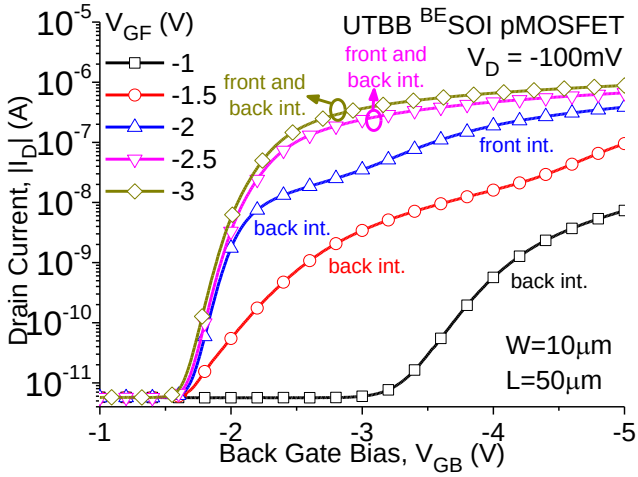

Fig.6 Drain current in log scale as a function of the back-gate bias ($I_D(V_{GB})$) of the UTBB ^{BE}SOI transistor for various front gate bias (V_{GF}).

Table IV. Subthreshold swing extracted from the I_D (V_{GB}) characteristics of the UTBB ^{BE}SOI MOSFET.

V_{GF} (V)	SS_B (mV/dec)
-1	346
-1.5	322
-2	116
-2.5	115
-3	113

IV). Besides, the strong coupling is also beneficially acting, which is better observable for $V_{GF} \leq$ -2V.

For V_{GF} = -2V, in spite of the two drain current elevations are separately observable, they are close enough to lead to a lower SS_B. In this case, the accumulation of both interfaces starts to split, but they are still close enough for the front interface to influence the back one (thanks to the strong coupling), since the SS_B is still 116mV/dec., a value close to the SS_B for $V_{GF} \leq$ -2.5V (Table IV).

For $V_{GF} \geq$ -1.5V, one can see the raise of the drain current once and with a higher SS_B. It means that the front interface did not accumulate during the range while the back channel is forming. In this case, the coupling between both interfaces is weaker and there is an SS_B degradation (Table IV).

Fig. 7 compares the transconductance (g_m) for ^{BE}SOI [16] and UTBB ^{BE}SOI during the V_{GF} sweep for various V_{GB}. and Table V, their transconductance/mobility degradation (θ) also for each V_{GB} [28].

Fig. 7 indicates an enhancement of 122% on the $g_{m,max}$ of the UTBB ^{BE}SOI (600nS) when compared to the ^{BE}SOI with thick buried oxide (270nS) thanks to the stronger coupling. Besides, as the higher part of the drain current flows at the front interface in UTBB ^{BE}SOI, the influence of the V_{GF} is greater than in ^{BE}SOI, where most of the drain current is at the back interface. The $g_{m,max}$ is also raised by applying a lower V_{GB}, which means more carriers to form the channel.

Concerning the transconductance degradation with V_{GF} (θ), as the V_{GB} is more negative, a higher part of the drain current flows at the back interface. Therefore, the transconductance degradation (θ) is reduced (improved), as indicated by Fig. 7 and Table V.

As the change from ^{BE}SOI to UTBB ^{BE}SOI is also towards rising the conduction at the front interface, which is more affected by V_{GF}, the transconductance degradation for UTBB ^{BE}SOI (for V_{GB}=-3V) is almost six times higher than for ^{BE}SOI with thick buried oxide (for V_{GB}=-15V, Table V). However, as previously discussed, a lower V_{GB} can reduce this degradation.

From the differentiation of the curves from Figs. 5 and 6, Fig. 8 completes the $I_D(V_G)$ analysis, with the transconductance related to the V_{GB} (g_B) during the V_{GB} sweep for various V_{GF}.

Improvements on the transconductance (g_B) of 43% and 125% can be observed (Fig. 8) when both interfaces are accumulated almost together (293nS for V_{GF}=-2.5V and 459nS for V_{GF}=-3V) over when their drain current start to flow separately (204nS for V_{GF}=-2V).

One can also notice that the maximum transconductance (g_m=600nS) is higher than the one related to V_{GB}, (g_B=459nS). Since, in UTBB ^{BE}SOI, most of the drain current is at the front interface, it is expected a stronger influence of the V_{GF} than of the V_{GB}.

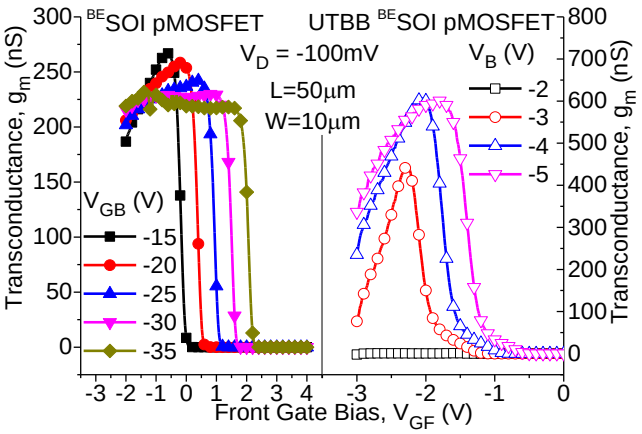

Fig.7 Transconductance of the ^{BE}SOI (left) and UTBB ^{BE}SOI (right) transistor during the V_{GF} sweep for various V_{GB}.

Table V. Transconductance degradation extracted from the g_m (V_{GF}) characteristics of the UTBB ^{BE}SOI MOSFET.

^{BE}SOI		UTBB ^{BE}SOI	
V_{GB} (V)	θ (V^{-1})	V_{GB} (V)	θ (V^{-1})
-15	-0.49	-2	-5.81
-20	-0.24	-3	-2.73
-25	-0.12	-4	-0.79
-30	-	-5	-0.27

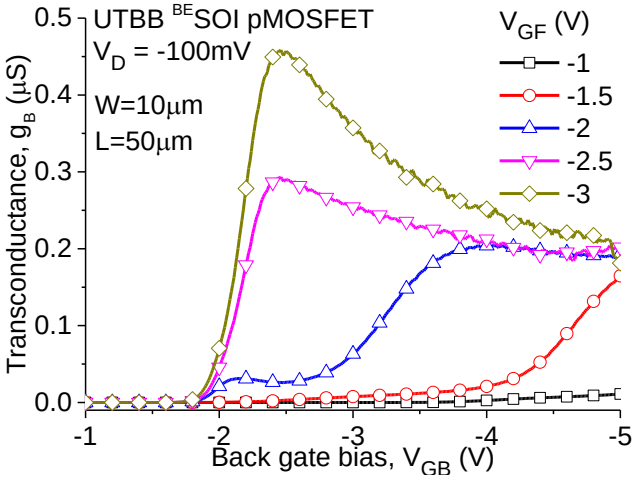

Fig.8 Transconductance related to the V_{GB} (g_B) of the UTBB BESOI during the V_{GB} sweep for various V_{GF}.

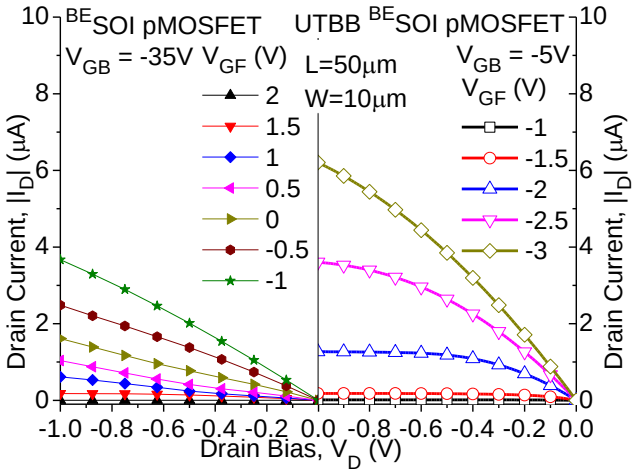

Fig.9 Output characteristics ($I_D(V_D)$) of the BESOI (left) and UTBB BESOI transistor (right) for different V_{GF}.

Finally, the output characteristics ($I_D(V_D)$) can be seen in Fig. 9 for BESOI with V_{GB} = -35V [16] and UTBB BESOI with V_{GB} = -5V.

In spite of the higher series resistance due to the thinner t_{Si}, the conduction at both interfaces increases from 3.7µA to 6.2µA (Fig. 9) for V_D = -1V and lowest V_{GF} measured, which means a 67% higher I_D.

IV. Conclusions

The third generation BESOI MOSFET on UTBB wafer was fabricated, analyzed and compared to the first generation BESOI with thick BOX.

The stronger coupling presented by changing from BESOI with thick buried oxide to UTBB BESOI MOSFET brought several advantages. The enhancement on the front interface conduction when the back channel is already formed improves the device performance by rising in 67% the current drive, 122% the maximum transconductance and 223% the coupling coefficient, α (consequently, the body effect, n), while still using seven times lower biases and a simpler fabrication process. The drawback observed were the 38% higher subthreshold slope and the almost six times higher transconductance degradation with V_{GF} (θ), which can be lowered by raising the back-gate bias.

Therefore, the stronger coupling, higher α and drain current, lower back gate biases and simplicity of fabrication make the UTBB BESOI MOSFET more compatible with the standard SOI CMOS technology than the BESOI with thick BOX, being more promising for future integrated circuits applications.

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References

[1] H. Iwai, "Future of Nano CMOS Technology," *Solid-State Electronics*, vol. 112, October, 2015, https://doi.org/10.1016/j.sse.2015.02.005, p. 56-67.

[2] L. Le Pailleur, "Fully-Depleted-Silicon-On-Insulator from R&D concept to industrial reality," in *2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, USA, October, 2013, https://doi.org/10.1109/S3S.2013.6716511, p.1-2.

[3] T. Chiarella et al., "Benchmarking SOI and bulk FinFET alternatives for PLANAR CMOS scaling succession," *Solid-State Electronics*, vol. 54, no. 9, September, 2010, https://doi.org/10.1016/j.sse.2010.04.010, p. 855-860.

[4] A. M. Ionescu and H. Riel, "Tunnel field-effect-transistors as energy efficient electronic switches," *Nature*, vol. 479, November, 2011, https://doi.org/10.1038/nature10679, p. 329-337.

[5] L. Gaben et al., "(Invited) Evaluation of Stacked Nanowires Transistors for CMOS: Performance and Technology Opportunities," *ECS Transactions*, vol. 72, no. 4, May, 2016, https://doi.org/10.1149/07204.0043ecst, p. 43-54.

[6] IEEE, "International Roadmap for Devices and Systems – More Moore", 2017 edition, https://irds.ieee.org/roadmap-2017, accessed in March, 2019.

[7] C. Navarro, S. Barraud, S. Martinie, Lacord J., M.-A. Jaud and M. Vinet, "Reconfigurable field effect transistor for advanced CMOS: A comparison with FDSOI devices," in *2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Austria, January, 2016, https://doi.org/10.1109/ULIS.2016.7440038, p. 5-8.

[8] T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick and W. M. Weber, "Stress-Engineering for Improved Tunneling in Reconfigurable Silicon Nanowire Transistors," in *2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Austria, January, 2016, https://doi.org/10.1109/ULIS.2016.7440037, p.1-4.

[9] F. Wessely, T. Krauss and U. Schwalke, "Reconfigurable CMOS with undoped silicon nanowire midgap Schottky-barrier FETs," *Microelectronics Journal*, vol. 44, no. 12, December, 2013, https://doi.org/10.1016/j.mejo.2012.08.004, p. 1072-1076.

[10] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick and W. M. Weber, "Reconfigurable Silicon Nanowire Transistors," *Nano letters*, vol. 12, no. 1, November, 2011, https://doi.org/10.1021/nl203094h, p. 119-124.

[11] T. Krauss, F. Wessely and U. Schwalke, "Eletrically reconfigurable dual metal-gate planar field-effect transistor for dopant-free CMOS," in *13th International Multi-Conference on Systems, Signals & Devices*, Germany, March, 2016, https://doi.org/10.1109/SSD.2016.7473724, p. 681-686.

[12] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick and W. M. Weber, "Elementary Aspects for Circuit Implementation of Reconfigurable Nanowire Transistors," *IEEE Electron Device Letters*, vol. 35, no. 1, January, 2014, https://doi.org/10.1109/LED.2013.2290555, p. 141-143.

[13] M. Simon, A. Heinzig, J. Trommer, T. Baldauf, T. Mikolajick and W. M. Weber, "Bringing reconfigurable nanowire FETs to a logic circuits compatible process platform," in *2016 IEEE Nanotechnology Materials and Devices Conference (NMDC)*, France, October, 2016, https://doi.org/10.1109/NMDC.2016.7777085, p. 1-3.

[14] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick and W. M. Weber, "Functionality-Enhanced Logic Gate Design Enabled by Symmetrical Reconfigurable Silicon Nanowire Transistors," *IEEE Transactions on Nanotechnology*, vol. 14, no. 4, May, 2015, https://doi.org/10.1109/TNANO.2015.2429893, p. 689-698.

[15] U. Schwalke, T. Krauss and F. Wessely, "Dopant-Free CMOS on SOI: Multi-Gate Si-Nanowire Transistors for Logic and Memory Applications,"

ECS Transactions, vol. 53, no. 5, May, 2013, https://doi.org/10.1149/05305.0105ecst, p. 105-114.

[16] R. C. Rangel and J. A. Martino, "Back Enhanced (BE) SOI pMOSFET" *Proc. of 30th Symposium on Microelectronics Technology and Devices (SBMicro)*, Brazil, September, 2015, https://doi.org/10.1109/SBMicro.2015.7298121, p.1-4.

[17] L. Yojo, R. C. Rangel, K. R. A. Sasaki and J. A. Martino, "Back Enhanced (BE) SOI MOSFET under non-conventional bias conditions" *Proc. of Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Greece, April, 2017, https://doi.org/10.1109/ULIS.2017.7962562, p. 1-4.

[18] L.S. Yojo, R.C. Rangel, K.R.A. Sasaki, J.A. Martino, "Optimization of Source/Drain Schottky Barrier Height on BE SOI MOSFET", *ECS Transactions*, vol. 85, no. 8, May, 2018, https://doi.org/10.1149/08508.0079ecst, pp. 79-84.

[19] K.R.A. Sasaki, R.C. Rangel, L.S. Yojo and J.A. Martino, "Tradeoff between the transistor reconfigurable technology and the zero-temperature-coefficient (ZTC) bias point on BESOI MOSFET", *Microelectronics Journal*, vol.94, December, 2019, https://doi.org/10.1016/j.mejo.2019.104658, p. 104658.

[20] L. S. Yojo, R. C. Rangel, K. R. A. Sasaki and J. A. Martino, "Optimization of the permittivity-based BE SOI biosensor" *Proc. of SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, USA, October, 2018, https://doi.org/ 10.1109/S3S.2018.8640139, p.1-3.

[21] J. A. Padovese, L. S. Yojo, R. C. Rangel, K. R. A. Sasaki and J. A. Martino, "Optimization of the silicon thickness on Back Enhanced (BE) SOI pMOSFET working as a visible spectrum light sensor", *Proc. of SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, USA, October, 2018, https://doi.org/10.1109/S3S.2018.8640140, p.1-3.

[22] L. S. Yojo, R. C. Rangel, K. R. A. Sasaki and J. A. Martino, "Influence of biological element permittivity on BE SOI MOSFETs" *Proc. of 33rd Symposium on Microelectronics Technology and Devices (SBMicro)*, Brazil, August, 2018, https://doi.org/10.1109/SBMicro.2018.8511350, p. 1-4.

[23] J. A. Padovese, L. S. Yojo, R. C. Rangel, K. R. A. Sasaki and J. A. Martino, "Back Enhanced SOI MOSFET as UV light sensor", *Proc. of 33rd Symposium on Microelectronics Technology and Devices (SBMicro)*, Brazil, August, 2018, https://doi.org/10.1109/SBMicro.2018.8511328, p.1-4.

[24] J. A. Padovese, R. C. Rangel, K. R. A. Sasaki and J. A. Martino, "Thin Si channel Back Enhanced (BE) SOI pMOSFET photodetector under different bias conditions", Proc. of EUROSOI-ULIS 2019, France, April, 2019, https://doi.org/10.1109/EUROSOI-ULIS45800.2019.9041870, p.1-4.

[25] C. Fenouillet-Beranger et al., "Hybrid FDSOI/bulk High-k/metal gate platform for low power (LP) multimedia technology," in *2009 IEEE International Electron Devices Meeting (IEDM)*, USA, December, 2009, https://doi.org/10.1109/IEDM.2009.5424251, p. 28.6.1-28.6.4.

[26] K. R. A. Sasaki, R. C. Rangel, L. S. Yojo and J. A. Martino, "Third Generation ^{BE}SOI (Back-Enhanced SOI) pMOSFET fabricated on UTBB Wafer", *Proc. of SBMicro* 2019, Brazil, August, 2019, https://doi.org/10.1109/SBMicro.2019.8919335, p. 1-4.

[27] R. C. Rangel and J. A. Martino, "Proposal of a process design methodology of fully depleted SOI nMOSFET using only three photolithograph steps for educational application." *Proc. Of 29th Symposium on Microelectronics Technology and Devices (SBMicro)*, Brazil, September, 2014, https://doi.org/10.1109/SBMicro.2014.6940124, p.1-5.

[28] J.-P. Colinge, *Silicon-on-insulator technology: Materials to VLSI*, 3rd ed., Kluwer Academic Publishers, 2004.

[29] H. S. Wong; M. H. White; T. J. Krutsick; R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET's". Solid-State Electronics, vol. 30, 1987, https://doi.org/10.1016/0038-1101(87)90132-8 , p. 953-968.

[30] K. R. A. Sasaki, C. Navarro, M. Bawedin, F. Andrieu, J. A. Martino and S. Cristoloveanu, "Impact of Supercoupling Effect on Mobility Enhancement in UTBB SOI MOSFETs in Dynamic Threshold Mode" *Proc. of SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, USA, October, 2015, https://doi.org/10.1109/S3S.2015.7333547, p.1-3.