Output conductance of Line-TFETs for different device parameters and its effect on basic analog circuits

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***Abstract*—This work addresses the impact of different device parameters on the analog characteristics of Line-Tunneling Field Effect Transistors (Line-TFETs). It was shown that increasing source-to-drain separation from 25 nm to 45 nm reduces output conductance degradation for high drain voltages but increases the saturation voltage in about 400 mV due to the increase in the inner resistance. Variation of 4nm in the pocket thickness, a major cause of device variability, resulted in a 50-fold reduction of the drain current, but the output conductance reaches the same value in all cases for sufficiently high Vds. The variation of the main parameters responsible for device variability (pocket thickness and doping and gate-source alignment) is performed in order to analyze their impact on current mirrors, revealing that gate-source overlap of 3 nm decreases the minimum output voltage from 820 mV to 300 mV, in comparison with no misalignment and improves the analog characteristics of the Line-TFET by preventing output conductance degradation for high drain voltages. Simulations compared to experimental data show that the output conductance (gd) of Line-TFETs is practically independent of the gate length. Simulations reveal that this unique characteristic is due to source-to-drain tunneling, which defines the average value of gd on the saturation-like region and does not depend upon the gate length. The impact of this characteristic on the design of a common-source stage is shown by comparing with a MOSFET design. This example shows that the designer may choose whether to increase gm or gd in order to increase the circuit gain when using Line-TFETs, fundamentally differing from the MOSFET case.**

***Index Terms*—Line-TFET, output conductance, analog design.**

I. Introduction

Tunnel Field Effect Transistors (TFETs) have been proposed as a possibility for overcoming the present Moore's Law limitations because these devices present the possibility of achieving subthreshold slopes (SS) smaller than 60mV/decade at room temperature. However, these devices present Phonon and Trap Assisted Tunneling (TAT), which degrades SS, and low drain currents, especially for silicon devices and simple topologies [1]. The Line-TFET used in this work, fabricated at imec/Belgium, is one example of a tunneling device that presents an innovative topology in order to overcome the aforementioned issues [2].

Even with optimized architectures, TFETs hardly achieve the current levels and SS necessary for surpassing MOSFET devices in high-density digital applications [1]. However, those devices, including the Line-TFET, present characteristics that may be suitable for some analog applications, especially in signal amplification, as they present extremely low output conductance (gd) and, consequently, high intrinsic voltage gain [3][4][5] and resistance to temperature variation [6]. The literature presents little insight, especially based on experimental results, on how the analog characteristics of Line-TFETs depend upon the device's dimensions and non-idealities. One exception is [5], in which the authors discuss that the minimum gate bias in this device is around 1V because of saturation region degradation Therefore, this work studies the impact on its analog characteristics of varying source-to-drain separation, pocket thickness, pocket doping, gate-source alignment and the gate length. These parameters are studied in both device and circuit levels, considering the examples of a current mirror and a common-source stage.

II. Device structure and working principle

Fig. 1.a) depicts the Line-TFET used in this work, fabricated at imec/Belgium. Fabricated on an SOI wafer and using shallow trench isolation (STI) between devices, it has a $Si_{0.55}Ge_{0.45}$ source region extended along the entire gate length (equal to Lg), ideally being aligned with the gate end. This region lies beneath a very thin strained silicon region (the pocket), which is about 5 nm thick and is ideally undoped. However, due to temperature variation across the wafer, the pocket thickness may vary over 2 nm, the pocket doping may reach values above 10^{19} cm^{-3} (due to diffusion from the source), and gate-source misalignment may reach some nanometers [2]. The impact of these variations on the device's analog characteristics will be analyzed on section III. Between the source and the drain, there is another undoped silicon region (with length Lsd). The drain has n-type doping in a concentration of 5.10^{18} cm^{-3} in order to suppress ambipolar current. The gate stack is composed of SiO_2/HfO_2(1.8nm)/TiN(2nm)/P-doped α-Si and has an effective oxide thickness (EOT) of 0.9 nm and length Lg. Fig. 1-b) depicts the band diagram along the vertical direction, showing that band-to-band tunneling happens from the source valence band (Ev) to the pocket conduction band (Ec) on the vertical direction and, as it happens evenly along the entire gate length, it is called line-tunneling. Ec quantization occurs in the pocket region because of its small thickness. Line-tunneling and the use of $Si_{0.55}Ge_{0.45}$ enable steeper SS, which reaches down to 55 mV/decade at room temperature and higher current levels (up to 10 μA/μm). Furthermore, as the line-tunneling generation rate is proportional to the gate area, the drain current is proportional to WxLg (gate width and length, respectively).

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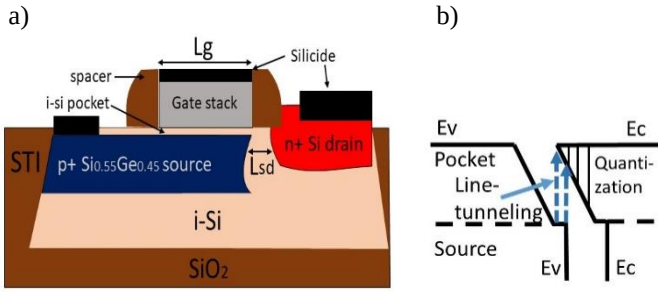

Fig.1 a) Line-TFET cross section, b) Band diagram along the vertical axis. Adapted from [2].

III. VARIATION OF DIMENSIONS AND POCKET DOPING

Using the TCAD tool Sentaurus by Synopsys, the Line-TFET was simulated using dynamic non-local path band-to-band tunneling model with the following parameters: A_{si}=1.5x10^{15} cm^{-3}; B_{si}=2.10^{7} V.cm^{-3}; A_{ge}=9.1x10^{16} cm^{-3}; B_{ge}=4.9x10^{16} V.cm^{-3}. TAT was not simulated as this work does not consider operation in the subthreshold regime. To account for the diffusion of boron from the source [2], 10^{19} cm^{-3} P-type doping in the pocket was used in simulations.

A. *Leakage tunneling*

The off-state current of the Line-TFET is highly dependent on the drain voltage due to source-to-drain tunneling [2]. Considering a device with the following dimensions: pocket thickness (tpocket) of 6nm, source-to-drain separation (Lsd) of 25 nm and Lg=1 µm, Fig. 2.a) depicts the Ids x Vgs transfer characteristics, separating electron and hole currents, for Vds=1.4 V. As Vgs increases and line tunneling becomes more significant, the main band-to-band tunneling mechanism plays a role and electron leakage current due to source-to-drain tunneling becomes less important. However, hole leakage current remains very dependent on Vds and varies between 5.10^{-12}A/µm and 7.10^{-9} A/µm for Vds from 1 V to 1.8 V. Fig. 2.b) shows its effect on the overall drain current, which greatly raises Ioff with Vds increase.

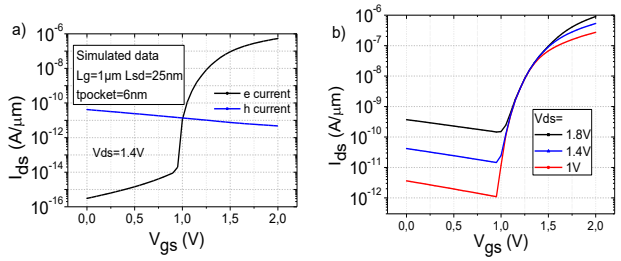

Fig.2 a) Electron and hole currents for Vds=1.4V b) total current for different Vds as a function of the gate voltage.

In order to further investigate leakage source-to-drain tunneling, Fig. 3 shows the electron tunneling generation rate between the source and the drain for Vds=1 V and 1.8 V (Vgs=2 V) while Fig.4 depicts the band diagram in this region for Vds=1 V; 1.4 V and 1.8 V (Vgs=1.8 V). Fig. 3 shows the presence of a point-TFET formed by the P-i-N junction at the edge of the source, controlled by the fringing electric field from the gate. However, as this is a short channel TFET (with channel length equal to Lsd), there is also direct tunneling to the drain, which is highly dependent on Vds due to the presence of Drain Induced Barrier Thinning (DIBT), as shown in Fig. 4 that exhibits the abrupt band bending in this region (similarly to what is discussed in [7]).

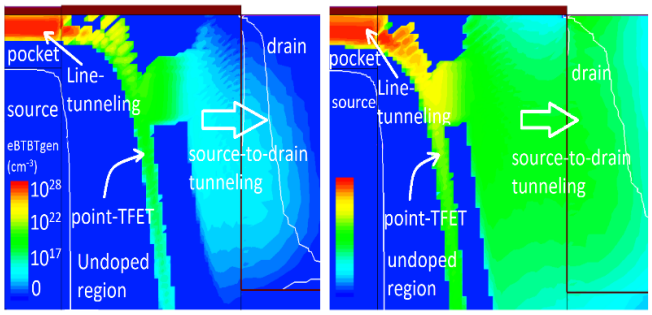

Fig.3 Electron tunneling generation rate at the source/drain separation region for Vgs=2V and a) Vds=1V; b) Vds=1.8V.

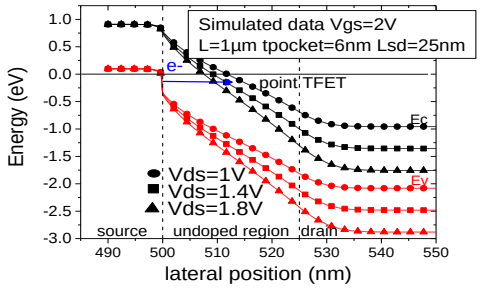

Fig.4 Band diagram from the source-to-drain separation region at 2nm below the pocket for Vgs=2V and different Vds.

B. *Variation of source-to-drain separation*

Varying the distance between source and drain (Lsd) affects not only leakage tunneling through DIBT but also the inner resistance of the device. Fig. 5.a) exhibits the drain current as a function of the gate voltage (Ids x Vgs) for Vds=1.8 V and Lsd=35 nm, separating hole and electron currents, while Fig. 5.b) shows the overall current for Lsd=25 nm, 35 nm and 45 nm.

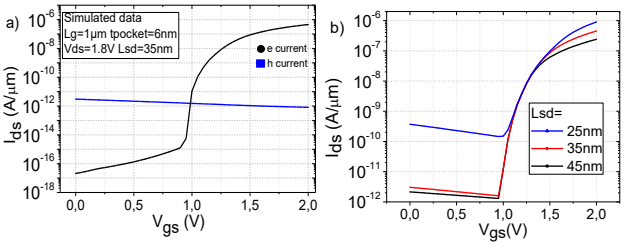

Fig.5 a) Electron and hole currents for source-to-drain separation of 25nm b) total current for different source-to-drain separations (25nm to 45nm).

The off-state electron current (Vgs<1 V) and hole current suggest that leakage tunneling is much more severe for Lsd=25 nm, which is about 6.10^{-9} A/µm while for Lsd=45 nm it is about 5.10^{-12} A/µm for Lsd=45nm. Figs. 6 and 7 depict the electron tunneling generation rate for Lsd=25 nm and 45 nm (Vgs=1.2 V and Vds=1.8 V) and the band diagram in the horizontal direction, respectively, of the P-i-N junction at the edge of the source. Even though DIBT is considerably reduced for Lsd=35 nm or higher, electron tunneling to the drain still happens for Lsd=45 nm.

Figure 8 exhibits the Ids x Vds transfer characteristics in the transition from the linear to the saturation-like region of

operation for Vgs=1.2 V and Lsd=25 nm, 35 nm and 45 nm. The saturation voltage raises rapidly with Lsd increase (about 200 mV for every 10 nm) while the current level in the linear region decreases because the inner resistance of the device increases as this is a high resistivity region.

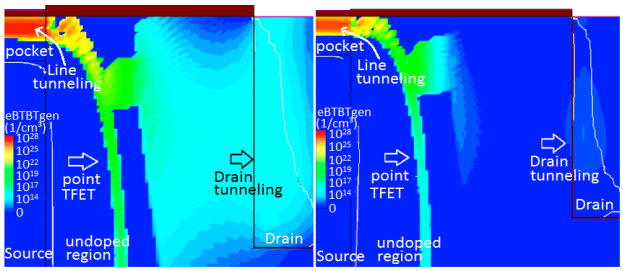

Fig.6 Electron tunneling generation rate for Vgs=2V, Vds=1.8V at the source/drain separations lengths of a) Lsd=25nm; b) Lsd=45nm

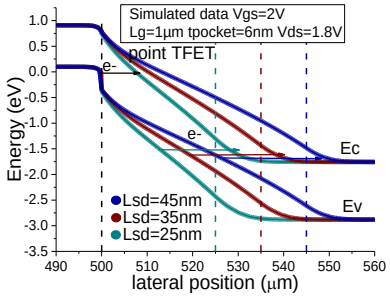

Fig.7 Band diagram between source and drain for different separation lengths (Lsd) for Vgs=1.2V and Vds=1.4V.

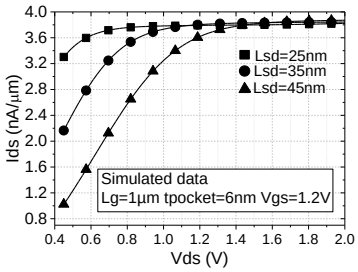

Fig.8 Drain current as a function of drain voltage for different source to drain separation lengths (Lsd) at Vgs=1.2V.

C. Output conductance and gate length

In [8], the authors propose that soft saturation is achieved in this device when the source is depleted of carriers due to Vds increase. The authors also discuss that deep saturation is achieved when the source-to-drain separation gets depleted of carriers. However, as discussed in the previous sections, leakage tunneling, which is highly dependent on Vds, takes place in this region, overlapping the deep saturation mechanism discussed in [8]. This causes at least three consequences for the output conductance (gd): 1) it reaches a minimum value (around $1.5x10^{-2}$ nS/µm and $3x10^{-2}$ nS/µm for Lg=100 nm and 1µm, respectively) and rises in deep saturation; 2) for sufficiently high Vds and low Vgs, gd rises exponentially, completely degrading the transfer characteristics [5] once leakage tunneling gets similar in magnitude to line-tunneling and 3) the average value of gd does not depend upon the gate length because leakage tunneling does not take place under the gate.

The key point is that, even if leakage tunneling is not intense enough to degrade the saturation characteristics of the device, this phenomenon is the main factor determining the average value of gd in saturation.

Figure 9 depicts the output conductance as a function of Vds for channel lengths varying from 100 nm to 1 µm (Lsd=35 nm). Once gd starts to rise for all devices with Vds increase (beyond Vds=1.8 V), the difference between them becomes negligible. Even though it is undesirable that gd rises with Vds, its value does not increase significantly for Lsd=35nm and Vgs=1.2 V (with Vds going from 1.5 V to 2 V, it goes from 0.015 nS to 0.033 nS for Lg=100 nm) and remains low.

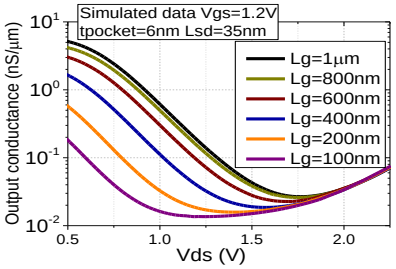

Fig.9 Output conductance as a function of drain voltage for different gate lengths.

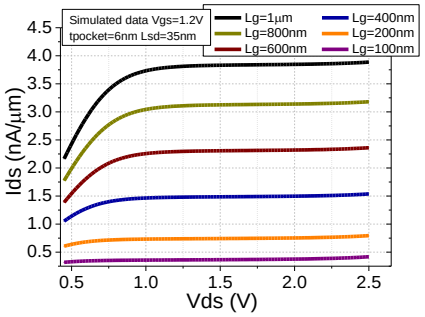

Fig.10 Drain current as a function of drain voltage with gate lengths from 100 nm to 1µm.

Figure 10 shows the Ids x Vds transfer characteristics for the same gate lengths of Fig. 9. The proportionality of the current with the gate length expected from Line-TFETs can be seen, revealing a different behavior from the output conductance.

Figure 11 shows the same trend for the output conductance for Lsd=25 nm, 35 nm and 45 nm (therefore, different leakage tunneling intensities), for Lg=100 nm and 1 µm. Even though gd rises less rapidly and steeply for greater values of Lsd, 100 nm and 1 µm devices always have the same output conductance for sufficiently high Vds.

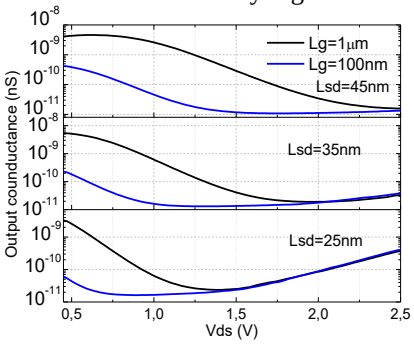

Fig.11 Output conductance as a function of drain voltage for different source/drain separations lengths and different Lg.

D. Variation of the pocket thickness

This section considers a P-type pocket doping of 10^{16} cm^{-3} in order to facilitate the comparison between devices with different pocket thicknesses. Such doping level reduces the thresh-

old voltage (Vth) [2] in order to visualize the transfer characteristics for different regimes of operation. Fig. 12 shows the electron current as function of the gate voltage (with hole current depicted in the inset) of devices with tpocket=4 nm, 6 nm and 8 nm (Lsd=25 nm). Reducing the pocket thickness increases gate coupling and the vertical electric field at the source, increasing the current level from $1x10^{-9}$ A/µm to $8x10^{-8}$ A/µm for Vgs=1.25 V and reducing SS. However, because of greater band bending and quantum confinement (QC, not considered in these simulations) in the pocket, Vth raises about 250 mV. Figure 13 depicts the output conductance as a function of Vds for those same values of pocket thickness. The current level and the saturation voltage are higher for smaller values of tpocket, but they eventually reach similar values for sufficiently high Vds. This is because leakage tunneling happens between the source and drain and is only affected by the pocket thickness through the fringing electric field from the gate. Understanding the behavior of gd with the pocket thickness is important in the analysis of experimental data to be accomplished in Section IV, since the pocket thickness significantly varies among devices [2].

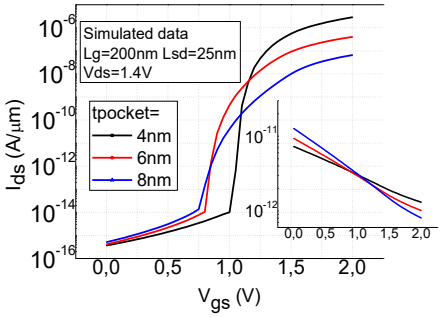

Fig.12 Electron drain current as a function of the gate voltage for different pocket thicknesses: 4nm, 6nm and 8nm (Lg=200nm). Inset: hole current.

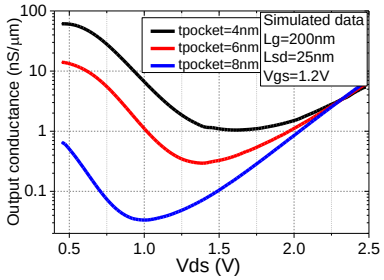

Fig.13 Output conductance as a function of drain voltage for different pocket thicknesses: 4nm, 6nm and 8nm. (Lg=200nm).

E. Pocket doping

Due to diffusion of boron from the source to the pocket, doping concentration in this region may reach values above $10^{19}cm^{-3}$, increasing the threshold voltage [2]. The doping profile in the pocket is considered uniform in the simulations, which is reasonable as the Gaussian distribution of dopants due to diffusion becomes approximately constant in small lengths, such as the pocket thickness. Figs. 14.a) and b) depict the Ids x Vgs transfer characteristics and the output conductance as a function of Vds for pocket dopings (pDop) of 10^{17}; 10^{18} and 10^{19} cm^{-3}. This device was simulated considering tpocket=4 nm, Lsd=21 nm and Lg=1 µm.

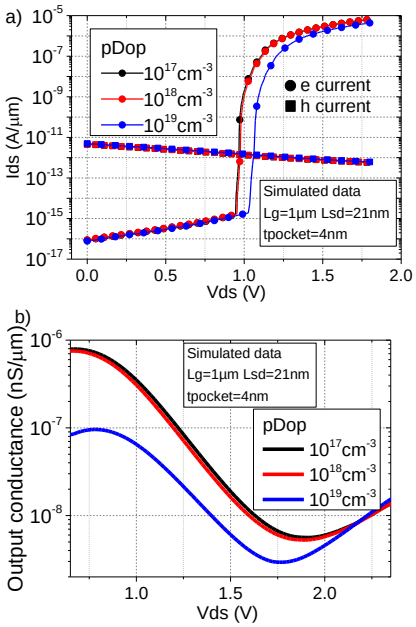

Fig.14 a) Drain current as a function of gate voltage and b) output conductance as a function of the drain voltage, for different pocket dopings (boron): 10^{17}, 10^{18} and $10^{19}cm^{-3}$ (Lg=1µm, Lsd=21nm and tpocket=4nm).

The threshold voltage shifts more abruptly for higher pocket doping levels because energy bands are less prone to cross with Vgs increase, presenting a shift of about 10 mV for pDop=10^{19} cm^{-3}. However, as shown by Fig.14.b), once the output conductance starts to rise for all devices, they all reach almost the same value because, once again, source-to-drain separation remains unaltered.

F. Gate-source misalignment

In [2], the authors discuss the effects of gate-source misalignment on the Ids x Vgs transfer characteristics. If the gate end extends beyond the source (positive misalignment), point tunneling at the edge of the source becomes stronger, possibly degrading the subthreshold slope, depending on the magnitude of TAT. If the source is extended beyond the gate (negative misalignment), the current level for higher Vgs drops due to the high Vth of the weakly gated region [2]. In order to evaluate its effect on the Ids x Vds transfer characteristics, which is important for analyzing the analog characteristics of the Line-TFET, a device with tpocket=4 nm, pDop=10^{17} cm^{-3}, Lsd=21 nm and Lg=1 µm is simulated with different gate-source misalignments. Fig. 15 depicts the gd x Vds transfer characteristics.

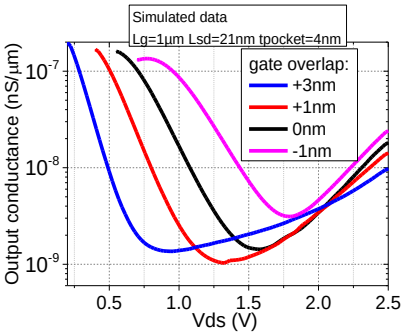

Fig.15 Output conductance as a function of the drain voltage, for different gate-source misalignments: -1nm (gate underlap), 0nm, +1nm (gate overlap) and +3nm (Lg=1µm, Lsd=21nm and tpocket=4nm).

Fig. 15 shows that positive misalignment improves the analog characteristics of the device by significantly reducing its saturation voltage (increasing Vgd_{sat}). This not only allows the operation with lower supply voltages but also delays the degradation of the saturation-like region due to source-to-drain tunneling, both allowing operation at lower gate voltages and improving the output swing.

IV. Experimental Verification

Fig. 16 depicts the experimental drain current (normalized by the gate area) as a function of Vds for devices with Lg=70 nm, 130 nm and 1 µm (Vgs=1.8 V). The normalized current is not the same for all devices due to process variation, especially in the pocket thickness and doping, and due to the increase in the inner resistance of devices with longer lengths [2]. The average output conductance has been assumed to be equal to the slope of the straight line that fits the saturation-like region. The difference between the gate and drain voltages when saturation is achieved (Vgd_{sat}) is above 1 V, suggesting a gate-source misalignment of about +3 nm.

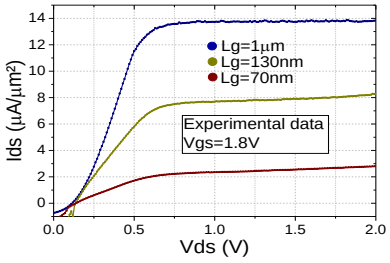

Fig.16 Experimental drain current as a function of drain voltage with gate lengths 70nm, 130nm and 1µm and Vgs=1.8V.

The authors in [2] estimate a source-to-drain separation of about 21nm, pocket thickness of about 6nm and body and source thickness of 45nm and 25nm, respectively, according to the transmission electron microscope (TEM) image and the strain profile of the device, which were used to match our simulations to the experimental data in the BTBT regime (Vgs ≥ 1 V). The average output conductance for Lg=70nm, 130 nm and 1 µm is 4.5 nS, 4 nS and 4.7 nS, respectively. This confirms that gd is not proportional to the gate length and that it is reasonable to assume gd to be constant with gate length variation.

V. Impact on Analog Circuit Design

A. Current mirrors and process variation

In order to evaluate the effect of process variation in a bias circuit, an elementary Widlar current mirror with 1:1 mirror rate is simulated considering three situations: different pocket thicknesses, different pocket doping and different gate-source alignment, which represent the main sources of device variation. All devices are biased with Vgs=1.2 V ±10 mV. The minimum and maximum loads that the circuit can sustain are defined as the voltages in which the output and reference currents differ in 10%. The simulations were performed in the Spectre circuit simulator by Cadence, with the TCAD simulation data inserted in Verilog-A lookup tables.

Fig. 17 depicts the result for a current mirror with devices presenting tpocket=4; 6 and 8 nm (Lg=200 nm, Lsd=25 nm and pDop=10^{16} cm^{-3}). Considering the extreme cases, Fig. 17 reveals a variation of 25 nA in the bias current and a variation of 300 mV in the minimum Vload for a variation of 4nm in the pocket thickness. Moreover, thicker pockets make the Line-TFET more prone to source-to-drain tunneling, in such a way that transistors with tpocket=6 nm and 8 nm present Vload maximum of 2.4 V and 1.86 V, respectively. This confirms that smaller pocket thicknesses greatly improve the output swing, even though it raises Vload minimum (and Vdsat) because of Vth increase.

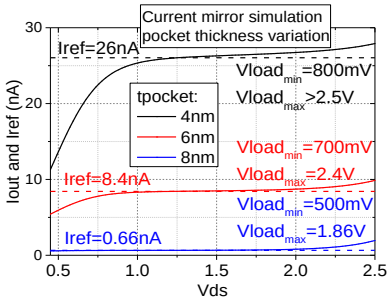

Fig.17 Current mirror simulation with variation of pocket thickness indicating Vload minimum and maximum, considering 10% tolerance of current mismatch.

Fig. 18 depicts the output characteristics of a current mirror considering pDop= 10^{17}, 10^{18} and 10^{19} cm^{-3} (Lg=1 µm, Lsd=21 nm and tpocket=4 nm). The threshold voltage shift results in a difference of 430 nA in the reference current comparing pDop=10^{17} and 10^{19} cm^{-3}, while pDop=10^{17} and 10^{18} cm^{-3} show a difference of only 36 nA (7%). Therefore, it is recommended to keep the thermal budget during the process after the fabrication of the pocket low enough to prevent source to pocket diffusion of boron greater than 10^{18} cm^{-3}. The negligible difference in Vload minimum can be explained as follows: as pDop and, consequently, Vth increases, the lower the inversion level of the transistors is for a given Vgs. Therefore, the saturation voltage reduces while increasing pDop. However, as seen in Fig. 13, this also causes gd to increase more sharply, in such a way that one effect compensates the other.

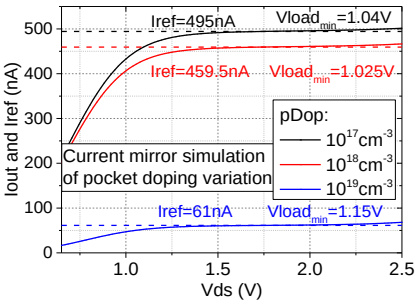

Fig.18 Current mirror simulation with variation of pocket doping indicating Vload minimum, considering 10% tolerance of current mismatch.

Fig.19 considers gate-source misalignments of -1, 0, +1 and +3 nm in both devices (pDop=10^{19} cm^{-3}, Lg=1 µm, Lsd=21 nm and tpocket=4 nm) and Iref=85 nm. By increasing the misalignment (that is, increasing gate overlap), the circuit's minimum output voltage decreases from 1.16 V to 300 mV, comparing the extreme cases, with negligible change in the reference current.

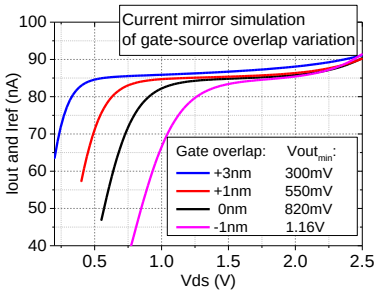

Fig.19 Current mirror simulation with variation of gate-source misalignment indicating Vload minimum, considering 10% tolerance of current mismatch.

B. Dependence of small-signal parameters with gate dimensions

The unique characteristics of Line-TFETs, in particular, the variation of electrical parameters with gate dimensions in this device, should change the way of performing the design. If the designer wishes to increase the gain, typically the channel lengths of conventional MOSFET devices must be increased in order to increase the output resistance. With Line-TFETs, the designer should also increase Lg, but for different reasons.

Table I summarizes the dependence of small-signal parameters with W and Lg for a single device, comparing MOSFET and Line-TFET technologies. As gd = Ids/V_A in saturation, where V_A is the Early voltage, the output conductance is roughly proportional to W/Lg² in MOSFET devices because of the current level, which scales it by W/Lg, and because V_A can be modeled as being approximately proportional to Lg due to channel length modulation. For Line-TFETs, only W affects this parameter as the parasitic phenomenon that defines the average gd takes place in a region that is not under the gate and thus doesn't depend upon Lg, which means that both the Early voltage and the current level increase with Lg. As pointed in [2], the unity gain frequency (ft) does not significantly depend upon Lg (if disregarding the increase in the inner resistance with Lg), because both gm and the parasitic capacitances (Cgg) increase with Lg and ft = gm/2πCgg. This means that the gain-unity gain frequency product (Av.ft, which evaluates the compromise between gain and frequency response on device parameters) increases with Lg in Line-TFETs, in contrast to MOSFETs in which it decreases with Lg. This represents a major advantage for Line-TFETs, because reducing the channel length is challenging and costly from the process perspective.

Table 1 Small signal parameters and their dependence on geometric design parameters comparing MOSFET and Line-TFET single devices.

	MOSFET	Line-TFET
Ids	∝ W/Lg	∝ W x Lg
gm	∝ W/Lg	∝ W x Lg
gd	∝ W/Lg²	∝ W
Av (gm/gd)	∝ Lg	∝ Lg
Cgg	∝ W.Lg	∝ W.Lg
ft (gm/2πCgg)	∝ 1/Lg²	constant
Av.ft	∝ 1/Lg	∝ Lg

C. Gate length variation: common source stage

The following procedures may be adopted by circuit designers in order to increase the gain when using Line-TFETs: (i) keeping gm and the current level constant, by decreasing W by the same factor Lg increases and consequently increasing gd; (ii) keeping W constant, increasing gm and the current level, with constant gd. To illustrate both scenarios, Table 2 compares the project of a common source stage with current source as load using 130nm MOSFET technology and Line-TFETs (Fig. 20), in which is desired to double the voltage gain from an initial situation. Win(load) and Lin(load) are the width and length of the input (load) transistor, I is the circuit current, Gm is the overall transconductance (equal to the transconductance of the input transistor) and Rout the output resistance of the circuit, equal to the parallel association of the output resistance of both transistors.

In the MOSFET design, the only interesting scenario is to keep the current level constant, which doubles Rout and keeps gm constant. The difference from this scenario to the constant W case is that the output resistance increases by a factor of 4, while degrading gm by a factor of 2, in the latter case. With Line-TFETs, it can be chosen whether to decrease gd, while keeping gm and the circuit area constant, or to double gm and keep gd constant in order to double the circuit voltage gain. Another interesting feature of Line-TFETs is that, when increasing Lg, ft remains constant if disregarding the increase in the inner resistance with Lg [2] and Av.ft raises, as with MOSFETs both decrease.

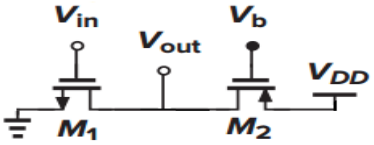

Fig.20 Common source stage with current source as load.

Table 2 Common source with current source load stage design example: device dimensions and parameters obtained.

Device	MOSFET			Line-TFET		
Situation	Initial	Const. I	Const. W	Initial	Const. I	Const. W
L_{in} (nm)	130	260	260	300	600	600
W_{in} (nm)	200	400	200	140	70	140
L_{load} (nm)	130	260	260	300	600	600
W_{load} (nm)	200	400	200	400	200	400
I (A)	15.5µ	15.5µ	7.75µ	66n	66n	132n
Gm (S)	110µ	110µ	55µ	400n	400n	800n
Rout (ohm)	125k	260k	550k	350M	700M	350M
Av (V/V; dB)	14; 23	28.6; 29	30.25; 30	140; 43	280; 49	280; 49

VI. CONCLUSION

The analysis of the relation between parasitic source-to-drain tunneling and the analog characteristics of Line-TFET devices (focusing on its impact on the Ids x Vds transfer characteristics), revealed that this phenomenon is the main responsible for defining the average output conductance. The consequences of this observation when varying different device parameters were addressed, showing that increasing

source-to-drain separation reduces source-to-drain tunneling, allowing operation at lower bias with smaller devices, but increasing their inner resistance, which shifts the drain saturation voltage up in about 400mV when increasing this parameter in 20nm. More importantly, it was demonstrated that the output conductance in this device does not descend asymptotically as previously thought, but instead starts to rise in deep saturation, resulting in an average value that is independent of the gate length. Moreover, varying the pocket thickness, which is an important source of device variation, was shown to not affect the output conductance significantly, even though the current level for Vgs=1.2 V suffers a 50-fold shift, allowing us to validate our results with experimental data.

The impact of pocket thickness variation, pocket doping, which shift the threshold voltage and changes the current levels, and of gate-source misalignment on current mirrors were also addressed. Gate-source misalignment proved to significantly shift the saturation voltage, which affects the minimum load that current mirrors can sustain (reducing it from 820 mV to 30 0mV comparing the self-aligned and 3nm gate overlap cases), improving the analog characteristics when the gate overlaps the source. Pocket doping of 10^{19} cm^{-3} increases the threshold voltage in about 10 mV, causing a 50-fold reduction in the drain current and negligibly affecting $Vload_{min}$. Reducing the pocket thickness from 8nm to 4nm causes a 40-fold increase in the current level and a reduction of 300 mV in $Vload_{min}$. Furthermore, the variation of different small-signal parameters with gate dimensions was summarized and their impact on analog design was studied through a common source stage example. It revealed that the designer may choose whether to increase Gm and the circuit area or to increase Rout while keeping the circuit area the same to increase the overall voltage gain.

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