Analysis of omega-gate nanowire SOI MOSFET under analog point of view

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***Abstract*—This paper presents an evaluation of omega-gate nanowire n- and p-type SOI MOSFETs performance focusing on the main analog figures of merit, like saturation transconductance (gm_{sat}), output conductance (g_D), transconductance over drain current (gm/I_{DS}) ratio, Early voltage (V_{EA}), intrinsic gain (A_V) and unit gain frequency (f_t). The different channel widths (W_{NW}) and channel lengths (L) were also evaluated. These devices presented values of subthreshold slope near the theoretical limit at room temperature (60 mV/dec), and in the worst case, a DIBL value smaller than 70 mV/V. Showing its immunity to short channel effects (SCEs) in the studied channel length range. The narrowest device showed great electrostatic coupling, improving gm, presenting an unit gain frequency over 200 GHz and intrinsic voltage gain over 80 dB. These values suggests that this device is capable of achieving good performance on new applications such as 5G communications and Internet-of-Things (IoT).**

***Index Terms*— SOI MOSFET; Omega-gate; Nanowire; Unit-gain Frequency; Intrinsic Voltage Gain.**

I. Introduction

After the advent of Silicon-On-Insulator technology, the study of new transistor geometry was necessary in order to improve the gate control over channel charges. The ideal geometry is the gate all around (GAA), and going in this direction, the omega-gate SOI transistor reduces the complexity of the fabrication process while ensuring a great electrostatic gate control [1-4].

The nanowire is an important technology to be studied as it is one possible technology to continue the MOSFET roadmap. This technology showed promising results in digital application, transport characteristics and analog performance [2, 5-8]. It also shows applicability in 5G communications and Internet-of-Things (IoT) [9].

The digital parameters of the omega-gate nanowire MOSFET have been thoroughly studied [10, 11], and this work evaluates the analog performance of the device focusing on intrinsic voltage gain and unit-gain frequency, and the influence of the devices dimensions on these parameters.

This work is an extended version of [12].

II. Device Characteristics

The studied devices were fabricated at CEA-LETI on a SOI substrate with a buried oxide thickness of 145 nm. The omega-gate nanowire SOI MOSFET dimensions are, 10 nm of fin height (H_{NW}), 220 nm and 10 nm of fin width (W_{NW}), and channel length ranging from 50 nm to 10 µm, with 1 fin and 50 fins. A scanning electron microscopy (SEM) and a cross-sectional transmission electron microscopy (TEM) images of omega-gate nanowire SOI MOSFET are presented in Fig. 1.

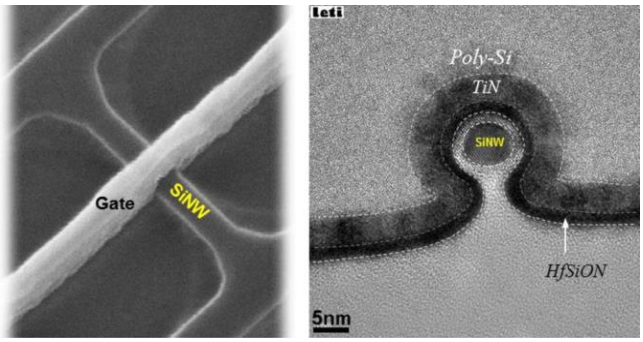

Fig. 1. SEM (left) and TEM (right) images of omega-gate nanowire SOI MOSFET [1].

III. Methodology

The measurements were performed with a drain voltage (V_{DS}) of 800 mV for saturation region and 50 mV for linear region, and gate voltage (V_{GS}) range from - 0.5 V to 1.2 V for the nMOS, and -1.5 V to 0.5 V for the pMOS, using the parameters analyzer B1500 (Keysight).

To measure the capacitance, a sinusoidal signal was applied between gate and drain/source (short-circuited), with an amplitude of 100 mV, 100 kHz of frequency and bias level ranging from -1.2 V to 1.2 V for nMOS and -1.5 V to 1.5 V for pMOS, using the LCR meter E4980A (Keysight). In addition, to have a more reliable capacitance measurement, the devices with channel length of 10 µm, channel width of 10 nm and 220nm, with 50 fins were analyzed.

Some of the analysis required normalization by the devices dimensions, but the devices have a cylindrical geometry, so some calculations were necessary in order to find the effective channel width (W_{eff}). In Fig. 2, the device with W_{NW} of 10 nm is presented.

Considering a circular geometry ($W_{NW} = H_{NW} = 10$ nm), the device has a radius of 5 nm, so, the effective transistor width is the perimeter minus the bottom part of the channel, which does not have a gate stack ($W_{eff} = 2.\pi.5 - 5nm = 26.42$ nm).

Considering that all devices have the same H_{NW}, in order to obtain the effective channel width for other W_{NW}, a generic equation is defined.

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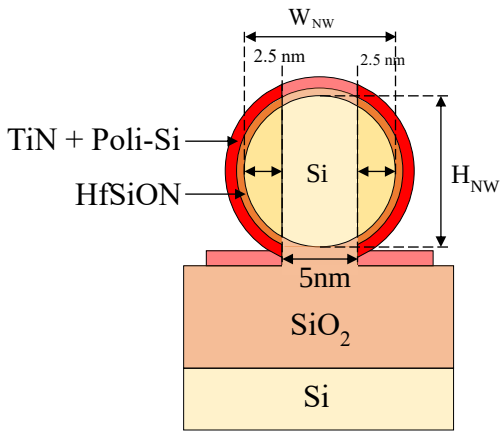

Fig. 2. Omega-gate nanowire SOI MOSFET cross section, with highlighted side gates.

Starting from the W_{eff} of the device with W_{NW} = 10 nm, the lateral length can be calculated by subtracting the superior part of the gate (rounded to 5 nm) from W_{eff} = 26.42 nm, resulting in the value of 21.42 nm, which is represented by the highlighted areas of Fig. 2. The side gates are considered the same for any channel width, as shown in Fig. 3.

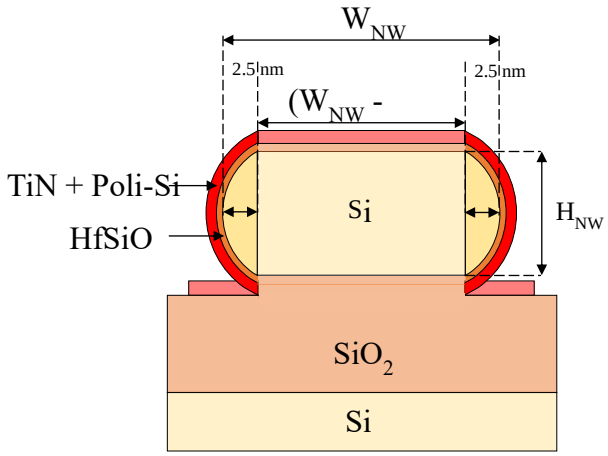

Fig. 3. Omega-gate nanowire SOI MOSFET cross section, with highlighted side gates.

To sum up, by adding the lateral length (21.42 nm) with the top gate (W_{NW} - 5 nm), W_{eff} is defined as it follows in (1):

$$W_{eff} = 16.42 + W_{NW} \quad (1)$$

With all values in nanometers.

IV. Results and Discussion

A. Short Channel Effect

Fig.4 and Fig.5 presents the threshold voltage as a function of channel length of omega-gate nanowire MOSFET for n-channel and p-channel, respectively. It is possible to notice that for narrow devices the threshold voltage value is kept almost constant for L > 50 nm for n-channel devices and for L>100nm for p-channel ones. The V_{TH} reduction observed for short and wide devices is explained by the short channel effect (SCE). P-channel devices with L<100 nm for all W_{NW} start to suffer of SCE.

It is also possible to notice that the threshold voltage decreases as the fin width increases even for long channel devices. A possible explanation to this behavior is the presence of a density of charges in the oxide due to fabrication process, which reduces the threshold voltage. Another possible explanation is the surface potential dependence on W_{NW} [13]. The devices starts to suffer from SCE for L < 1000 nm for n-type. For the narrower device (W_{NW} = 10 nm), the V_{TH} is not affected for L>50nm because of this dimension, a strong electrostatic coupling shields the device from the effects of the density of charges.

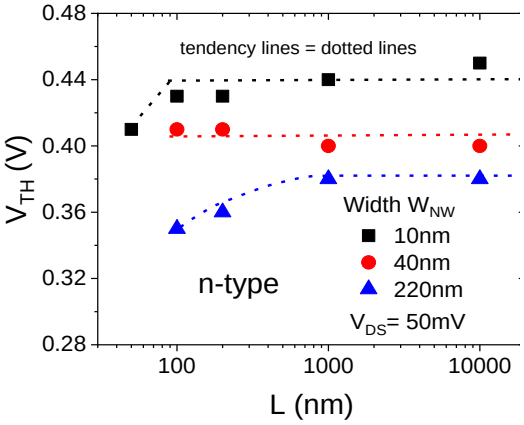

Fig. 4. Threshold voltage as a function of channel length for different channel width of an n-type omega-gate nanowire SOI MOSFET.

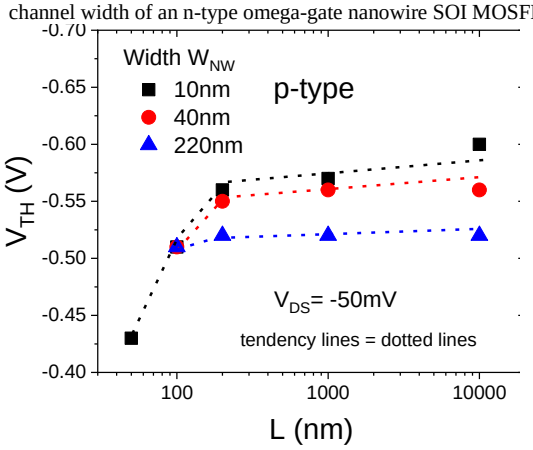

Fig. 5. Threshold voltage as a function of channel length for different channel width of a p-type omega-gate nanowire SOI MOSFET.

Even though the V_{TH} behavior analysis showed that narrow devices are almost immune to SCEs till L=100nm, it is known that the subthreshold slope (SS) is also sensible to the occurrence of SCEs. The SS evaluation, as function of channel length, is presented in Fig. 6 and Fig. 7.

It is notable that all values are near the theoretical limit of MOS technology, which is 60 mV/dec at room temperature. Although all the SS values are small, the SCE starts for the narrowest device (W_{NW} = 10 nm) with channel length of 50 nm, while for the largest devices (W_{NW} = 220 nm) already presents the SCE for L = 100nm.

The DIBL was extracted by the formula

$$DIBL = |V_{TH\,Tri} - V_{TH\,Sat}| / |V_{DS\,Tri} - V_{DS\,Sat}| \quad (2)$$

Where $V_{TH\ Tri}$ is the threshold voltage in triode region, $V_{TH\ Sat}$ is the voltage in saturation region with the same drain current at $V_{TH\ Tri}$ in triode region, $V_{DS\ Tri}$ is the drain voltage bias at triode region, and $V_{DS\ Sat}$ is the drain voltage bias at saturation region.

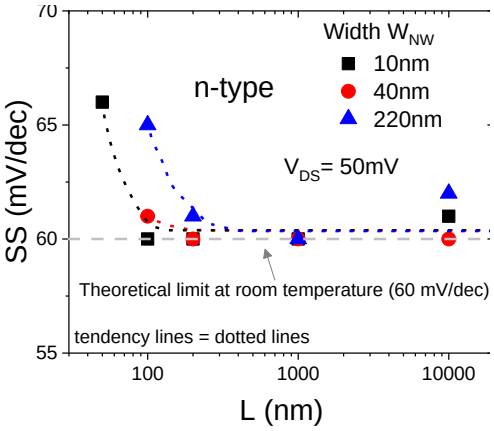

Fig. 6. Subthreshold Slope as a function of channel length for different channel width of an n-type omega-gate nanowire SOI MOSFET.

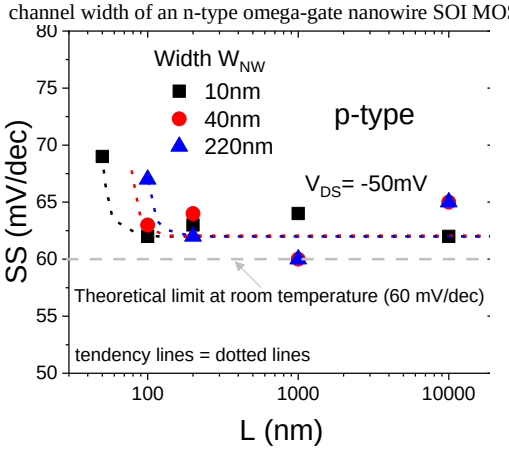

Fig. 7. Subthreshold Slope as a function of channel length for different channel width of a p-type omega-gate nanowire SOI MOSFET.

Fig.8 presents the curve of Drain Induced Barrier Lowering (DIBL) versus channel length for an n-type nanowire SOI MOSFET with fin width of 10 nm, 40 nm and 220 nm. It is possible to notice, that for long devices ($L \geq 1000$nm), the threshold voltage is not affected by the high drain electric field. For the narrowest devices ($W_{NW} \leq 40$ nm) this behavior starts to be degraded for channel length ≤ 100 nm, but for the largest devices, the lack of electrostatic coupling results in a stronger influence of drain voltage on V_{TH}, causing early DIBL increase, hence lowering the transistor performance.

The same device characteristics were analyzed in Fig. 9 but for a p-type omega-gate SOI MOSFETs. It is possible to realize that for larger devices ($W_{NW} \geq 40$ nm), DIBL starts a little bit higher for the longest devices (L = 10 µm) and it increases as the device gets shorter, as well as for the n-type ones.

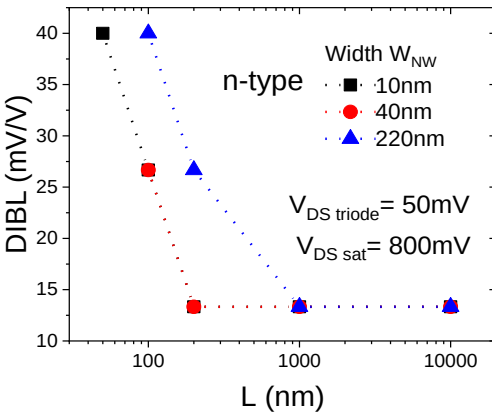

Fig. 8. DIBL as a function of channel length for different channel width of an n-type omega-gate nanowire SOI MOSFET.

These devices achieved, in a worst case, a DIBL around 65 mV/V, while a FinFET , with 65 nm of height, 130 nm of width, and channel length of 130 nm ,achieves around 180 mV/V [14].

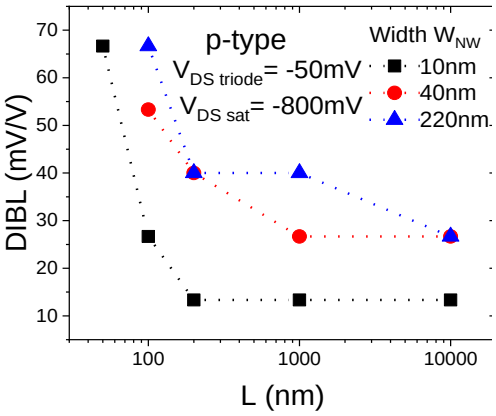

Fig. 9. DIBL as a function of channel length for different channel width of a p-type omega-gate nanowire SOI MOSFET.

B. Analog figures of merit

The equation used to calculate intrinsic voltage gain (A_V) is defined by (3):

$$|A_{V|} = gm/g_D \quad (3)$$

And unit-gain frequency (f_t) is defined by (4):

$$f_t = gm / 2\pi C_{gg} \quad (4)$$

Where C_{gg} is the gate capacitance. Considering saturation region for analog operation, the transistors capacitance can be assumed to be $C_{gg} \cong C_{gs} \cong 2/3C_{max}$ [15], then (4) becomes (5):

$$f_t = gm / (4\pi C_{max} / 3) \quad (5)$$

Where C_{max} is the maximum device capacitance.

As show in (3), one way to calculate the intrinsic gain, is to divide the transconductance (gm) over output conductance (g_D), so the behavior of those parameters are very important to consider. Both, gm and g_D, are normalized by the transistors dimensions (W_{NW}, L and fin number).

In Fig. 10 and Fig. 11, the normalized transconductance and output conductance, respectively, of omega-gate nanowire SOI MOSFET are presented as a function of channel length for both n-type and p–type,. It is possible to note that for increasing W_{NW} the transconductance gets lower and the output conductance gets higher, which happens because of the loss of electrostatic coupling as the lateral gates become more distant from the channel.

The transconductance is similar for all channel lengths, except for L=50 nm in the n-type transistor and L ≤ 100 nm for the p-type, which suffers from SCEs as noted before and also due to the higher impact of series resistance. This behavior was observed for both types of transistors.

However, the output conductance increases for lower channel lengths because of the higher influence of channel length modulation over short channels.

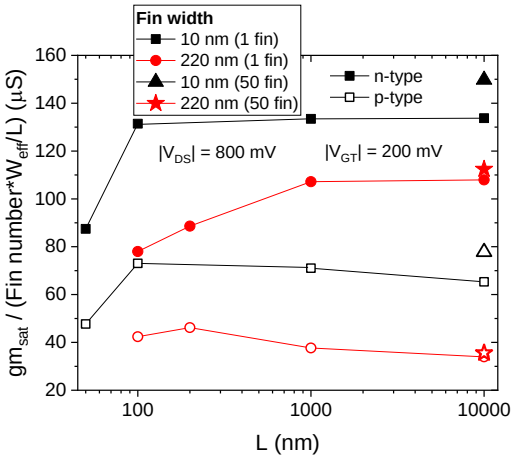

Fig. 10. Normalized transconductance as a function of channel length for devices with fin width of 10 nm and 220 nm, 1 fin and 50fins, of n- and p-type omega-gate nanowire.

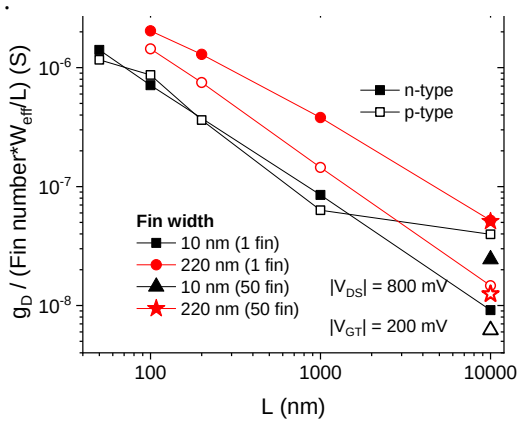

Fig. 11. Normalized output conductance as a function of channel length for devices with fin width of 10 nm and 220 nm, 1 fin and 50fins, of n- and p-type omega-gate nanowire.

In order to calculate the unit gain frequency, the maximum capacitance is needed, as showed in equation (5). Fig. 12 shows the devices capacitance and current as a function of gate voltage. With the increase of gate voltage, the device goes from accumulation (V_{GS} < 0.2 V) to depletion (0.2 V<V_{GS}<0.6), and then it reaches inversion, which gives the maximum capacitance. However, the capacitance does not reach a plateau because the gate current begin to increase and further degrade the device, as it is possible to see I_D and $|I_S|$ splitting. From the capacitance curve (dashed line), it was possible to obtain a C_{OX} = 3.7 µF/cm^2, dividing the capacitance, at V_{GS}= 1.2 V for n-type or at V_{GS}= -1.5 V for p-type, by the devices dimensions and number of fins.

Fig. 13 presents a similar curve as Fig. 12, but for the p-type device. This curve has a higher gate voltage range due to higher threshold voltage (considering absolute values) for the p-type devices. Even at high V_{GS} values, the capacitance does not suffer degradation due to gate leakage current, which is almost 2 orders of magnitude lower than I_{DS}.

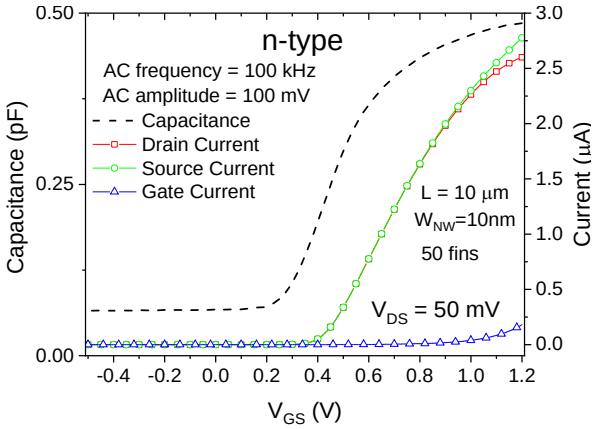

Fig. 12. Capacitance and current as a function of gate voltage, for a device with fin width of 10 nm and 50 fins, of a n-type omega-gate nanowire SOI MOSFET.

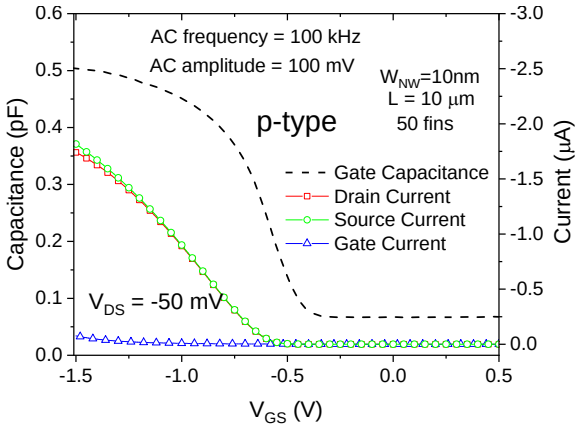

Fig. 13. Capacitance and current as a function of gate voltage, for a device with fin width of 10 nm and 50 fins, of a p-type omega-gate nanowire SOI MOSFET.

In Fig. 14, the gm/I_{DS} ratio is presented as a function of normalized drain current. Because the device with W_{NW} = 10 nm has a greater electrostatic coupling, its values are higher than the W_{NW} = 220 nm one. As the current increase, the device starts at weak inversion where the values of gm/I_{DS} are inversely proportional to the SS (which has a dependence on the transistor body factor) [16], which is around 60 mV/dec at room temperature. When it goes to moderate inversion, the gm/I_{DS} depends both on SS and mobility degradation, and finally, at strong inversion the device has a strong dependence on mobility degradation and series resistance. However, narrow devices have higher series resistance, so the difference between the two curves is reduced.

The Early voltage, presented at table I, gets higher for long channels because of the channel length modulation effect, similarly occurs to output conductance. The p-type device presented higher values than n-type.

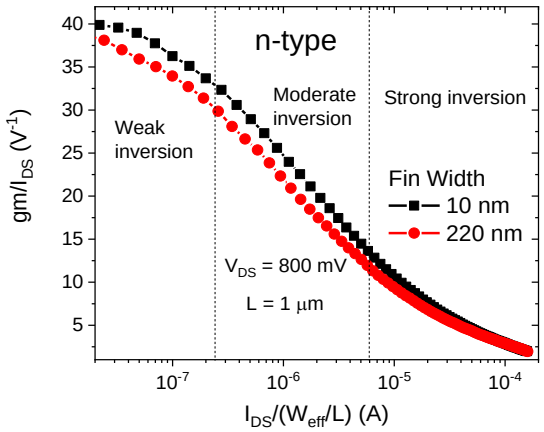

Fig. 14. gm/I_{DS} ratio as a function of normalized drain current of a n-type omega-gate nanowire MOSFET for different channel widths.

Table I: Early Voltage

L (nm)	W_{NW} (nm)			
	10		220	
	N-type	P-type	N-type	P-type
50	6.9	4.74	-	-
100	18.55	10.48	4.6	3.38
200	18.85	31.37	7.72	7.14
1000	84.37	217.64	30.79	30.98
10000	447.45	1801.32	247.03	307.13
10000 (50 fins)	912.29	3570.71	260.67	290.39

Intrinsic voltage gain and unit-gain frequency as a function of channel length are shown in Fig.15 and Fig. 16, respectively. In order to calculate f_t for devices with 1 fin, the gate capacitance was obtained through the multiplication of C_{OX} ($3.7\mu F/cm^2$) with the devices dimensions.

The A_V increases as L increases too. That happens because this parameter depends on gm_{sat}/gd, and short channel devices are more affected by channel length modulation and loss of electrostatic control (through SCEs). The longest channel device achieved more than 80 dB, while a FinFET, with 65 nm of height, 130 nm of width, and channel length of 130 nm, achieves around 60 dB [17].

However, the f_t has the opposite behavior of A_V. The f_t decreases as L increases because it is proportional to gm/C_{gg} (which gm is proportional to W_{eff}/L and C_{gg} to W_{eff}*L), so in the end it depends on $1/L^2$. Although, there is a difference between the curves, it is because of the greater electrostatic coupling of the narrow device (W_{NW} = 10 nm). The devices showed values over 100 GHz, while other MOSFET technologies, like FinFETs, presents values lower than 100 GHz [17].

The p-type transistor behaves similarly as the n-type. Even though this device presents lower values than the n-type, it shows an f_t over 100 GHz and A_V over 70 dB.

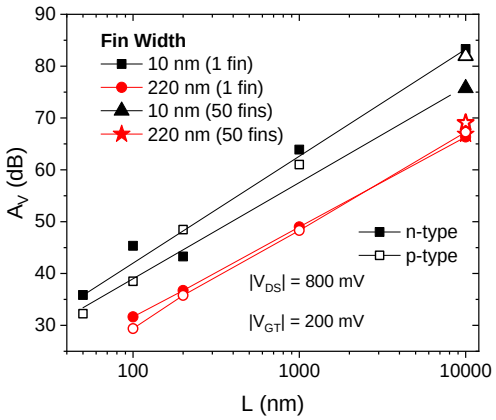

Fig. 15. Intrinsic voltage gain as function of channel length for an n- and p-type omega-gate nanowire SOI MOSFET with 10 nm and 220 nm of W_{NW}.

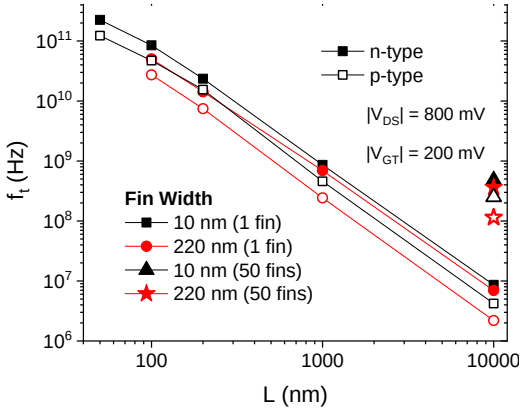

Fig. 16. Unit-gain frequency as function of channel length for an n- and p-type omega-gate nanowire SOI MOSFET with 10 nm and 220 nm of W_{NW}.

V. CONCLUSION

In this work some basic parameters were analyzed for different dimensions (W_{NW} and L) of n- and p-type nanowire omega-gate SOI MOSFET. These devices presented great immunity to the SCEs for $L \geq 50$ nm, where SS were around 60 mV/dec (theoretical limit at room temperature) and very low DIBL (less than 70 mV/V). While having in mind that the W_{NW} plays a major role on these devices, as it is related to the electrostatic coupling between channel and gate.

This paper also evaluated the analog applicability of the nanowire SOI MOSFET, based on A_V and f_t, and for the latter, the experimental gate capacitance (C_{gg}) was extracted.

The narrowest device (W_{NW} = 10 nm) shows better electrostatic coupling between gate and channel. The shortest device presents an f_t over 200 GHz, and the longest presents an A_V near 80 dB, which suggests that these devices are very well suited for high frequency or high gain analog applications, such as 5G communications.

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