A Comparative Analysis of Electrical Behavior and Soft Error Impact on XOR Logic Gates in Nanotechnologies

Rafael N. M. Oliveira[1] and Cristina Meinhardt[1,2]

[1] Department of Computer Science and Statistics, PPGCC, Federal University of Santa Catarina, Florianpolis, Brazil
[2] Computer Science Center, PPGComp, Federal University of Rio Grande, Rio Grande, Brazil
e-mail: rafaelnmo@grad.ufsc.br, cristina.meinhardt@ufsc.br

***Abstract*— With the advance of computer systems, XOR gates design became essential to the arithmetic circuits. At nanometer nodes, despite the electrical characterization, designers must consider soft error impact on the circuits. The challenges change significantly as feature sizes are smaller, even for FinFET devices. The effects of Single Event Transient are dependent on the circuit topology. Thus, in this work, we evaluate the soft error susceptibility on nine XOR topologies, discussing the influence of logic family, the device technology and environment factors as temperature, on the radiation robustness. Also, this work explores the nominal and near-threshold operation of these XOR topologies. Results show that FinFET devices are significantly more robust to the radiation effects. Also, most PTL logic XORs topologies present about 40% of the increase on the LET threshold. The dependence of temperature aggressively impacts the FinFET technology devices operating at near-threshold. Finally, the complete set of information provided in this work supports designers in choosing the most appropriate XOR topology according to the specific design requirements.**

***Index Terms*— XOR topologies; complementary CMOS; PTL; FinFET; LET; radiation effects.**

I. Introduction

MOSFET devices have reached the physical limits for technology nodes sub-22nm, and the technology scaling has introduced new challenges in circuit design due to the tiny dimensions and process variability. Since 2012, the semiconductor industry has widely use FinFET devices and, nowadays, a set of discussion has been established in order to point the future for the nanotechnologies. Besides the dimension shrinking, the supply voltage is reduced to meet the design requirements, reducing the consumption of dynamic power and static power. In nanotechnologies, there is an increase of leakage currents featuring an increase in static consumption of logic gates [1]. From a design standpoint, these challenges require an accurate estimate of process variability impact and Soft Error (SE) susceptibility, new methodologies to attenuate the effects caused by them and Electronic Design Automation (EDA) tools to cope with the constraints imposed by FinFET technology nodes [2].

Furthermore, the scaling process has a direct and negative impact on reliability [3]. At each new technology node, there is a significant increase in the number of possible transient faults, reflecting high device failure rates and low yield [4]. Moreover, advances in microelectronics have led to the scale down of technology and reduction in the threshold voltage and the increase in operating frequencies. However, it causes an increase in the circuit's susceptibility relative to the noise from the environment, particularly to the effects of the bombardment of particles of radiation [5]. Even particles with low energy found on the Earth's surface, previously overlooked, are now able to interfere within the operation of the circuits [6], provoking soft errors. Thus, one of the biggest challenges in the semiconductor industry is to ensure the reliability of circuits due to ionizing particles' interaction in silicon.

For a long time, soft errors affecting combinational circuits, mainly the Single Event Transient (SET) kind of faults, were considered irrelevant due to the combinational cells' intrinsic capacity to mask their effect. However, at nanometer nodes, the effects of masking have been reduced, increasing the need to study and develop SET mitigation techniques [7]. The challenges and solutions change significantly as feature sizes become small, then, soft errors produced by ionizing radiation pose significant challenges for integrated circuits and electronic devices [8].

The radiation effects are also more aggressive for circuits operating at Near-Threshold Voltage (NTV). The increasing demand for portable computation, mobile sensor networks, and other Internet of Things (IoT) devices makes low power devices a vital industry sector. One of the most applicable methods to reduce the power consumption of circuits is voltage scaling. However, low voltage operation reduces the circuits' performance and increases the sensibility of the devices to noise sources, as provoked by ionized particles. In this context, designers must consider radiation effects on designs, mainly on memories and arithmetic modules.

Complex arithmetic circuits are an essential part of computer systems demanded by practically all the instructions available in an architecture's instruction set. A set of logic gates composes these circuits. One of these cells is the exclusive-OR (XOR), presented in adders, multipliers, muxes, and comparators, for example. Due to its broad application, the electrical characteristics of XOR logic gates are essential because they should significantly affect these systems' performance.

This work evaluates and compares a set of XOR topologies using CMOS Logic and PTL, implemented with 16nm CMOS and FinFET technology. The SET effects have been investigated for XOR gates [9, 10, 11, 12]. Radiation hardening techniques for XOR-based circuits are presented in few works, but this highlight the relevance of known the SET sensibility of the XOR gates to best design decisions [13, 14, 15, 16]. However, there is a lack of works evaluating different XOR topologies considering radiation robust-

Digital Object Identifier 10.29292/jics.v15i2.131

ness operating at NTV and different ranges of temperature. The main contributions of this work are:

1. Evaluating the influence of the logic family on the radiation robustness.
2. Investigating the impacts of the near-threshold voltage operation on XORs regarding electrical characteristics and soft errors.
3. Analyzing the effects of temperature regarding soft errors.
4. Providing a complete set of information about the electrical behavior of XOR gates under soft error effects to help designers to choose the most appropriate XOR topology for different design requirements.

The remaining of this paper is organized as follows. In the Section II are presented the main differences between CMOS and FinFET devices and the nanometer scale influences. Section III introduces the selected set of XOR topologies investigate in this work. Section IV details the methodology adopted. Section V presents the results for delay, power consumption and the relation between power and delay provided by the figure of merit of the Power-Delay-Product (PDP). Section VI discuss the results for the radiation robustness analysis and section VII presents the main results for the temperature influence in the robustness. Finally, Section VIII presents the conclusions of this work.

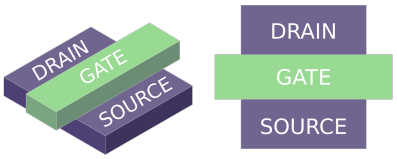
II. Background

The MOSFET devices have allowed continuous technology scaling over the last decades. The main property of these devices is that, depending on the signal applied to the transistor's gate, a conductive path can be formed between the source and drain terminals. However, when the technology reached the nanometer scale, the bulk CMOS technology became even more sensitive to the Short Channel Effects (SCE), mainly due to the high channel doping, mobility degradation. The evolution follows in the search for new devices, and in the last years, Silicon-on-Isolator (SOI) CMOS devices and multigate devices have been explored to the industrial manufacturing, killing evolutionary step.

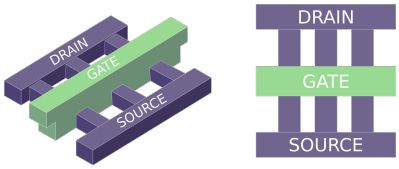
FinFETs are a type of multigate device, where the fin-like geometry ensures that depletion regions reach the gates entirely into the body region. A comparison between the MOSFET and FinFET structures can be seen in Fig. 1. The key geometric parameters for a FinFET are the Gate Length (LG), the fin height (H_FIN), fin thickness (T_FIN) or W_FIN), and oxide thickness (T_OX) [17]. This fin structure implies the absence of free charge carriers, making the suppression of SCE possible [18].

FinFET manufacture presents low-cost wafers, low defect density, less back gate-bias effect, better immunity to heat transfer problems, and low Bias-Temperature Instability (BTI) stress [19]. FinFET devices can be built on bulk or SOI technology, as represented in Fig. 2, similar to the NMOS and PMOS technology processes. In bulk FinFETs, all fins share a common silicon substrate, and an oxide provides the insulation between adjacent fins [20]. The SOI FinFET has a thin layer of oxide (SiO2), and the devices are built on the top of this buried oxide.

FinFET devices presented a new challenge on the traditional transistor sizing. The fin structure restricted the sizing to a quantization problem, where fin replicas are connected in parallel to enhance the signal drivability, differently of bulk CMOS devices that the sizing is continuous, However, due to the fin structure, the NFET and PFET devices with one fin have driving force and conductivity equivalence for a large NMOS/PMOS device.

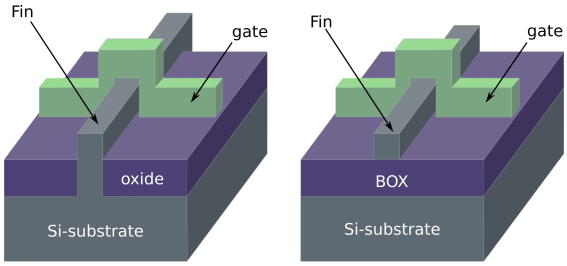


(a) MOSFET.



(b) FinFET.

Fig. 1 MOSFET and FinFET devices.



(a) Bulk FinFET. (b) SOI FinFET.

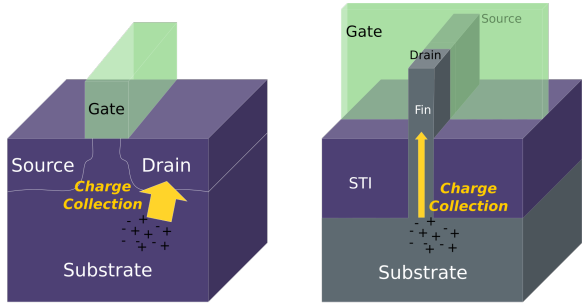
Fig. 2 FinFET devices.

Predictive models are essential in integrated circuit designs to identify design requirements, explore challenges and possible solutions during the evolution of the technology [2]. Predictive models are developed considering previous results and industrial data. Multigate devices were modeled through 3D simulation tools to predict the devices behaviour previously of the manufacture information be widely released. The provided electrical models for SPICE simulations require shorter computational time compared to 3D models, providing an alternative to aid circuit designers [21]. The most widespread models for FinFET technology are the Predictive Technology Model for MultiGate devices (PTM-MG) [2] and the 7-nm FinFET ASAP design kit (PDK) [22].

The PTM-MG model was chosen because it is freely available for academic use and to make possible a predictive comparison between the bulk CMOS and FinFET technologies.

A. Radiation Effects on Devices

The soft errors result from a transient pulse generated by the interaction of energetic particles near a sensitive region of a transistor when the collected charge (Qcoll) exceeds the



(a) CMOS charge collection. (b) FinFET charge collection.

Fig. 3 Charge collection method [23].

critical charge (Qcrit). According to the energy of the ionized particles hitting the silicon and the angular incidences on charge collection, transient pulses can cause perturbations and even critical system behavior failures. Despite there being other models more complex that consider sub 22nm technologies characteristics, this work presents a comparative analysis of radiation effects and adopted the Messenger model [24]. By adopting a comparative rather than quantitative analysis, the model's possible inaccuracies are less significant, allowing abstracting specific details of each technology, especially considering the comparison between predictive technologies.

The collision of energetic particles causes a strong electric field perturbation due to the direct ionization, a primary mechanism of charge deposition caused by the incidence of alpha particles or heavy ions. As an energetic particle hits in the silicon, it loses energy and forms a track of electron-hole pairs. If the ionization track transverses the depletion region, the electric field collects the carries generating a transient current pulse at the node. The charge generated by particles' impact varies depending on the ion type, incident angle, and impact site.

The disturbance caused due to the impact of energetic particles depend on energy lost in the track length is known as Linear Energy Transfer (LET). For every 3.6 electron volts (eV) of energy loss by the particle, one electron-hole pair is created in the silicon substrate. The LET depends on the particle's mass/energy and the material in which it is traveling. The highest LET values are obtained when more massive and energetic particles impact denser materials. In this way, the pulse width is dependent on the particle energy, the charge stored at a node, and the charge collection in the affected junction. After the silicon particle ionization, the process of charge collection proceeds through two mechanisms: drift and diffusion [25]. When the resultant ionization track traverses the depletion region, carriers are rapidly collected by the high electric field. This charge collection is known as drift. The crossing of particles through the depletion region is responsible for temporary deformation in a funnel shape. This effect is called funneling, causing an increase in the collected charge efficiency due to the increase of the depletion region area. Finally, the diffusion process collects all the other carries generated besides the depletion layer. The funnel creation and drift mechanisms are high-speed processes. They are responsible for controlling the almost instantaneous rise of the transient current due to the deformation of the junction's electric field. In the diffusion mechanism, a longer time is needed to collect the charge and, then, the transient pulse has a slower fall time.

The charge deposition mechanism proposed in [24] is widely used to form a current source whose behavior is modeled as a double exponential. In bulk silicon, a typical charge collection depth for a heavy-ion is approximately 2μm. For every $1(MeVcm^2/mg)$, an ionizing particle deposit about 10.8fC of electron-hole pairs along each micron of its track. For sub-22nm nanometer technologies, especially for LETs higher than 10 MeV, the typical transient current waveform tends to suffer some modifications presenting a behavior similar to "plateau". However, double exponential current sources are still considered the most reasonable first-order estimate, and it is widely adopted as a base model for SET analysis.

In traditional planar devices, charges associated with the ion tracks colliding the silicon substrate are deposited in the drain directly and then diffuse to the drain, as shown in Fig. 3 [26]. On bulk FinFET devices, the thin fin region has a tight connection to the substrate of the bulk FinFETs. This reduces the area of silicon available for the charge collection when compared with planar devices. In this case, less deposited charges will be diffused in the FinFET drain as illustrates Fig. 3 (b). For these reasons, the FinFET devices are considered less sensitive to soft errors.

Even though the FinFET structure robustness to soft errors compared to planar technologies, its effects cannot be considered negligible [27]. The aggressive scaling and the low supply voltages and the high-frequency operation tend to degrade the robustness in several aspects. These factors help to increase the soft error sensitivity induced by energetic particles such as heavy ions, protons, neutrons and muons coming from space and terrestrial radiations.

III. XOR GATES

Several works explore different implementations of the XOR gate. Most of the works investigate new transistor arrangements, for example, presenting comparative evaluations [28] or reduced number of transistors XOR gates, as in [29] that a 2T XOR circuit is proposed, or as in [30] that menristor MOS technology is explored. Few work have observed the behavior of these circuits under critical situations, as for example low power operation [31, 32], radiation environments [10] or the nanometer variability effects [33, 9].

From the literature review, this work selected a set of nine different XOR topologies similar to the explored in the related works [10, 9], extending the XORs gates considered, the technologies evaluated and the analysis of the near-threshold operation on the radiation robustness. The schematic diagram for each XOR gate is presented in Fig. 4. In this set, four XOR implementations explore the conventional Complementary Logic family, i.e. the CMOS logic family, (V1-V4) and five explore the PTL family (V5-V9) [34].

The CMOS Logic family uses the concept of designing circuits with two complementary networks: a complementary pull-up and pull-down network. It makes circuits present better robustness against noise and reliable operation at low voltages when compared with PTL [35].

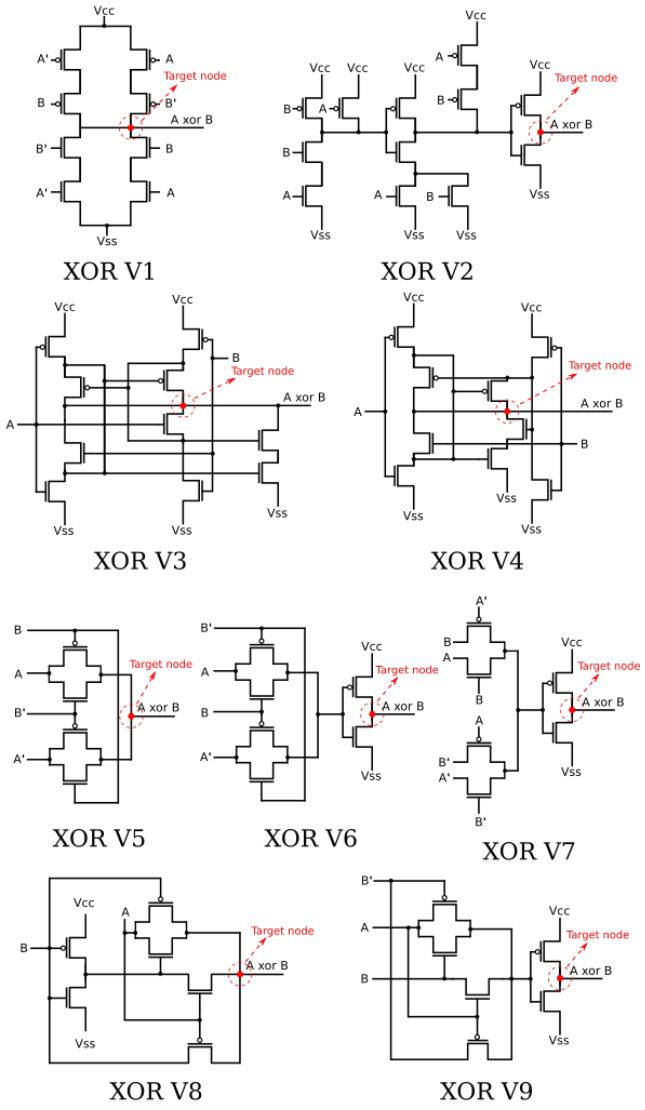


Fig. 4 XORs topologies explored in this work.

The PTL explores transistors' use as switches to transmit logic levels between nodes of a circuit rather than switches connected directly to supply voltages. PTL circuits enable the reduction of redundant transistors, leading many logic functions the capacity of achieving an implementation with a smaller area than complementary logic. However, their output signals tend to be more susceptible to noise [35].

A previous evaluation shows that XOR gates based on PTL are more robustness against radiation effects when compared with the gates implemented with CMOS logic [12]. Furthermore, FinFET-based circuits are more robust than CMOS technology, with an improvement on the LET threshold for both logic families evaluated [12]. Further, a study about the voltage fluctuation considering oscillations about 10% from the nominal voltage shows that this small fluctuation on the operation voltage due to environmental variability can reduce the threshold LET up to 20,8%, increasing the susceptibility of the analyzed circuits [10]. However, there is a lack of a complete evaluation for XOR circuits about the influence on the radiation robustness of technology (bulk CMOS versus FinFET), transistor arrangement, and logic family structures (CMOS logic family versus PTL), considering nominal operation and NTV operation effects. This paper provides a set of data about it, including evaluating how the environment variability effects on the temperature can change the expected SET sensitivity of the XOR gates.

IV. Methodology

To evaluate the soft error impact on XOR logic gates the development of this work consists of four steps, illustrated in the flowchart presented in Fig. 5:

1 - Logical validation of topological arrangements: all nine XOR versions are logically validated and, after that, they are electrically described and simulated in order to guarantee their correct behavior. For both technologies, they are implemented using the model provided by Arizona State University, through Predictive Transistor Model (PTM) at HP 16nm technology node [2, 36].

2 - Electrical characterization: obtains the electrical behavior of the XOR circuits in nominal and NTV conditions, observing the critical delay and power characteristics. To help identify the best design options combining power and delay requirements, this paper also features the PDP.

3 - Evaluation of the robustness to radiation: identifies all the maximum current values that produce a logical change, for all combinations of the logic XOR inputs and choose the worst case. The extraction of data consists of determining the minimum current resulting from the collision of a particle in the circuit in order to cause an error. The minimum current is used to obtain the LET Threshold.

4 - Temperature influence: evaluates the LET threshold under temperature variability for both technologies. The temperature variation goes from the nominal -25 $°C$ to the maximum of 125 $°C$ with an increasing step of 25 $°C$ at each new evaluation. Also, this step evaluates the circuits operation at nominal supply voltage and NTV. In order to keep the same environment of the electrical characterization, it is chosen to keep the same HP models instead of the low power models, considering a critical scenario where the voltage is reduced to near-threshold operation but the circuit is designed to high performance.

All transistors were sized based on the MOSIS CMOS scalable rules for the bulk CMOS technology [37]. Each transistor has a channel length L = 16nm, and channel width of NMOS transistor Wn = 32nm, and PMOS Wp = 64nm. For the FinFET technology, all devices adopted the number of fins equal to three and a channel length L = 16nm. FinFET transistors were sized based on design rules that explicitly relate that FinFET layout demands a minimum sized of FinFET devices to allow internal signal routing and access to the cell's internal pins [22]. All transistor sizing values are summarized in Table I. Two inverters were used as an input and four inverters (fanout-of-4) were used as a load in order to emulate a more realistic scenario [37].

A. Delay and Power Evaluation

All the evaluations of the XOR gates consider the circuits operating at nominal supply voltage and NTV for bulk CMOS and FinFET devices. Both technologies are simulated using the model provided by Arizona State University through Predictive Transistor Model (PTM) at 16nm technology node [36]. The nominal supply voltage used is 0.7V

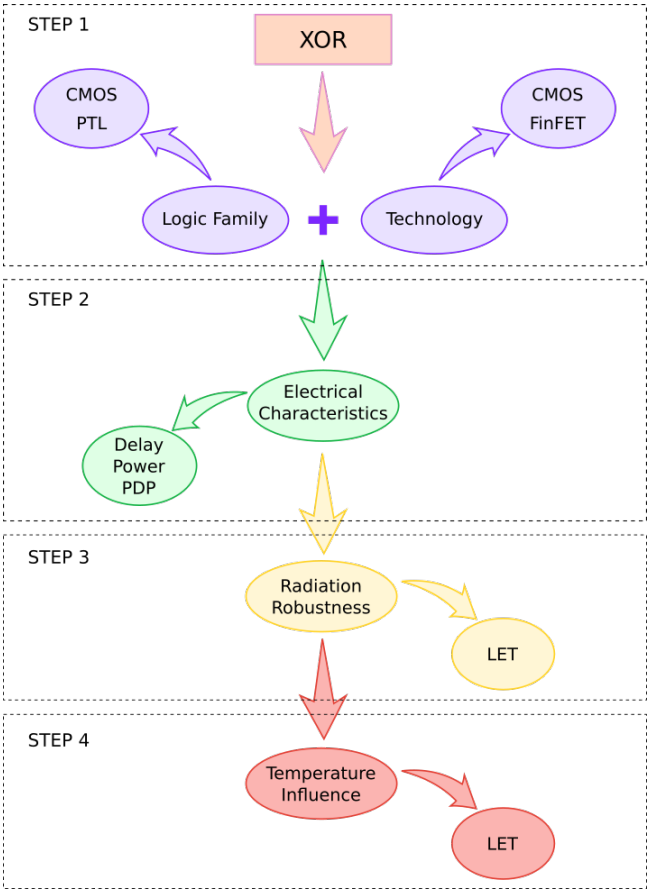


Fig. 5 Evaluation workflow.

for CMOS technology and 0.85V for FinFET technology. The reference threshold voltage ($Vth0$) for both technologies is presented in Table I with other information about the technology parameters, where the fin height is a parameter not applied to the CMOS planar bulk technology. The near-threshold voltage adopted is 0.3V for all the bulk CMOS and FinFET XOR circuits.

One of the challenges for technology scaling is the energy consumption because the increasing in the number of transistors per integration at each new node. The NTV operation has a potential to improve energy efficiency because the frequency of operation reduces almost linearly with reduction in the supply voltage. The NTV also reduces performance linearly, and bring down active energy per operation close to four times. Leakage power also reduces exponentially, and therefore reducing supply voltage should not only reduce power but also improve energy efficiency [38].

Table I. 16nm CMOS and FinFET parameters adopted in this work.

Parameter	**CMOS**	**FinFET**
Supply voltage (V_{dd})	0.70V	0.85V
Threshold voltage ($Vth0$)	0.48V	0.43V
Oxide thickness (t_{ox})	0.95nm	1.35nm
Gate length (L_g)	14.5nm	20nm
Min Width/ Fin width (T_{SI})	29 nm	12 nm
Fin height (h_{FIN})	-	26nm
Minimum device sizing	NMOS=32nm, PMOS= 64nm	3 fins

Hence, it is desirable to operate close to the threshold voltage of the transistor for maximum energy efficiency, providing an increased energy efficiency compared to operating at the nominal supply voltage.

Many experiments show the benefits of the NTV operation continue with technology scaling even including new technologies like tri-gate (FinFET) transistor, showing the advantages across technology generations [39, 40, 41, 42].

The evaluation in this work considers the electrical behavior of the circuits at nominal and NTV operation, starting from the CMOS logic family and then presenting the outcomes for the PTL XOR circuits.

Extensive simulations in HSPICE are carried out to characterize the XOR designs. The experiment consists in extracting critical delay time and energy consumption to calculate total power consumption and PDP for all XOR gates. According the definition of propagation delay time, all the timing arches are evaluated to obtain the critical delay a transient analysis [37]. In order to acquire energy consumption a transient analysis is made, using the energy consumed definition [37].

The total power consumption is the energy necessary for the circuit to compute an operation. It is calculated using the division between energy consumption and the total simulation time multiplied by the power supply voltage, as describe eq. (1).

$$P = \frac{E}{\Delta t} \times Vdd \tag{1}$$

The PDP is the product between power consumption and critical delay, a metric that defines the power dissipated by the circuit to perform a logical operation.

B. Radiation Robustness

The impact that one ion causes in a junction depend on the amount of charge collected while it tracks into the depletion region, i.e., the Linear Energy Transfer (LET) [5]. The robustness of a cell is measured considering the LET threshold, i.e., the minimum energy that cause a transient fault resulting in an error in the system. The simulation of the ion hit at the junction of a device is carried out at the circuit level and the experiments consist of extracting minimum current that causes a transient fault on the device. To obtain the minimum current in a junction, the radiation effect is modeled as a double exponential transient pulse by inserting an independent current source at the sensitive node, based on an analytic solution [24]. For all topologies, the output node was the target of the ion hit injection because the output is always a sensitive node for XOR logic.

After that, the LET is calculated for all XOR gates using the eq. (2). The Q_{coll}, defined by the eq. (3), is the amount of charge collected due to an ion strike in the junction. I_o is the minimum current to cause a fault, obtained by simulations. The term τ_α is the collection time constant of the junction and τ_β is the time constant for the initially establishing the track. For the devices used in this work, these constants are equal to 200ps for τ_α and 10ps for τ_β [43]. The term Q is

the constant charge that the particle deposits along its track and L is the charge collection depth. The value for these constants, Q and L, for CMOS devices are 10.8fC/μm and 2μm, respectively [44]. For FinFET devices the constants Q and L are 10.8fC/μm and 20nm, respectively.

$$LET = \frac{Q_{coll}}{Q \times L} \tag{2}$$

$$Q_{coll} = I_o \times (\tau_\alpha - \tau_\beta) \tag{3}$$

C. Temperature Influence

Variability consists of characteristic deviations, internal or external to the circuit, which can determine its operational features and can be divided by three types concerning its sources: Environmental Factors - External factors to the circuits e.g., temperature and supply voltage variations [45, 46], Reliability Factors - related to the aging process e.g., Negative Bias Temperature Instability (NBTI), electromigration, dielectric breakdown and Hot Carrier Injection (HCI) [47, 46] and Physical Factors - caused by the manufacturing process, consequence of imprecision in the manufacturing process which can be systematic, design-dependent or random. [46, 48, 49, 50, 51].

Despite the multiple advantages of new technologies, the atom scale makes variability one of the most crucial challenges. In this work, XOR cells have been investigated about the temperature variability impact. Typically, the temperature of a circuit in operation may vary from 25°C to 75°C, but, in some cases, this temperature could be superior to 100°C. In the digital design of standard cell libraries, it is considered the behavior of the evaluated XORs from negatives values of -25°C to critical environments with temperature up to 125°C, evaluating the impact of temperature in the radiation robustness.

V. Delay and Power Evaluation

The evaluation considers the electrical behavior of the XOR circuits, first for bulk CMOS technology and then for FinFET devices, starting with the outcomes for the XORs in the CMOS logic, and then, PTL XORs versions. After that, a comparison between the results of the logic families is discussed and finally the results for both technologies are compared. This analysis consider nominal voltage and temperature and the absolute results are presented in Table II. This information is complementary to the radiation robustness evaluation and is essential to help designers choose the most appropriate XOR cell for different applications.

A. Delay

The delay among the CMOS logic versions (V1-V4) implemented in bulk CMOS shows that V4 is the faster gate being up to 8% faster than the worst-case XOR V1 and close to 5% faster than the average for the logic family. For the PTL topologies (V5-V9), the version V5 is the faster one with a delay just close to 17% lower than the worst-case observed in V8 and 12% faster in average for the logic family. Comparing the two logic families, by average, the PTL topologies show 13% improvement in speed and compare the best cases among the two logic, the PTL (V5) shows to be up to 21% faster than the best case for CMOS logic (V4).

For FinFET devices in CMOS logic versions (V1-V4), XOR V3 shows the best results with a delay 30% lower than the worst-case (XOR V2) and almost 2% faster than the average among the logic family. The results for the delay between the PTL topologies (V5-V9) using FinFET devices present that V5 is the faster implementation with a delay up to 42% lower than the worst-case (V9) and almost 28% lower than the average for PTL versions. Comparing the two logic families, PTL topologies show up to 20% lower delay on average. Analyzing the best cases for the families, XOR V5 is more than 30% faster than the best CMOS logic version (V3).

The delay for the topologies implemented with FinFET devices has shown a huge improvement over bulk CMOS devices, as shown in Fig. 6. By average, FinFET implementations have almost 70% of upgrades in computation time. The topology XOR V8 has the greatest delay improvement, more than 77% faster than the same topology within bulk CMOS devices.

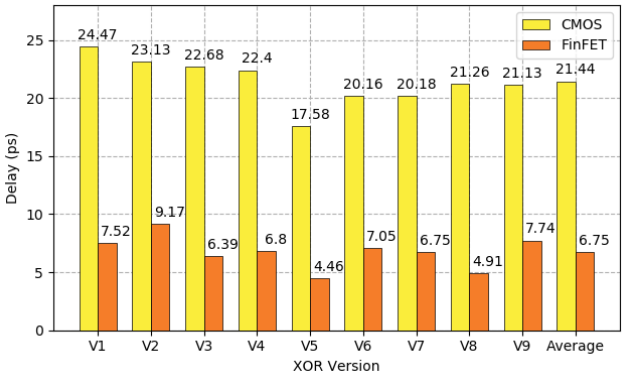


Fig. 6 Critical delay for bulk CMOS and FinFET at nominal voltage.

B. Power

Fig. 7 shows the power results for bulk CMOS devices implemented using CMOS logic each XOR version had similar results. However, it is important to pay attention to XOR V4 that shows a small reduction of almost 7% compared with XOR V2, which had the higher results, but only close to 2% less than the average consumption for the logic family. For the power results for PTL topologies, XOR V8 is the version with less consumption, being close to 21% more efficient than the worst cases presented by the versions V6 and V7, and, up to 8% less than the average among the five PTL implementations. Analyzing and comparing the two logic style, PTL topologies are close to 5% less efficient than CMOS logic. However, V8 shows a little improvement with 5% less consumption than the best case for CMOS logic (V4).

For FinFET technology in CMOS logic, version XOR V1 had the lowest power consumption with a reduction of almost 15% compared with the worst-case (XOR V2) and matching the average value among CMOS logic topologies. The PTL topologies show similar results of CMOS logic. However, the best case (V8) has 28% less consumption than the worst case (V6) and 20% less consumption than the average among the logic family implementations. Comparing the two logic families, PTL topologies reduces almost 8% in the

Table II. Electrical Results of the XORs circuits evaluated for bulk CMOS and FinFET technologies at nominal temperature and voltage

Tech	Result	V1	V2	V3	V4	V5	V6	V7	V8	V9	Average
bulk CMOS	Delay (ps)	24.47	23.13	22.68	22.40	17.58	20.16	20.18	21.26	21.13	21.44
	Power (μW)	0.38	0.39	0.38	0.36	0.37	0.43	0.43	0.34	0.39	0.39
	PDP (aJ)	9.19	9.07	8.59	8.17	6.55	8.61	8.62	7.18	8.16	8.24
FinFET	Delay (ps)	7.52	9.17	6.39	6.80	4.46	7.05	6.75	4.91	7.74	6.75
	Power (μW)	0.35	0.39	0.41	0.37	0.36	0.39	0.38	0.28	0.35	0.36
	PDP (aJ)	2.63	3.58	2.65	2.52	1.58	2.72	2.59	1.35	2.70	2.48

average power consumption for the XOR logic gates implemented. The reduction is more considerable when comparing the best case for PTL (V8) and the best case for CMOS logic, with 20% more efficiency for the PTL topology.

The total power consumption for FinFET devices reaches similar results of bulk CMOS technology, with only a discrete decrease close to 5% on the average power consumption, noticed in the Fig. 7.

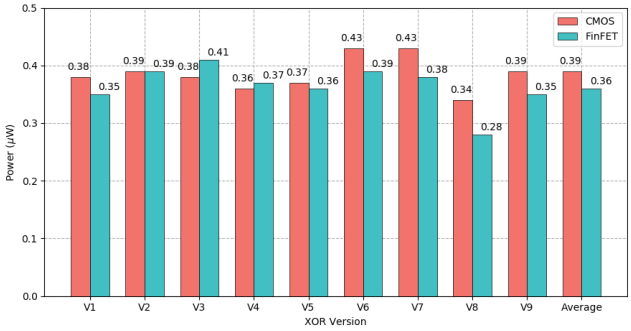


Fig. 7 Power for bulk CMOS and FinFET at nominal voltage.

C. *Power Delay Product*

Fig. 8 shows the results to the PDP to highlight the electrical differences for bulk CMOS and FinFET technologies. Observing the results in the bulk CMOS technology implementations, among the CMOS logic versions, the V4 has the lowest PDP, which is 11% better than the worst-case presented by XOR V1 and up to 6% better than the average between the logic family. For the PTL topologies, V5 is the best case with 24% of reduction on PDP comparing with the V7 (the worst case), and, close to 16% of reduction with the average for the family logic. Comparing the two logic families, PTL topologies show a small reduction of 10% on average PDP and comparing the two best cases PTL topology (V5) present almost 20% reduction in the PDP.

For FinFET devices implemented in CMOS logic, the XOR V4 presents the best PDP being almost 30% lower than the worst-case XOR V2, and,11% lower than the average for the logic family. Observing the PDP results for PTL topologies, V8 is more than 50% better than the worst-case presented by V9, and, close to 38% lower than the average among the PTL topologies. Comparing the two logic families, PTL topologies reduces PDP almost 23% on average. Also, analyzing the best cases for the logic families, we see an almost 47% reduction on the PDP.

The delay reduction of FinFET devices reflects on the PDP. The change for FinFET devices can decrease the average PDP about 70%. Thus, XOR V8 implemented with FinFET presented even better results with a reduction superior to 80% over the same topology in bulk CMOS technology.

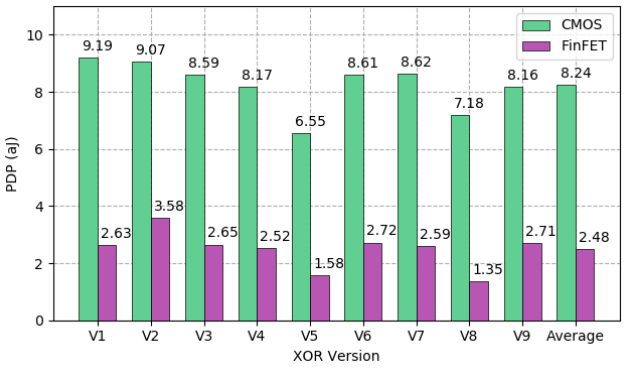


Fig. 8: Power Delay Product for bulk CMOS and FinFET at nominal voltage.

VI. Radiation Robustness

This section considers the radiation robustness of the XOR circuits for bulk CMOS and FinFET technologies, first presenting the results for the CMOS logic topologies, and then, the outcomes for the PTL XOR circuits. After that, a comparison between the logic families is discussed. The last comparison is between bulk CMOS and FinFET.

A. *Bulk CMOS technology*

The XOR V2 was the most robust gate among the CMOS logic topologies (V1-V4) with a LETth of 272.69 $keVcm^2/mg$. It is 2x higher than the other three gates (V1, V3, and V4), that had the same behavior, with a LETth of 131.94 $keVcm^2/mg$.

For the PTL topologies (V5-V9), V5 and V8 had the worst LETth of 131.94 $keVcm^2/mg$. It is near 39% lower than the average of PTL topologies, and, up to 51% lower than the best cases (V6, V7, and V9).

Comparing CMOS logic and PTL families, it was noticed that the PTL topologies analyzed are more robust against radiation effects, with an average LETth of 216.39 $keVcm^2/mg$ which is almost 30% greater than the average for the complementary topologies (167.12 $keVcm^2/mg$). Another point to notice is that V2, V6, V7, and V9 had better results for bulk CMOS technology with a LETth of 272.69 $keVcm^2/mg$, as Fig. 9 shows.

B. *FinFET technology*

For XOR with FinFET devices, from the CMOS logic topologies, V1 and V4 had the worst performance with a LETth of 43.10 $MeVcm^2/mg$, which is close to 18% lower

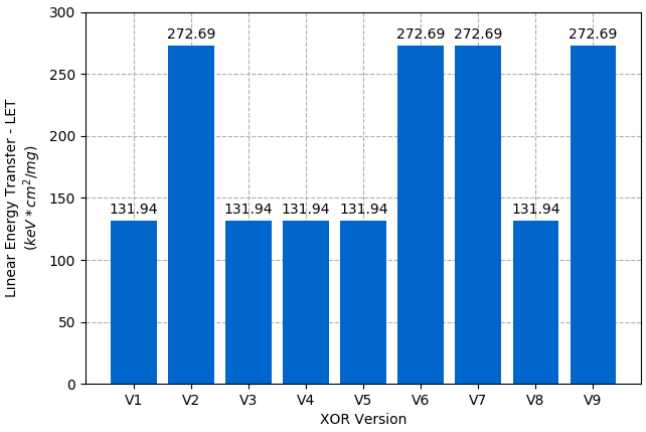


Fig. 9 LETth worst cases for bulk CMOS technology.

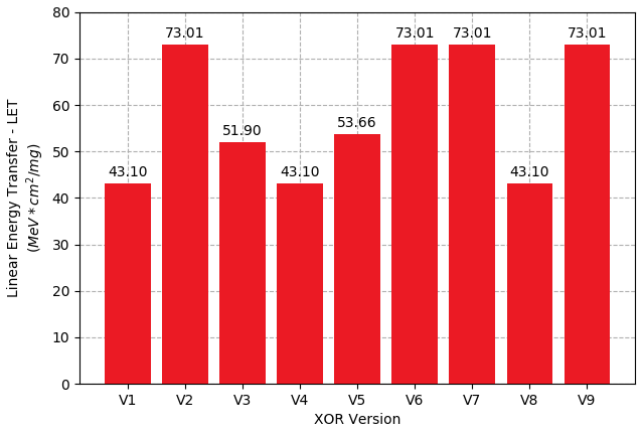


Fig. 10 LETth worst cases for FinFET technology.

than the average LETth among the complementary topologies. Comparing these two topologies with the best case (V5), they have even worst, results being almost 41% lower.

Among the PTL topologies, V8 had the worst LETth of 43.10 $MeVcm^2/mg$, up to 32% worst than the average. Comparing with the best case (V6, V7, and V9), topology V8 is even worst with its LETth being close to 41% lower.

Comparing FinFET complementary logic and PTL topologies, the same behavior noticed for CMOS technology of PTL topologies being more robust than complementary is replicated. The average LETth for the PTL is up to 19% superior to the average for complementary logic. The topologies XOR V2, XOR V6, XOR V7, and V9 presented the best LETth results (73.01 $MeVcm^2/mg$), as showed in Fig. 10.

C. Bulk CMOS and FinFET technology comparison

The FinFET technology has performed an improved robustness compared to the bulk CMOS technology at the two logic analyzed in this work. This can be explained by the better gate control over the channel. As shown in Fig. 9 and 10, the XOR V2, XOR V6, XOR V7 and XOR V9 gates have shown to be the most robust topologies in both technologies with LETth = 272.69 $keVcm^2/mg$ for bulk CMOS and LETth = 73.01 $MeVcm^2/mg$ for FinFET.

The XOR V1, one of the most common topologies found in standard cells, proved to be one of the most sensitive gate with a LETth up to 25% lower than the average for both technologies. FinFET-based for PTL topologies have shown an average LETth 291x greater than bulk CMOS-based devices and for CMOS logic 350x. Further, considering all topologies, FinFET average LETth has shown to be up to 300x higher than bulk CMOS-based devices. This improvement on the LETth demonstrate how the charge collection mechanism differences presented in [23] influence on the fin devices at 16nm technology.

VII. Temperature Influence

This section aims at verifying the influence of temperature variability in the LET threshold for the XOR topologies analyzed at nominal and NTV for both technologies. First, the discussion is made for the bulk CMOS devices at nominal voltage, then for FinFET, comparing temperature variations for the CMOS logic topologies. After that, the results show the temperature influence on PTL versions both logic families. The second half of the section is the discussion for the NTV operation following the same structure. At the end, a short comparison between the nominal and NT voltage is made, all results are presented in Table III and Table IV.

Table III. Results of LET threshold of XOR circuits evaluated at nominal voltage for *bulk CMOS* and *FinFET* technology.

Tech	Temp. ($^\circ C$)	V1	V2	V3	V4	V5	V6	V7	V8	V9	Average
bulk CMOS ($keVcm^2/mg$)	-25	193.52	334.26	193.52	193.52	193.52	334.26	334.26	193.52	334.26	256.06
	0	167.13	307.87	167.13	167.13	167.13	307.87	307.87	167.13	307.87	229.68
	25	131.94	272.69	131.94	131.94	131.94	272.69	272.69	131.94	272.69	194.50
	50	114.35	246.30	114.35	114.35	114.35	246.30	246.30	114.35	246.30	172.99
	75	96.76	211.11	96.76	96.76	96.76	211.11	211.11	96.76	211.11	147.58
	100	79.17	175.93	79.17	79.17	79.17	175.93	175.93	79.17	175.93	122.17
	125	70.37	158.33	70.37	70.37	70.37	149.54	149.54	70.37	149.54	106.53
FinFET ($MeVcm^2/mg$)	-25	42.22	67.73	49.26	42.22	49.26	67.73	67.73	42.22	67.73	55.12
	0	42.22	70.37	50.14	42.22	51.02	70.37	70.37	42.22	70.37	56.58
	25	43.10	73.01	51.90	43.10	53.66	73.01	73.01	43.10	73.01	58.54
	50	43.10	74.77	51.90	43.10	52.70	74.77	74.77	43.10	74.77	59.22
	75	43.10	75.65	51.90	52.78	52.78	75.65	75.65	43.10	75.65	59.62
	100	42.22	76.53	51.02	42.22	51.90	76.53	76.53	42.22	76.53	59.52
	125	41.34	76.53	50.14	41.34	51.90	76.53	76.53	41.34	76.53	59.13

A. *Nominal voltage*

For bulk CMOS technology, the temperature variation reduces the robustness for CMOS logic topologies in average 44%, when working in the maximum temperature value $(125°C)$. The topology less sensitive to temperature impacts is XOR V2, with a maximum decrease close to 42%. A point to highlight is that the biggest decrease in the robustness occurs when the temperature vary from $(100°C)$ to $(125°C)$ with a reduction over 15% for the XOR V2 version. Among the PTL versions, the robustness reduction is slightly higher than the CMOS logic, with a decrease of almost 46%. The less sensitive version for PTL topologies is V6, with a maximum reduction in robustness close to 45%. When comparing the two logic families, the PTL topologies are more sensitive to the temperature variability, on average 2%. The Fig. 11 illustrate the reduction in the robustness for bulk CMOS devices in the temperature variability.

For FinFET technology, the temperature variability results show that CMOS logic topologies have an average variation of 1% in the robustness. The versions XOR V1, XOR V3, and XOR V4 present a decrease of almost 4%. However, XOR V2 shows an increase in the LET threshold close to 4%. The PTL versions show, in average, a higher sensitivity to radiation of 2% in the temperature variability scenario. The less sensitive are XOR V6, V7, and V9 that presented an increase in the robustness close to 4%, as the CMOS logic version XOR V2. The PTL versions appear similar to the radiation effects in higher temperatures to CMOS logic comparing the two logic families.

The results of LETth for FinFET devices show an average variation of up to 1%. With this percentage can be noticed that the technology is more robust to the temperature variation, presenting almost no drawbacks, even to higher temperature values, as shown in Fig.12.

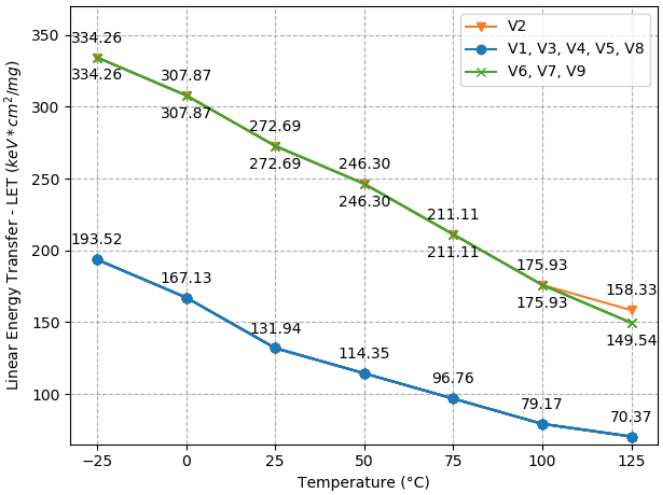


Fig. 11: The LETth worst cases for bulk CMOS technology at nominal voltage.

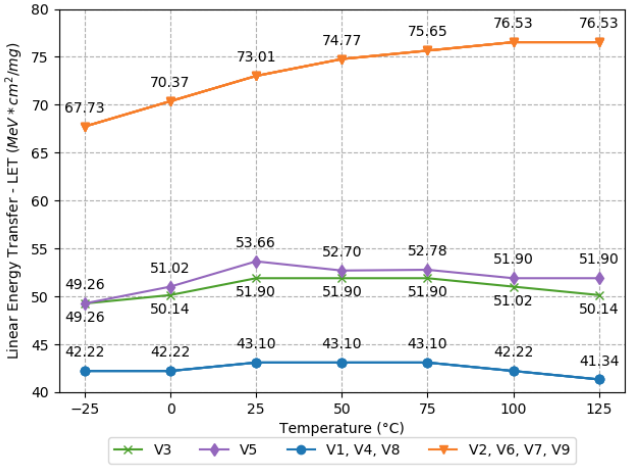


Fig. 12 The LETth worst cases for FinFET technology at nominal voltage.

B. *Near-Threshold Voltage*

The bulk CMOS technology increases up to 8% the LETth value for CMOS logic, on average. The XOR V1 at NTV shows no drawback under the temperature variability, having a constant LETth of 5.28 $keVcm^2/mg$. Among the PTL topologies, the improvement in the average LETth under temperature variation was also close to 8%. The XOR V7 and V9 show less affected with an increase of just 2% in the minimum LETth. When comparing both logic families, it is possible to identify that PTL topologies show, on average, higher LETth values, which means they are more robust to the radiation effects. Besides that, the PTL gates have a

Table IV. Results of LET threshold of XOR circuits evaluated at near-threshold voltage for *bulk CMOS* and *FinFET* technologies.

Tech	Temp. $(°C)$	V1	V2	V3	V4	V5	V6	V7	V8	V9	Average
bulk CMOS $(keVcm^2/mg)$	-25	5.19	7.30	5.28	5.10	5.45	7.30	7.30	5.28	7.30	6.16
	0	5.10	6.69	5.19	5.10	5.28	6.69	6.69	5.10	6.69	5.83
	25	5.28	6.33	5.19	5.06	5.32	6.42	6.42	5.19	6.42	5.74
	50	5.28	6.42	5.23	5.13	5.45	6.44	6.47	5.32	6.42	5.80
	75	5.28	6.51	5.37	5.22	5.57	6.51	6.50	5.41	6.51	5.88
	100	5.28	6.69	5.45	5.32	5.69	6.60	6.55	5.45	6.56	5.95
	125	5.28	6.86	5.54	5.41	5.72	6.65	6.60	5.54	6.59	6.02
FinFET $(MeVcm^2/mg)$	-25	1.32	2.02	1.32	1.32	1.32	2.02	2.02	1.32	2.02	1.63
	0	1.94	2.90	1.94	1.85	1.94	2.90	2.90	1.85	2.90	2.34
	25	2.55	3.87	2.55	2.46	2.55	3.78	3.78	2.46	3.78	3.09
	50	3.34	5.01	3.34	3.25	3.25	4.93	5.01	3.25	4.93	4.03
	75	4.13	6.33	4.22	4.05	4.22	6.33	6.33	4.05	6.33	5.11
	100	4.93	7.74	5.10	4.84	5.10	7.34	7.74	4.84	7.74	6.20
	125	5.72	9.06	5.98	5.63	5.98	9.06	9.06	5.63	9.06	7.24

lower or equal improvement in the robustness under temperature variability, as Fig. 13 shows, which means they suffer less influence of temperature effects. It also possible to observe a slight increase in the LETth for temperatures under $0°C$ for all topologies.

For CMOS logic with FinFET devices, the LET threshold improvement is 1.3x, on average, under the temperature variability. The topologies XOR V2 and XOR V3 presented the best results with the LETth 1.34x higher in the maximum temperature, which means they are less sensitive to radiation when operating on higher temperatures. For the PTL versions, the increase in the robustness is close to 1.36x, on average. The XOR V9 shows the best improvement when working on higher temperatures with a LETth becoming approximately 1.4x greater. The Fig. 14 shows that the PTL versions working in the maximum temperatures have a slightly better improvement of up to 2% in robustness.

Comparing both technologies working at NTV, the topologies implemented using CMOS logic with FinFET devices have proved to be 525x, on average, more robust than the same implementations on bulk CMOS. For PTL versions, with FinFET technology, the improvement is even more significant, being 550x more robust on average. However, the temperature dependence severely impacts the FinFET technology devices operating at near-threshold, mainly due to the quantum-mechanical limit [52].

C. *Nominal vs Near-threshold voltage*

The reduction of the supply voltage can directly affect the robustness to SET of XOR circuits. The temperature affects the bulk CMOS devices mainly due to energy imposed in the doped structure provoking the rise of SCE effects as the rise on the leakage current and other thermal features on the model. FinFET devices, due to the fin structure, high metal gate isolation and undoped (or slightly doped) channels are less sensitive to thermal effects. More details about the temperature behavior of Multigate devices are presented [53, 54]. The LETth is also related with the internal energy on the device due to the charge collection and funneling effects. For bulk CMOS technology, the robustness reduction working on NTV is almost 97% for CMOS logic topologies and close to 95% for PTL topologies. Comparing the same results for FinFET technology, the reduction of robustness while working at NTV is similar, presenting a decrease of 94% in the average LETth for CMOS logic and almost 95% to PTL versions.

VIII. Conclusions

This paper presented a comparative analysis of electrical behavior and radiation sensitivity at different XOR logic gate topologies based on CMOS and FinFET devices.

The fastest topology among the nine XOR logic gates analyzed was the XOR V5, for both technologies. The results for power consumption shows that the topology XOR V8 presents the best result for both technologies. The PDP analysis shows that XOR V5 presents the best result for bulk CMOS and XOR V8 for FinFET. However, it was found that XORs with FinFET devices, at nominal conditions, are almost 70% faster than the same implementations with bulk

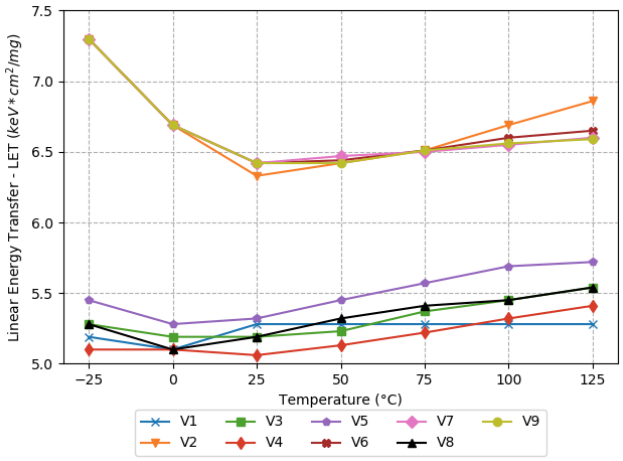


Fig. 13: The LETth worst cases for bulk CMOS technology at near-threshold voltage.

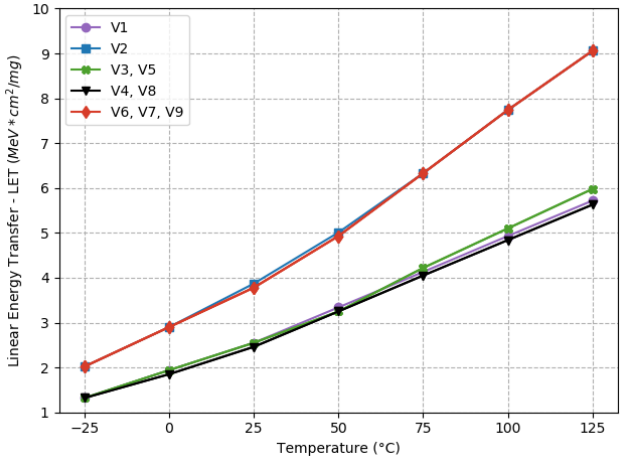


Fig. 14: The LETth worst cases for FinFET technology at near-threshold voltage.

CMOS. Also, they decrease power consumption close to 5% and reduce PDP up to 70%.

At nominal condition, the evaluation concludes analytically that the topologies implemented with CMOS logic are more sensitive to transient faults caused by radiation, at the output node than PTL topologies. For all evaluated circuits, FinFET devices have shown to be more robust against transient faults, caused by radiation, than the bulk CMOS-based circuits. For both technologies, XOR V2, XOR V6, XOR V7, and XOR V9 have shown to be the least sensitive to the radiation effects, considering both logic style. These four circuits are the topologies with one inverter on the outputs, delivering the XNOR and XOR functions. The addition of the inverter on the output have enhanced the XOR robustness for SETs adding one more logical step on the circuit, changing the output capacitance and disconnecting the internal nodes from output interference. Also, circuits with FinFET devices improve robustness against transient faults, by average, more than 300x for both CMOS logic and PTL on nominal temperature and voltage.

It is also possible to verify that both temperature variability and supply voltage range, can affect the sensitivity of XOR logic gates and reduce its robustness for both technolo-

gies. However, FinFET devices still show to be more than 525x more robust against transient faults, caused by radiation. The improvement is still greater when evaluating PTL topologies with an increase in robustness over bulk CMOS devices over 550x.

Best XOR gate designs have unarguable relevance on computer systems and consider the effects of nanotechnologies is each day more essential. Each day new technologies with new challenges are emerging as new XOR topologies. As future work, it is important to consider process variability and aging effects on the electrical characteristics and the radiation robustness, also contemplating new XOR topologies and technologies.

ACKNOWLEDGEMENTS

This work was financed in part by National Council for Scientific and Technological Development CNPq and the Propesq/UFSC.

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