Analysis of Current Mirrors with Asymmetric Self-Cascode Association of SOI MOSFETs through SPICE Simulations

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***Abstract*— In this paper the performance of different architectures of current mirrors implemented with single SOI transistors and self-cascode transistors, both symmetric and asymmetric is evaluated. A comparison of current mirrors figures of merit, looking for the advantages of the asymmetric composite structure in relation to a single SOI MOSFETs and the symmetric self-cascode transistor is performed. This analysis has been carried out through analytical simulations, using common-source, Cascode and Wilson current mirrors architectures. It is shown that asymmetric configuration can provide larger output resistance even in the common-source current mirror than other architectures with conventional single transistors.**

Index Terms*— SOI nMOSFET transistor, Asymmetric self-cascode, Composite transistor, Current Mirror, SPICE Simulation.

I. INTRODUCTION

Silicon-On-Insulator (SOI) technology consists in an alternative to the conventional Metal-Oxide-Semiconductor (MOS) technology for realizing integrated circuits of high scalability (Ultra Large-Scale Integration – ULSI) for digital and analog circuits [1]. In this technology devices are fabricated in a thin film of semiconductor separated from the substrate by an insulating film, named buried oxide. The intrinsic dielectric isolation between the active region and the substrate promoted a series of advantages, such as the increase of drain current and the transconductance (g_m), reduction of short-channel effects [1], and reduction of body factor and junction capacitance [2], especially for thin-film Si layers, that operate in full depletion. Despite of these advantages, fully depleted (FD) SOI transistors may present degraded analog performance, due to parasitic bipolar effects, responsible for decreasing the breakdown voltage [3], and the channel length modulation that degrades output conductance (g_D) [4], reducing the output resistance (R_{OUT}).

The output conductance is a very important parameter for analog circuits. There are different ways to improve the output conductance in MOS transistors. The most common way is to increase its channel length [5]; however, apart from increasing area consumption, the use of longer channel lengths degrades transconductance and hence cutoff frequency [4]. The cascode association is another possibility for improving output conductance of MOS transistors, but on the other hand, causes loss of linear output voltage range [6]. An alternate composite structure is the self-cascode association [7, 8, 9], which provides the output conductance reduction while keeping the advantages of short channel lengths, such as high drain current level and cutoff frequency. This structure consists in a series association two transistors with short-circuited gates acting as a single device [7, 8, 9], as schematically shown in Figure 1.

In this composite structure, transistor M_D is placed at the drain side and features length L_D, while M_S is the transistor near the source side with length L_S. The effective channel length (L) is then the sum of L_S and L_D. V_X corresponds to the voltage at the intermediate node of the composite device. Usually, the self-cascode (SC) structure [4, 7, 8, 9] features transistors M_D and M_S with the same channel doping concentration level, leading to similar threshold voltage (V_{TH}) for both transistors. This structure will be called symmetric self-cascode (S-SC).

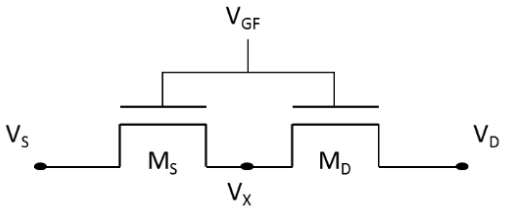

Fig. 1 - Schematic representation of a self-cascode transistor.

An alternative to further improve analog performance of SC transistors is the asymmetric self-cascode (A-SC) configuration where M_D features reduced threshold voltage, whereas M_S is responsible for fixing the threshold voltage of the overall structure [10]. The reduced threshold voltage of M_D forces it to work in saturation, absorbing part of the voltage bias applied to the drain of the composite transistor structure. This structure has been reported to provide several advantages from analog perspective, at device level, such as larger current drain, transconductance and breakdown voltage and reduced output conductance in comparison to S-SC and single transistors with similar dimensions [10, 11, 12, 13].

One of the most important analog basic blocks is the current mirror [5]. In this circuit, the input current, I_{IN}, is mirrored to the input branch, keeping its current, I_{OUT}, constant. To achieve this constant current, high output resistance is required, reducing output current dependence on output voltage. There are several architectures for this circuit. The Common-Source (CS) configuration is the simplest approach for CM, and it consists in two transistors connected as shown in Fig. 2A. In a first approximation, the ratio between output and input currents, named mirroring precision, is given by the ratio $(W/L)_{Q2}/(W/L)_{Q1}$, where W is the channel width. Therefore, for Q_1 and Q_2 with the same dimensions, I_{OUT}/I_{IN} is expected equals one. However, since input and output transistors are biased at different drain-to-source voltage (V_{DS}), the finite MOSFET output resistance is responsible for the accuracy deviation from the expected value. As expected, as channel length is reduced, the output degradation worsens this effect. Aiming at reducing the output conductance (increase output resistance) of current mirrors, some alternative architectures can be used, such as the Cascode and Wilson

Digital Object Identifier 10.29292/jics.v15i2.159

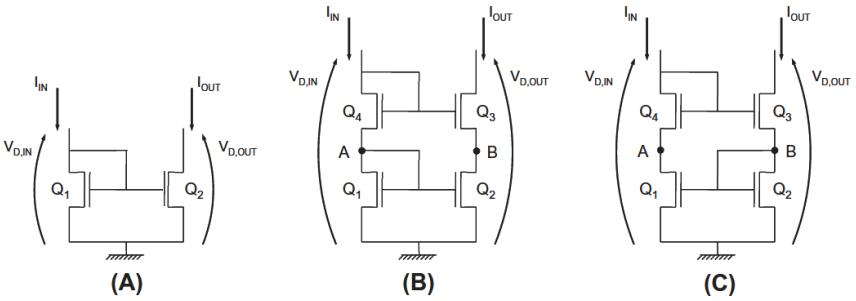

Fig. 2 - Common-source (A), Cascode (B), and Wilson (C) current mirrors architectures.

configurations, also shown in Figure 2 (B and C, respectively), which are composed by four transistors.

Although the A-SC has shown to provide advantages from the analog point of view, only one work has reported its use in an analog block (common-source CM) [12]. However, there is no report on analytical simulation of any analog blocks with A-SC, that could allow for its design. This way, in this paper a comparative analysis of electrical characteristics of different current mirror architectures using single transistors, symmetric and asymmetric self-cascode is presented. The analysis is performed for Common-source, Cascode and Wilson current mirrors, by means of analytical SPICE simulations. Mirroring precision, saturation voltage and output resistance were used as figures of merit in this study.

II. Devices Characteristics and Simulator Calibration

The software ICAP/4 by Intusoft [14] was used to run the analytical simulations in this study. This simulator presents in its library the model proposed by Iñiguez *et al* [15] for FD SOI transistors drain current. This model is analytical, continuous and physically-based, taking into account mobility degradation due to electric field, channel length modulation and carrier velocity saturation. The drain current is obtained through the inversion charge densities at the drain and source edges ($Q_{nf,D}$ and $Q_{nf,S}$ respectively), using equation (1):

$$I_{DS} = \frac{W}{L_{eff}} \frac{\mu_n}{1+V_{DSE}\frac{\mu_n}{L_{eff}v_{sat}}} \left[v_T\left(Q_{nf.D} - Q_{nf.S}\right) - \frac{Q_{nf.D}{}^2 - Q_{nf.S}{}^2}{2nC_{oxf}} \right] \quad (1)$$

Model parameters were calibrated to fit experimental data of FD SOI transistors fabricated at *UCLouvain*, Belgium. This technology features front gate oxide thickness of 31 nm, back gate oxide thickness of 390 nm and silicon layer thickness of 80 nm [02]. Experimental measurements of transistors with W/L = 20 µm/2 µm and two different doping concentration levels were used to fit model parameters. Table I summarizes the obtained parameters.

Figure 3 presents the comparison between experimental and simulated results for the drain current (I_{DS}) and the transconductance as a function of gate voltage (V_{GS}). The drain current as a function of drain bias (V_{DS}), measured at $V_{GT} = V_{GS} - V_{TH} = 200$ mV is presented in Figure 4 as well its derivative, the output conductance (g_D). From these curves one can note that the simulation results fit the experimental data with good agreement, except in the region where impact ionization occurs, since the analytical model does not consider this effect. However, this region is not of interest for analog circuit operation.

These figures also show the obtained curves for the symmetric and asymmetric self-cascode transistors. It is possible to note that the S-SC reduces the drain current and transconductance to approximately half of the values obtained for the standard single transistor, due the increase of channel length ($L_{eff} \approx L_S + L_D$). On the other hand, the use A-SC, increases the drain current and transconductance peak. However, the increase of front gate voltage causes larger transconductance degradation in the A-SC, and its values get closer to the transconductance of S-SC device with similar dimensions as reported in the literature. One can also note that the S-SC reduces the output conductance in comparison to the single transistor (ST), and that A-SC allows for further reduction of this parameter.

Table 1 - Model parameters fitted to the experimental data.

Parameter	$N_A = 10^{17}$ cm^{-3}	$N_A = 10^{15}$ cm^{-3}	Unit
V_{TH}	0.380	-0.3650	V
n	1.100	1.100	–
μ_0	600×10^{-4}	800×10^{-4}	m^2/V.s
af	3.0×10^{-8}	3.0×10^{-8}	–
S_{NT}	0.97	0.97	–
A_{TS}	2.50	2.50	–
σ	0.0115	0.0040	–
l_d	5.0×10^{-8}	9.0×10^{-8}	m

III. Current Mirror Simulation and Discussion

By using the model parameters fitted to experimental measurements, current mirrors composed by identical transistors were simulated with different circuits architectures and channel lengths.

A. *Mirroring precision*

Current mirrors composed by identically designed transistors are expected to present mirroring precision, i.e. I_{OUT}/I_{IN} close to the unity [5]. However, the mirroring precision may depart from its ideal value due to several reasons, such as geometrical mismatching or difference between bias conditions of transistor that composes input and output branches of the mirror [5].

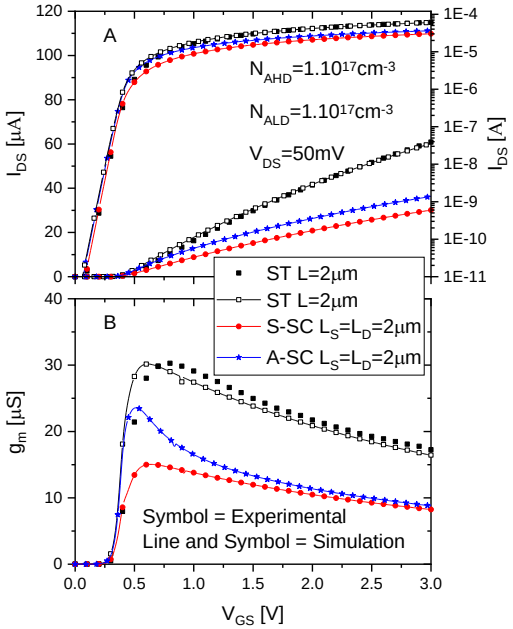

Fig. 3 - (A) Drain current and (B) transconductance as a function of gate voltage measured for single transistor, symmetric and asymmetric self-cascode devices, biased at V_{DS} = 50 mV.

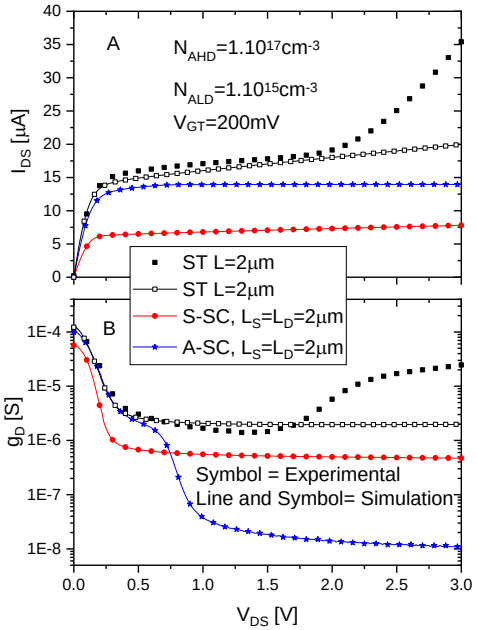

Fig. 4 - (A) Drain current and (B) output conductance as a function of drain voltage measured for single transistor, symmetric and asymmetric self-cascode devices, biased at V_{GT} = 200mV.

As the performed simulations do not consider random mismatching that may occur during fabrication, any deviation from unity may be attributed to bias mismatching.

Figure 5 presents curves of the mirroring precision (I_{OUT}/I_{IN}) as a function of input current (I_{IN}) simulated for common-source CM with S-SC and A-SC with total channel length ($L_S + L_D$) of 4 µm with fixed output voltage (V_{OUT}) of 1.5 V. Results for CMs with ST with L = 2 µm and 4 µm, Cascode and Wilson CM with L = 2 µm are also shown. From these curves it is possible to note that as I_{IN} is reduced, approaching weak inversion region, the mirroring precision departs from unity for all structures and devices. The use of a composite transistor reduces the accuracy variation in comparison to single transistors. In the case of SC, both symmetric and asymmetric, the reduction of L_S worsens the mirroring precision. However, it is possible no note that the use of asymmetric structure reduces the accuracy variation since the improved output conductance reduces the dependence of the output current on applied bias.

B. Output resistance

Figure 6 presents the output current I_{OUT} as a function of V_{OUT} curves simulated at I_{IN} = 10 µA, which bias the circuits in a moderate inversion regime. In this figure, curves for CM composed by single transistor, S-SC and A-SC are presented. Cascode and Wilson CM results for ST with L = 2 µm are also presented. As expected, for CS current mirrors, the reduction of channel length (L) makes I_{OUT} current more dependent on V_{OUT}. By using the S-SC in the CS mirror reduces this dependence, although it is still larger than that observed for Cascode and Wilson CMs, where I_{OUT} is practically constant. The use of A-SC in the CS mirror allows for obtaining results close to those presented by Wilson and Cascode.

This I_{OUT} dependence on V_{OUT} can be expressed as the output resistance (R_{OUT}) of the current mirrors. This parameter

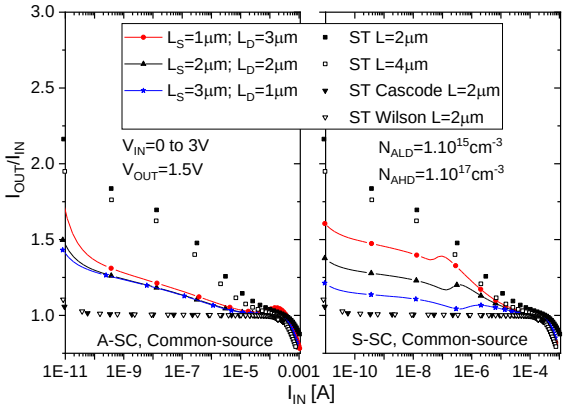

Fig. 5 - I_{OUT}/I_{IN} curves as a function of input current for current mirrors implemented with conventional transistors in common-source, Cascode and Wilson architecture, symmetric and asymmetric self-cascode, extracted at V_{IN} = 0 V - 3 V and V_{OUT} = 1.5 V.

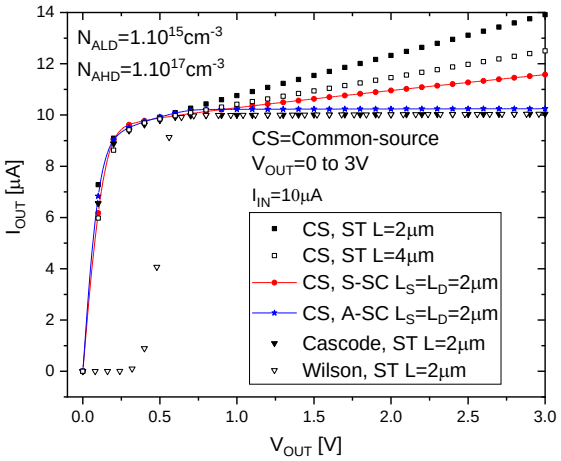

Fig. 6 - I_{OUT} curves as a function of the output voltage, biased at I_{IN} = 10 µA for current mirrors implemented with conventional transistors in common-source, Cascode and Wilson architecture, symmetric and asymmetric self-cascode structure.

Table 2 - Output resistance for different CMs biased at I_{IN} = 10 nA and 1 µA with V_{OUT} = 2 V.

Device	L_S [µm]	L_D [µm]	Current Mirror	R_{OUT} [Ω] @ V_{OUT} = 2.0V	
				I_{IN} =10 nA	I_{IN} =1 µA
Single Transistor	2	-	CSource	1.2×10^{8}	2.5×10^{6}
			Cascode	1.9×10^{10}	2.8×10^{8}
			Wilson	1.8×10^{10}	2.8×10^{8}
	4	-	CSource	1.3×10^{8}	3.4×10^{6}
S-SC	1	3	CSource	2.8×10^{8}	4.5×10^{6}
	2	2		6.3×10^{8}	7.2×10^{6}
	3	1		1.7×10^{9}	3.1×10^{7}
A-SC	1	3	CSource	4.2×10^{10}	5.7×10^{8}
	2	2		4.6×10^{10}	6.7×10^{8}
	3	1		3.7×10^{10}	5.7×10^{8}

Table 3 - Saturation voltage for different CMs biased at I_{IN} = 10 nA and 1 µA.

Device	L_S [µm]	L_D [µm]	Current Mirror	V_{SAT} [V]	
				I_{IN} =10nA	I_{IN} =1µA
Single Transistor	2	-	CSource	0.12	0.10
			Cascode	0.30	0.47
			Wilson	0.32	0.48
	4	-	CSource	0.12	0.12
S-SC	1	3	CSource	0.13	0.12
	2	2		0.13	0.12
	3	1		0.14	0.13
A-SC	1	3	CSource	0.61	0.64
	2	2		0.68	0.67
	3	1		0.70	0.71

has been extracted from the inverse of the output conductance as a function of V_{OUT}. The results obtained at weak inversion (I_{IN} = 10 nA) and moderate inversion (I_{IN} = 1 µA) are presented in Table 2, extracted at V_{OUT} = 2 V.

Comparing R_{OUT} of CMs with single transistors, one can note that Cascode and Wilson current mirrors provide significantly larger values than in the Common-source architecture for all lengths and current bias. The adoption of Cascode and Wilson provides an improvement of about 150 times in the value of R_{OUT} at I_{IN}=10 nA and 112 times at I_{IN} = 1 µA in relation to CM mirrors with single transistors with L = 2 µm. The improved output conductance provided by the A-SC transistors is responsible for further increasing the output resistance of CM even in Common-Source configuration. When comparing the CS with A-SC (with L_S = L_D = 2 µm) to Cascode and Wilson with the same transistor dimensions, the improvement is about 2.4 times at both I_{IN} levels.

C. Saturation Voltage

To work as a current source, it is desirable that current mirrors present large range of output voltage for which I_{OUT} is kept constant. Apart from having high breakdown voltage, it is desired that CMs present low saturation voltage (V_{SAT}). Since the model used in the SPICE simulations does not consider high electric field effects that lead the transistor to breakdown, only the saturation voltage will be analyzed. However, it has been already reported that A-SC presents larger breakdown voltage at device level [10], that would result in larger maximum allowed output voltage in the CM with the asymmetric structure.

The saturation voltage has been obtained using the extraction method described in [16], that uses the peak of curve $[d(1/g_{D,OUT})/dV_{OUT}\ x\ g_{D,OUT}]$ as a function of V_{OUT}, biased with constant I_{IN} to define V_{SAT}. The results obtained with I_{IN} = 10 nA and I_{IN} = 1 µA are presented in Table 3. Since Cascode and Wilson CMs present two transistors in series with different gate voltages, larger V_{OUT} is necessary to saturate both transistors in the output branch in comparison to CS mirrors with ST. On the other hand, although CS mirror with S-SC also features two transistors in series, they have the same gate voltage, and present overall V_{SAT} like that of ST [10]. However, it is not observed when CS mirror is implemented with A-SC. Due to the reduced threshold voltage of M_D in the A-SC, this composite transistor presents larger saturation voltage, as also shown in Table 3.

D. Influence of L_D length on the Current Mirror performance

It has been already reported that the output conductance of A-SC can be reduced with the increase of L_D [17]. Therefore, in order to verify if this characteristic can contribute to CM performance, CS CMs were simulated both with S-SC and A-SC with L_S = 2 µm and different values of L_D. Figure 7 presents the mirroring precision as a function of I_{IN} for CMs biased at V_{OUT} = 1.5 V. One interesting point to be noted is

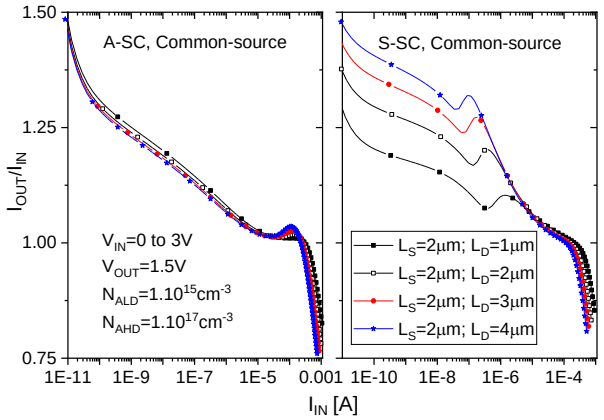

Fig. 7 - I_{OUT}/I_{IN} curves as a function of input current for CMs implemented with ST, S-SC and A-SC transistors with L_S fixed and L_D variable, simulated at V_{OUT} = 1.5V.

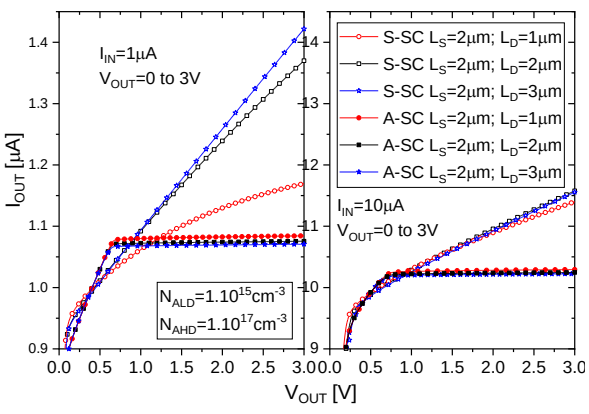

Fig. 8 - I_{OUT} curves as a function of V_{OUT}, biased at I_{IN} = 1 µA and I_{IN} = 10 µA for CMs implemented with symmetric and asymmetric self-cascode structure with L_S fixed varying L_D from 1 µm to 3 µm.

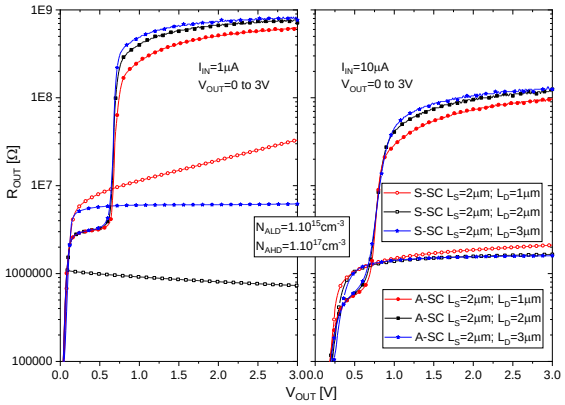

Fig. 9 - R_{OUT} curves as a function of V_{OUT}, biased at I_{IN} = 1 μA and I_{IN} = 10 μA for CMs implemented with symmetric and asymmetric self-cascode structure with L_S fixed varying L_D from 1 μm to 3 μm.

that the accuracy in CM with S-SC is strongly affected by L_D, since it corresponds to an increase of the total effective length. On the other hand, for CM with A-SC, as M_S acts as a main transistor, the bias mismatching is weakly dependent on L_D, indicating that any geometrical mismatching in this transistor during fabrication process would not significantly affect the mirroring precision.

Figure 8 presents I_{OUT} *vs* V_{OUT} curves at I_{IN} = 1 μA and I_{IN} = 10 μA for the CMs with L_S = 2 μm and L_D ranging from 1μm to 3 μm. From the presented results one can note that the use of A-SC is able to keep output current virtually independent on the output voltage, while CMs with S-SC present a large current variation.

The output resistance as a function of output voltage is presented in Figure 9 for the two different input current levels. It is possible to see that for devices with same dimensions, the reduction of M_D threshold voltage can promote the increase of R_{OUT} in more than two orders of magnitude. Also, it is possible to achieve larger R_{OUT} with A-SC with reduced dimensions in comparison to CM with S-SC.

IV. Conclusions

The presented work has analyzed the performance of current mirrors implemented with single transistors, symmetric and asymmetric self-cascode structures. The analysis has been performed through analytical simulation using Common-source, Cascode and Wilson architectures. As expected, Cascode and Wilson CMs are able to increase output resistance in more than 100 times in comparison to Common-source mirrors. However, they also cause an increase of saturation voltage. Common-source mirrors using self-cascode structure uses the same number of transistors than Wilson and Cascode, but as all transistors present the same gate voltage, there is no increase of saturation voltage in comparison to single transistor. However, the maximum increase of output resistance is only 15 times. The results have shown that A-SC in Common-Source mirrors was able to promote output resistance increase from 228 to 383 times in comparison to single transistor, depending on channel lengths and input current. However, due to the reduced threshold voltage, an increase of saturation voltage is observed. It has been shown that for fixed L_S, L_D variation causes reduced bias mismatching if A-SC is used in relation to S-SC due its reduced output conductance for the same dimensions. Also, CM parameters are less sensitive to L_D in the asymmetric structure, indicating that it would be less affected by intrinsic mismatching. By lowering the threshold voltage of M_D, larger output resistance can be achieved with shorter transistors in comparison to the symmetric structure.

Acknowledgements

The work was supported by CNPq grants #311466/2016-8 and #427975/2016-6.

References

[1] Colinge, J. P. Silicon-on-insulator technology: materials to VLSI. Kluwer Academic, Massachusetts, 2004, 3rd edition.

[2] Flandre, D., Adriaensen, S., Akheyar, A., *et al.*: Fully depleted SOI CMOS technology for heterogeneous micropower, high temperature or RF microsystems. Solid-State Electronics, 2001, **45** (4), pp. 541-549.

[3] Choi J. I., Fossum J. G. Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFETs. IEEE Trans. Electron Dev. 1991, **38**, pp. 1384-1391.

[4] Schneider M. C., Galup-Montoro C. CMOS analog design using all-region MOSFET modeling. Cambridge: Cambridge University Press, 2010.

[5] Laker, K.R., Sansen, W.M.C. Design of analog integrated circuits and systems. McGraw Hill, New York, 1994.

[6] Crawley, P. J., Roberts, G. W. Designing operational transconductance amplifiers for low voltage operation. In: Proceding of IEEE international symposium on circuits and systems, Chicago, IL; May 1993. pp. 1455-1458.

[7] Galup-Montoro C., Schneider M. C. Series-parallel association of FET's for high gain and high frequency applications. IEEE Solid-State Circuits 1994, **29,** pp. 1094-1101.

[8] Gao, M., *et al*. Dual MOSFET Structure for suppression of kink in SOI MOSFETs at room and liquid helium temperature, in Proc. 1990 IEEE SOS/SOI Techn. Conf., 1990, pp. 13-14.

[9] Gao, M., Colinge, J. P., Lauwers, L., Wu, S. and Claeys, C. Twin-MOSFET Structure for Suppression of the Kink and Parasitic Bipolar Effect in SOI MOSFET's at Room and Liquid Helium Temperatures, Solid-State Electronics, **35**, no. 4, 1992, pp. 505-512.

[10] Souza, M. de, Flandre D., Doria R. T., Trevisoli R., Pavanello M. A. On the improvement of DC analog characteristics of FD SOI transistors by using asymmetric self-cascode configuration. Solid-State Electronics, **117**, pp. 152-160, 2016.

[11] Doria, R.T., Flandre D., Trevisoli R.D., Souza M. de, Pavanello M.A. Effect of the Back Bias on the Analog Performance of Standard FD and UTBB Transistors-Based Self-Cascode Structures. Semiconductor Science and Technology, **32**, pp. 1-10, 2017.

[12] Assalti, R., D'Oliveira L. M., Pavanello M. A., Flandre D., Souza M. de. Experimental and simulation analysis of electrical characteristics of common-source current mirrors implemented with asymmetric self-cascode silicon-on-insulator n-channel metal-oxide-semiconductor field-effect transistors. IET Circuits, Devices & Systems (Print), **1**, pp. 1, 2016.

[13] Souza, M. de, Flandre, D., Pavanello, M. A. Asymmetric self-cascode configuration to improve the analog performance of SOI nMOS transistors. Int. SOI Conf., Tempe, USA, 2011, pp. 1-2.

[14] ICAP/4 Simulation, Interative Circuit Analysis Program (version 8.11) Bld, 4444, Intusoft, 2011.

[15] Iñiguez, B., Ferreira, L. F., Gentinne, B., Flandre, D. A. Physically-Based C∞-Continuous Fully-Depleted SOI MOSFET Model for Analog Applications. IEEE Transaction Electron Dev., **43**, n.4, pp. 568-575, 1996.

[16] Ferreira R. S, Pavanello M. A. Improved current mirror performance using graded-channel silicon-on-insulator devices in high temperature operation. In: Santos EJP, Ribas RP, Swart J, editors. 19th symposium on microelectronics technology and devices – SBMicro2004. New Jersey: The Electrochemical Society, Inc., 2004. pp. 45-50.

[17] Assalti, R., Flandre, D., Souza, M. de. Influence of Geometrical Parameters on the DC Analog Behavior of the Asymmetric Self-Cascode FD SOI nMOSFETs. JICS. Journal of Integrated Circuits and Systems (Ed. Português), **13**, pp. 1-7, 2018.