Numerical Simulation of the Temperature on the Metallization of an Integrated Circuit and its Impact on Interconnect Lifetime

Rafael O. Nunes, José L. Ramirez, and Roberto L. de Orio

Semiconductors, Instruments and Photonics Dept. – DSIF
School of Electrical and Computer Engineering (FEEC), University of Campinas (UNICAMP)
Av. Albert Einstein 400 – Cid. Univ. Zeferino Vaz, 13083-852 Campinas – SP, Brazil
rafaelon@dsif.fee.unicamp.br

Abstract— **This paper uses a finite element model to investigate the temperature change of the interconnects of an integrated circuit due to the power dissipation of the transistors in the substrate. The temperature of the local interconnect is more significantly affected, exhibiting an increase of 49 K and 34 K, for the Metal 1 and Metal 2, respectively. We discuss the impact of the temperature increase in the electromigration and, as a consequence in the lifetime of the operational amplifier, which demonstrates the importance of considering the metallization temperature distribution in the design stage.**

Index Terms— **BEOL, reliability, electromigration, integrated circuit**

I. Introduction

An accurate analysis of the temperature distribution on the interconnect structures is essential to a better understanding of the integrated circuit (IC) reliability. This can be accomplished, for example, by estimating the temperature of each layer of the back-end-of-line (BEOL) [1]. The temperature estimation becomes more relevant for the new technologies, which have a reduced distance between metal layers and transistors, being the BEOL more affected by temperature change due the self-heating from transistors [2,3].

As the metal layers serve as a thermal path to the heat generated by the transistors, the temperature of the interconnect lines increases. The number of vias, the metal density, the metal thickness and the material contribute to a non-uniform temperature distribution [4-6]. Such a temperature distribution is of great importance to the IC designer and has to be considered for the performance and reliability evaluation at circuit level [7,8].

Under electromigration (EM), the wire is affected by voids, which leads to an increased interconnect resistance or even open circuits [9]. The high temperature accelerates the void evolution [10,11] and leads to faster IC performance degradation, and as a consequence the circuit lifetime reduces. Therefore, the interconnects have to be sized considering the temperature increase to guarantee an adequate circuit operation for a longer period. In this paper we simulate the temperature on the interconnect layers of an integrated circuit using a finite element model (FEM) where the main heat source is positioned in the center or in the corner of the circuit. We compare the results with the temperature estimated with an analytical model. The impact of the temperature change on the mean time-to-failure (MTTF) of an operational amplifier designed in 45 nm technology is evaluated.

II. Temperature Effect on MTTF

Under EM, the interconnect resistance increase degrades the performance of circuits. The $(\Delta R/R_0)_{crit}$ is the resistance ratio value that results in a circuit performance change out of an acceptable range. Then, the time to reach this critical value can be considered the time to circuit failure and expressed by

$$MTTF = \frac{kLA_bT}{D(T)e\,|Z^*|\,\rho_b(T)I}\left(\frac{\Delta R}{R_0}\right)_{crit}, \qquad (1)$$

where $D(T)$ is the diffusion coefficient, Z^* is effective valence, $\rho_b(T)$ is the resistivity, e is the elementary charge, k is the Boltzmann's constant, T is the temperature, I is the electrical current, A_b is the cross-sectional area of the barrier layer and L is the length of the line.

The EM is very sensitive to the temperature. Temperature changes affect the diffusion coefficient and the resistivity of lines. The diffusion coefficient follows an Arrhenius relation with an exponential variation with T given by

$$D(T) = D_0 \exp\left(-\frac{E_a}{kT}\right). \qquad (2)$$

Here, D_0 is a pre-exponential factor and E_a is the activation energy, both dependent on the diffusion mechanisms. The line resistivity, ρ, calculated by

$$\rho = \rho_0\left[1 + \alpha\left(T - T_0\right)\right], \qquad (3)$$

depends on the resistivity ρ_0 in the reference temperature T_0 and the temperature coefficient α of the metal.

Depending on the accuracy of the parameters used to calculate the resistance change, some lines initially classified as critical can be an EM safe line.

A resistance increase of 10% is generally used as a failure criterion, since this variation in global wiring can produce timing errors [12]. Using this percentage increase as a failure criterion has some limitations. First, the actual damage that causes the failure is a function of the initial resistance of the line, which is affected by the temperature and the stress during the fabrication [13]. Second, as the maximum resistance change depends on the width of the line, the current density, and the bias of the transistors, the resistance ratio can assume values higher than 10%, and the circuit continues to operate correctly or, on the other hand, it can be lower than 10% and the circuit does not satisfy the minimum performance.

Digital Object Identifier 10.29292/jics.v15i2.168

III. FEM Model Structure

The finite element method (FEM) is a useful tool to understand the effect of heat transfer from transistors in the silicon substrate. With FEM, we simulate the temperature change (ΔT_{PT}) in the interconnects with the 2D physical model based on the GPDK 45 nm Bulk CMOS technology [14]. The BEOL has 11 layers of interconnects and 10 of vias, with 6% of volume fraction of the vias and 40% of volume fraction of the metal in each layer. Fig. 1 shows the schematic of the model structure with four metal layers, nonetheless we simulate the eleven layers. A very low thermal conductivity epoxy resin isolates gold bond wires which are connected to the packaging. The thermal conductivity of the materials, dimensions of the vias and the metal layers, etc. are described in Table I.

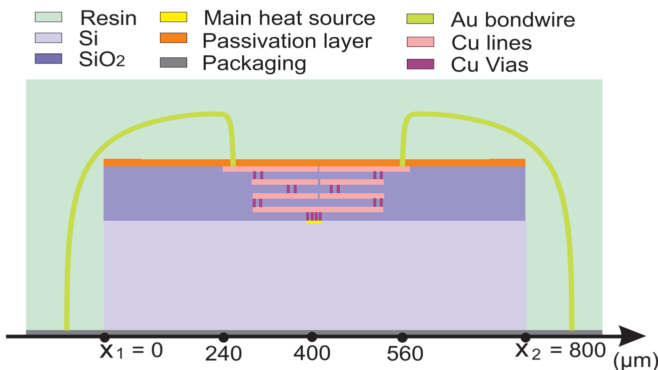

Fig. 1: Schematic BEOL structure with four layers of metallization and vias.

Table I. Parameters used in the BEOL model simulated in the COMSOL.

Description	Value	Unit
Si thickness	20	μm
Chip's width	800	μm
Contact's thickness	150	nm
Via1 and Via2 thickness	150	nm
Vias3 to Via9 thickness	180	nm
Via10 and Via11 thickness	1000	nm
Metal1 and Metal2 thickness	150	nm
Metal3 to Metal8 thickness	180	nm
Metal9 to Metal11 thickness	1000	nm
Volume fraction of metal	0.4	n.a.
Contact width	65	nm
Via12 width	65	nm
Via23 and Via34 width	70	nm
Via45 to Via67 width	140	nm
Via78 and Via89 width	400	nm
Via910 and Via1011 width	800	nm
Volume fraction of via	0.06	n.a.
Distance between vias	500	nm
Heat source thickness	60	nm
Heat source width	2000	nm
Bondwire width	2000	nm
Packaging thickness	100	nm
Passivation thickness	5	nm
Resin thickness	80	μm
Si - Thermal conductivity [16]	130	W/(K·m)
Cu bulk - Thermal conductivity [15]	400	W/(K·m)
Acrylic - Thermal conductivity	0.18	W/(K·m)
SiO2 - Thermal conductivity [16]	1.4	W/(K·m)

IV. BEOL Temperature Simulation

Based on the FEM model, we investigate the temperature on the BEOL with the transistors' power dissipation of 400 W/m. The reference temperature is 293 K. Two studies are carried out: a) first we investigate the ΔT_{PT} in the metal layers, b) we evaluate the mean-time-to-failure (MTTF) change with the temperature.

Fig. 2 illustrates a temperature distribution on a chip with a length from x_1 to x_2 and a width from y_1 to y_2. In the first case, we simulate the thermal distribution on the BEOL from x_1 = 240 μm to x_2 = 560 μm and y = 200 μm with the primary heat source in the center of the chip at x = 400 μm and y = 200 μm. Here, the primary heat source in the center of the chip produces heat that flows into the BEOL and changes the temperature of the lines. The transistors occupy a small region of 2 μm, equivalent to 0.25% of the width of the chip, resulting in a higher temperature in a narrow central region of the metal lines. In a typical integrated circuit, the transistors occupy a larger area, and as a consequence, the temperature distribution is more homogeneous along the lines.

The temperature in regions further away from the heat source, in particular at the corners A, B, C, and D, undergoes a lower change. Besides the power dissipated by the transistors, the temperature change in each metallic layer (ΔT_{PT}) is a function of thermal conductivity of the several materials, the geometry of the layers, and the number of vias.

Fig. 3 shows the temperature of lines from Metal 1 to Metal 11 from x=240 to 560 μm. The interconnects of the local layers near the primary heat source operate under the highest temperatures. As expected, the temperature near the corners A, B at x = 240 μm and C, D at x = 560 μm are significantly lower than in the center of the chip. The result considers the vias distributed at the end of the metallic layers, in a formation named quasi-manhattan structure [17]. The concentration of the vias near the heat source between the layers M2-M3, M4-M5, M6-M7, M8-M9 and M10-M11 results in the same ΔT_{PT} for the lines of these layers.

In a second case, the primary heat source is near one of the chip's corners, shown in Fig. 4. With the primary heat source near the corner A, the highest ΔT_{PT} of 57 K is at x = 280 μm, y = 150 μm and a lower ΔT_{PT} at the other corners, as shown in Fig. 5. Observe that the primary heat source sized

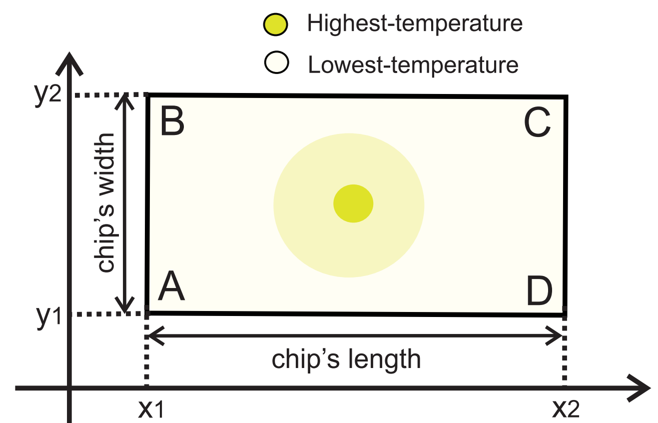

Fig. 2: Top view of the temperature distribution on a chip with a primary heat source in the center.

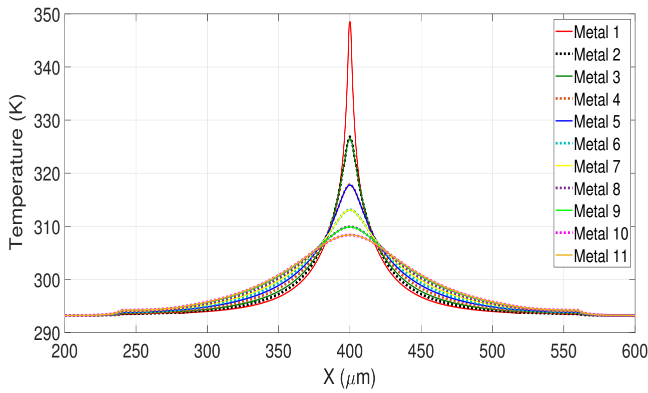

Fig. 3: Temperature on the BEOL with the heat source in the center of the chip at x = 400 μm and the power dissipation of 400 W/m.

near the extremity results in a temperature of 333 K and 324 K in M2 and M3, equivalent to a ΔT_{PT} of 33 K and 24 K, respectively. Differently from the first case, the others pairs M4-M5, M6-M7, M8-M9 and M10-M11 also have a different ΔT_{PT} due to the position of the vias in the extremity of the metal layers, and the primary heat source placed in an intermediary position near the corner A. The regions near the epoxy resin result in a large variation of the temperature due to the differences in the thermal conductivity of the BEOL and the epoxy material.

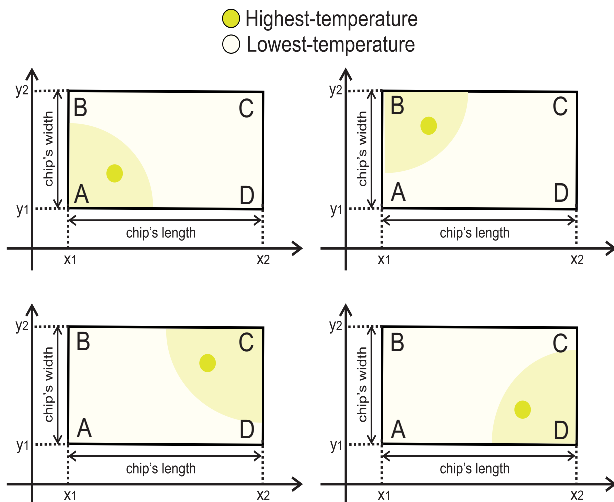

Fig. 4: Temperature distribution with the primary heat source near the corners of the chip.

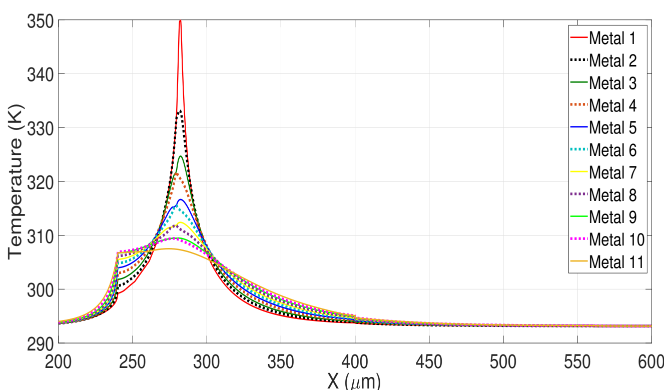

Fig. 5: Temperature on the BEOL with the primary heat source near the corner A of the chip at x = 280 μm and the power dissipation of 400 W/m.

In the third case, the center and regions near the corners have heat sources with the same power dissipation of 400 W/m, as illustrated in Fig. 6. Fig. 7 shows the temperature along the BEOL with the heat sources at the center at x = 400 μm, y = 200 μm and near the corners A and D, at x = 280 μm, y = 150 μm and at x = 520 μm, y = 150 μm. The inclusion of more heat sources increasing the power dissipated in the FEOL, increases the temperature on the BEOL as observed in the Metal 10 layer, which has the maximum temperature of 311 K, equivalent to ΔT_{PT} of 11 K, 4 K higher than the case 2, and 3 K higher than the case 1. Note that the Metal 2 in the position 280 μm has a temperature of 334 K, 5 K higher than the Metal 2 positioned in 400 μm, in the center of the chip, indicating the influence of the position of the vias in the thermal distribution of the chip.

Fig. 8 shows a comparison between the maximum temperature change on each metal layer estimated with [18] and simulated with the primary heat source at the center, at the corner and at the center and the corner (Fig. 3, 5 and 7). A large temperature difference between two consecutive layers is observed in the three curves. The results indicate that in Metal 1 the ΔT_{PT} is near to the simulated temperature change in Fig. 3, 5 and 7. The small differences in the ΔT_{PT} has a relation with the different materials used in the simulation, while the temperature estimated considers the effective conductivity from the Si and Cu. The distribution of the vias and the heat source position affect the temperature, evidenced by the differences between the temperatures simulated in Figs. 3 and 5.

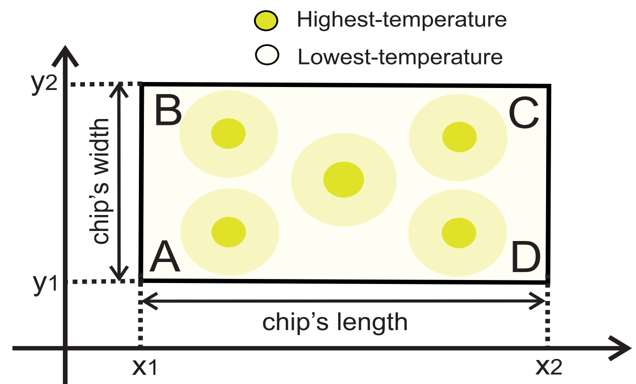

Fig. 6: Temperature distribution with heat sources at the center and near the corners of the chip.

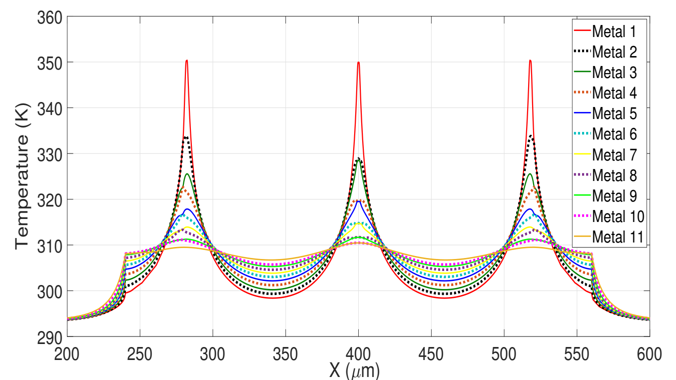

Fig. 7: Temperature on the BEOL with the primary heat source near the corners A and D at x = 280 μm and x = 520 μm, respectively and in the center of the chip at x = 520 μm, with P_T = 400 W/m.

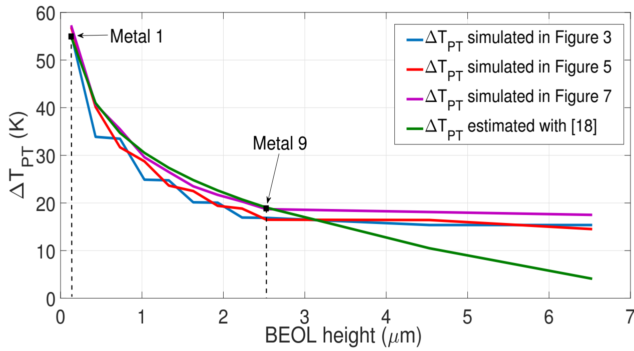

Fig. 8: Comparison between the maximum Δ_{PT} estimated with [18] and simulated with a single heat source from Figure 3, 5 and with multiple heat sources from Figure 7.

V. MTTF CHANGE WITH TEMPERATURE

To evaluate the impact of the ΔT_{PT} in $\Delta R/R_0$ and in the circuit lifetime, we simulate 176 paths from interconnects of an operational amplifier shown in Fig. 9. The length and the width of the paths vary from 2 μm to 123 μm and from 0.06 μm to 1.7 μm, respectively, as illustrated in the histograms from Figure 10(a) and Figure 10(b). Here, the length is the largest metal line of an interconnect containing the path. The lines are designed with 3 metal layers, where 6 paths are Metal 3, 33 paths are Metal 1 and 137 paths are Metal 2, as shown in Figure 10(c). The resistance of each path is given in Figure 10(d). The histograms in Figure 10(e) and Figure 10(f) indicate the current density through the lines in relation to the maximum current density of 2 mA/μm for static and DC simulations. Note that some paths have the current density ratio (J/J_{max}) higher than 1 and operate under a current density above the maximum indicated by the technology.

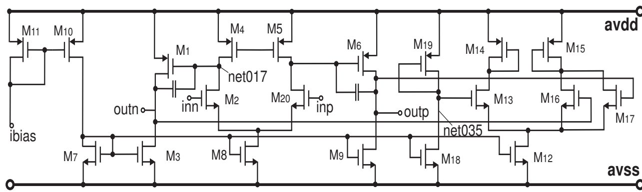

Fig. 9: Operational amplifier used to evaluate the EM effect of the lines resistance.

The average power dissipated per transistor is 75 μW, equivalent to a normalized power of 416 W/m, for the transistor's pitch of 180 nm. Fig. 11 shows the ΔT_{PT} of 61 K, 48 K and 42 K for the Metal 1, Metal 2 and Metal 3 respectively. This results in a temperature of 361 K, 348 K, and 342 K, for a reference temperature of 300 K. The importance to estimate the temperature by layer is evident when observing the temperature in Metal 1, which is 19 K higher than the estimated temperature in the Metal 3 layer. Although the local layers have elevated temperature, ICs can support higher temperatures. A chip designed for an industrial application, for example, supports maximum temperatures of 398 K [19].

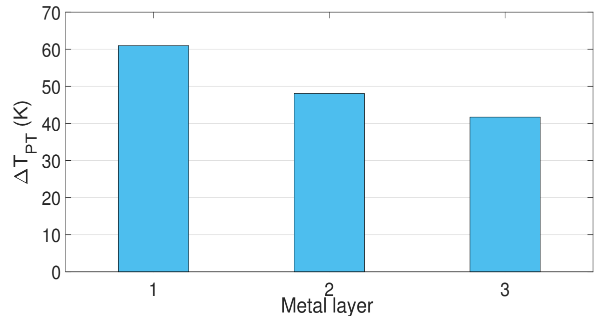

Fig. 11 (a) ΔT_{PT} in metal layers.

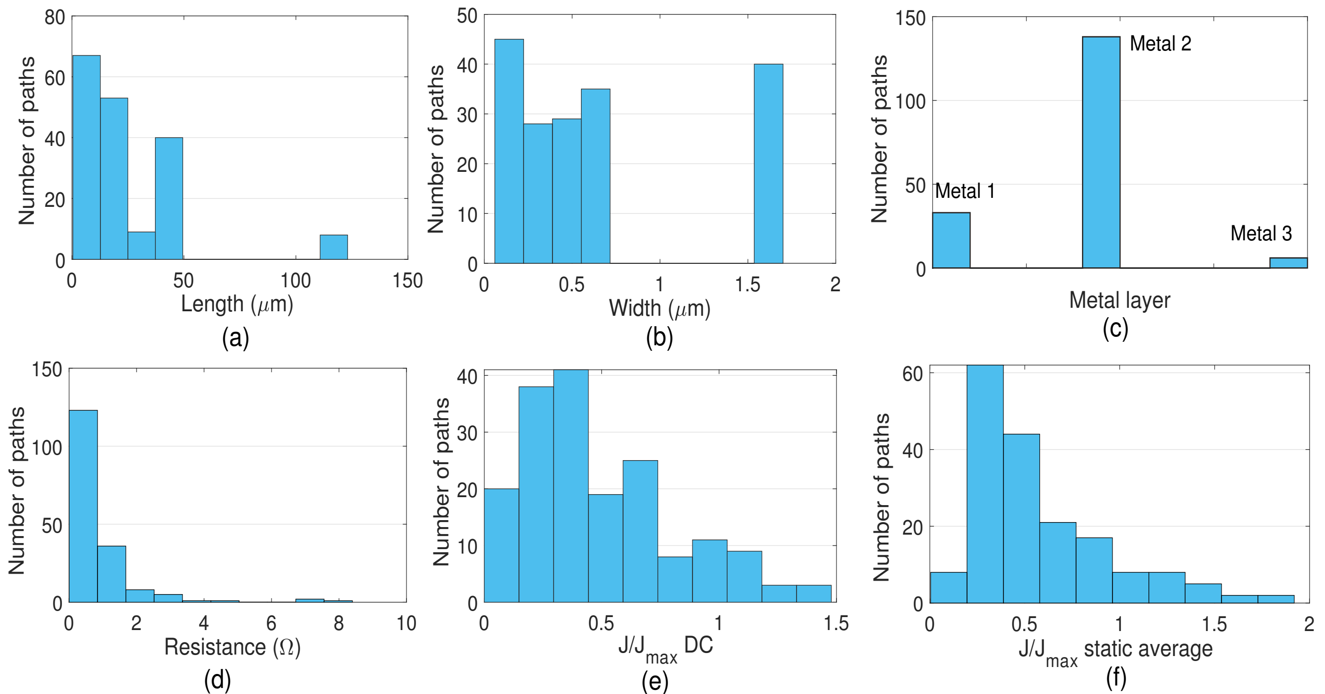

Fig. 10: Parameters to evaluate the lines of an operational amplifier: (a) Length. (b) Width. (c) Metal layer. (d) Resistance. (e) Current density ratio in DC operation. (f) Current density ratio in static operation.

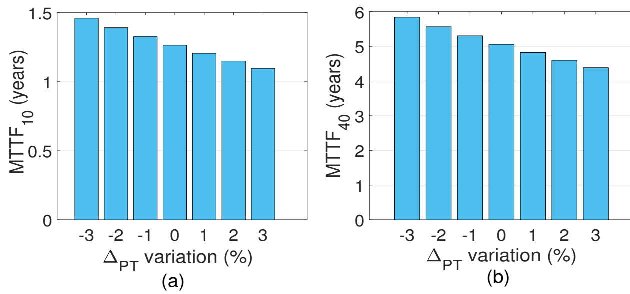

Fig. 12: (a) Time to the resistance of the lines increase 10% with a ΔT_{PT} variation from -3% to 3%. (b) Similar analysis with the critical resistance of the lines of 40%.

Fig. 12 shows the time to the first ten interconnect paths failure, i.e., the time to ten paths suffers a critical resistance change due to EM. The MTTF_{10} in Fig. 12(a) means that the critical resistance is 10%, while in Fig. 12(b) the MTTF_{40} represents the critical resistance of 40%. Observe in Fig. 12(a) that a variation from -3% to 3% in ΔT_{PT} changes the MTTF_{10} from 1.45 to 1.2 years. In Fig. 12(b), the expected lifetime varies from 5.8 to 4.3 years for the same ΔT_{PT} variation. A reduction of some degrees in the temperature improves the MTTF of the circuit considerably. This analysis considers that the operational amplifier works full time. For a workload of 50%, the lifetime of the lines doubles.

A high temperature affects the performance of a circuit leading to changes in the transistors' operation and to increase the metal lines' resistance. The lines resistance is expected to be larger as the dimensions reduce in each new technology. However, in addition, the temperature increases the lines resistance even more, which strongly affects the power consumption, operation frequency, and signals delay of circuits. The temperature increase due to the Joule heating and to the dissipated power from transistors makes the circuit operation slower.

An adequate estimation of the temperature distribution on the circuit and on the interconnect structure is essential to a better understanding of the interconnect reliability. This is accomplished by estimating the temperature of each layer of the BEOL. The temperature estimation becomes more relevant for the new technologies which have reduced pitches and are more compact, so the BEOL experiences a higher temperature due to self-heating of the transistors. Such a temperature distribution is of great importance to the IC and layout designer, and has to be considered for the performance evaluation at circuit level. Indeed, the use of FinFET and SOI is particularly problematic due to the increasingly severer self-heating effect, because the heat dissipation to the bulk is reduced [20,21].

VI. Conclusion

We investigated the temperature increase of the interconnects due to the power dissipation from transistors using numerical simulations based on a FEM model for the 45 nm technology. The large differences of temperature in the metal layers indicate that the local interconnects are more prone to failure due to EM, considering only the temperature.

The higher temperature accelerates the electromigration and reduces the lifetime of an integrated circuit. We evaluated the reduction of the mean time-to-failure of an operational amplifier, a significant reduction of 31% with the temperature increase of 6 K was observed. The additional temperature has to be considered in the design stage to allow sizing the wires to guarantee the reliability of the circuit.

Acknowledgment

This study was financed in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brasil (CAPES) - Finance Code 001.

References

[1] Nunes, R. O., and de Orio, R. L. Effect of Lines and Vias Density on the BEOL Temperature Distribution. JICS (2019), 14(2), 1-9.
[2] Tu, K. N., Liu, Y., and Li, M. Effect of Joule heating and current crowding on electromigration in mobile technology. App. Phys. (2017),1-4.
[3] Choi, J., Monga, U., Park, Y., Shim, H., Kwon, U., Pae, S., and Kim, D. S. Impact of BEOL Design on Self-heating and Reliability in Highly-scaled FinFETs,SISPAD IEEE (2019), 1-4.
[4] Pop, E., Sinha, S., and Goodson, K. E. Heat generation and transport in nanometer-scale transistors. Proc. of the IEEE (2006), 1587-1601.
[5] Chandra, R., Srinivasan, A., and Gopal, N. (2010). U.S. Patent No. 7,823,102. Washington, DC: U.S. Patent and Trademark Office.
[6] Nunes, R. O., Bohorquez, J. L. R., and De Orio, R. L. Analysis of Vias Position on the BEOL Temperature Distribution. LAEDC IEEE (2019), 1-4.
[7] Rahimipour, S., Zhang, R., Wang, K., Skadron, K., Rokhani, F. Z. B., and Stan, M. R. MTTF Enhancement Power-C4 Bump Placement Optimization. IEEE Trans.on VLSI Systems (2019), 1633-1639.
[8] Lu, T., Yang, Z., and Srivastava, A. (2016, March). Electromigration-aware placement for 3D-ICs. ISQED IEEE (2016), 35-40.
[9] Nunes, R. O., and de Orio, R. L. Evaluating the impact of electromigration on the integrated circuit performance. SBMicro IEEE (2017), 1-4.
[10] Sun, Z., Sadiqbatcha, S., Zhao, H., and Tan, S. X. D. Accelerating electromigration aging for fast failure detection for nanometer ICs. ASP-DAC IEEE (2018), 623-630.
[11] Lamontagne, P., Ney, D., Doyen, L., Petitprez, E., and Wouters, Y. Resistance trace modeling and electromigration immortality criterion based on void growth saturation. IRPS IEEE (2010), 922-925. IEEE.
[12] Lloyd, J. R. Electromigration for designers: An introduction for the non-specialist. TechOnLine (2020).
[13] Ogurtani, T. O., and Oren, E. E. Computer simulation of void growth dynamics under the action of electromigration and capillary forces in narrow thin interconnects. Journal of Appl. Phys. (2001), 1564-1572.
[14] Cadence. GPDK 45 nm Mixed Signal Process Specgpdk045 drc manual, revision 1.0 edition, 2009.
[15] Liu, W., Yang, Y., and Asheghi, M. Thermal and electrical characterization and modeling of thin copper layers. ITHERM IEEE (2006), 1171-1176.
[16] Fang, A., Jones, R., Park, H., and Sysak, M. (2009). U.S. Patent No. 7,639,719. Washington, DC: U.S. Patent and Trademark Office.
[17] Nunes, R. O., Bohorquez, J. L. R., and De Orio, R. L. Analysis of Vias Position on the BEOL Temperature Distribution, LAEDC IEEE, 1-4.
[18] Ahn, W., Zhang, H., Shen, T., Christiansen, C., Justison, P., Shin, S., and Alam, M. A. A predictive model for IC self-heating based on effective medium and image charge theories and its implications for interconnect and transistor reliability. IEEE Trans. on Electron Devices (2017), 3555-3562.
[19] Pan, S., and Makinwa, K. A. A 0.25 mm 2-Resistor-Based Temperature Sensor With an Inaccuracy of 0.12 C (3σ) From -55 C to 125 C. IEEE Journal of Solid-State Circuits (2018), 3347-3355.
[20] Zhao, Y., and Qu, Y. Impact of Self-Heating Effect on Transistor Characterization and Reliability Issues in Sub-10 nm Technology Nodes. IEEE Journal of the Electron Devices Society (2019), 829-836.
[21] Gupta, C., Gupta, A., Vega, R. A., Hook, T. B., and Dixit, A. Impact of Hot-Carrier Degradation on Drain-Induced Barrier Lowering in Multifin SOI n-Channel FinFETs With Self-Heating. IEEE Trans. on Electron Devices (2020), 2208-2212.