Physical Insights on the Dynamic Response of SOI n- and p-Type Junctionless Nanowire Transistors

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***Abstract*— This work evaluates, for the first time, the roles of the intrinsic capacitances and the series resistance on the dynamic response of p- and n-type Junctionless Nanowire Transistors. The dynamic behavior evaluation will be carried out through the analysis of the limitation imposed by such parameters on the maximum oscillation frequency (f_{max}). In the sequence, it will be shown the impacts of f_{max} and the carriers' transit time on the minimum switching time presented by JNTs. It has been observed that Junctionless devices present lower f_{max} than inversion mode transistors of similar dimensions due to higher resistance and lower transconductance. However, the intrinsic capacitances of such devices are smaller than the inversion mode ones, which compensates part of the degradation on f_{max} caused by the other parameters. Besides that, it is shown that transit time can be important on the dynamic behavior of long devices, but plays a negligible role in shorter ones.**

***Index Terms*— Junctionless Transistors; Transient Response; Transit Time.**

I. Introduction

The continuous scaling of field effect transistors along the last decades pushed by Moore's Law [1] has led to the fabrication of extremely shorter devices, in which several second order effects have become increasingly prominent. The most important of such phenomena consists in the short channel effects (SCEs), where a significant portion of the depletion charge in the channel region is controlled by the depletion regions from source to channel and drain to channel junctions. Such effects are responsible for the degradation in the subthreshold slope of the devices as well as for the threshold voltage (V_{TH}) roll-off. The reduction on the occurrence of short channel effects can be reached through devices with a better capacitive coupling, which can be attained through the application of multiple gate architectures such as triple gate FinFETs [2] and nanowires [3] instead of planar ones. In sub-16 nm nodes, such devices are widely used to meet the ITRS roadmap requirements [4].

However, another important bottleneck of sub-16 nm nodes consists in the formation of source and drain junctions. The doping concentration must vary several order of magnitude in a few nanometers, which requires extremely precise thermal budget [5] since variations on the fabrication process may lead to the source/drain dopants diffusion into the channel [5]. For that reason, a recent developed device so-called Junctionless Nanowire Transistor (JNT), whose source, drain and channel regions present the same doping type and concentration, was developed [6, 7]. It has usually been fabricated in SOI technology [6], although there are papers showing its implementation in conventional bulk wafers [8] and works similarly to accumulation mode transistors [9]. The longitudinal section of both an n-type inversion mode (IM) and an n-type JNT fabricated in SOI technology are shown in Fig. 1 (A) and (B), respectively.

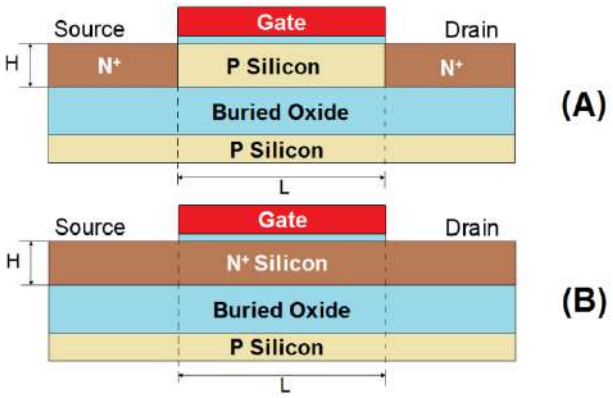

Fig. 1. Longitudinal sections of (A) an n-type IM transistor and (B) an n-type JNT.

By the appropriate choosing of the gate material, the difference between gate and silicon active layer workfunctions induces a depletion region inside the silicon. In the case of n-type devices, for gate voltages (V_{GS}) below the threshold one (V_{TH}), the entire silicon layer becomes depleted. As V_{GS} is increased above V_{TH}, the depletion is reduced and a neutral conduction path is formed close to the center of the silicon layer, which gives rise to a bulk conduction. Considering the device working at low drain bias (V_{DS}), operating in linear regime, this path becomes larger with the increase of V_{GS} and covers the whole silicon thickness when V_{GS} reaches the flatband voltage (V_{FB}). If V_{GS} is increased above V_{FB}, there is the accumulation of majority carriers in a superficial layer, inducing the formation of another current component, which contributes for the total drain current (I_{DS}) presented by the devices [7, 8].

Along the last years, several groups have dedicated efforts to the research of JNTs. It can be found in the literature several papers about the performance of Junctionless transistors in terms of short channel effects [10], analog and digital properties [11, 12] and modeling [13-16]. However, only a few works have addressed the dynamic response of such devices. In [17], it is presented a study about the off-current transient of JNTs, in which some curves of the devices switching as a function of time are used to estimate the appropriate bias conditions for measuring carriers lifetime whereas [18] presents a quasi-static model for the

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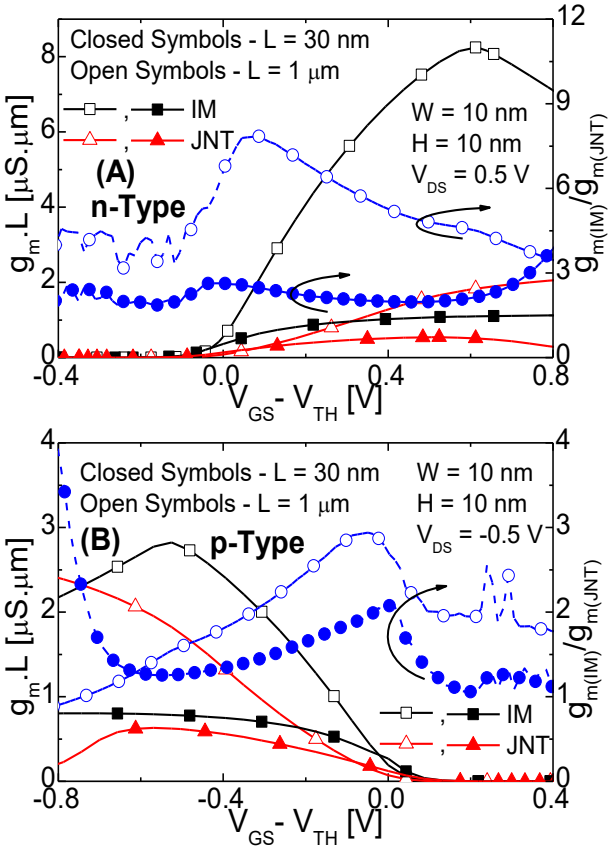

Fig. 2 Simulated g_m normalized by the channel length (left axis) and the g_m ratio between IM and JNTs (right axis) as a function V_{GS}-V_{TH} for (A) n-type and (B) p-type devices with different channel lenghts.

transcapacitances of triple gate JNTs aiming at their dynamic operation.

Recently, in [19] it was presented a study dealing with the switching time (t_{switch}) of JNTs, which is responsible for limiting the frequency of operation of the devices, being of extreme importance in both digital and RF CMOS circuits. The minimum theoretical t_{switch} is associated to the carriers' transit time ($t_{transit}$), defined as the time taken by the carriers to flow from the source to the drain of the devices. Anyway, in real short channel transistors, the minimum switching time is usually limited by the time required to charge/discharge the capacitances associated to them, given by $t_{min} = 1/f_{max}$. In [19], the t_{switch} of JNTs is compared to the one shown by IM transistors considering the effects of the the gate to source (C_{gs}) and gate to drain (C_{gd}) capacitances, besides the transconductance (g_m), which also plays an important role in the dynamic behavior of the devices. However, the analysis is only carried out for n-type devices and the impact of the series resistance (R_S) on f_{max} is not considered.

For that reason, in this work, the study performed in [19] is extended for p-type devices and effect of R_S is taken into account. As the influence of R_S on the dynamic behavior of the devices can mask the impact of the intrinsic capacitances and g_m on f_{max} and t_{min}, the analysis is performed for both JNTs and IM devices, initially, neglecting R_S in section II and then, accounting for series resistance in section III, respectively. A comparison of t_{min} with the minimum theoretical t_{switch} given by the transit time is presented in section IV whereas, the main conclusions of the work are pointed out in section V. It is worth mentioning that, due to the extremely lower values presented by intrinsic capacitances of shorter devices, the analysis could not be performed experimentally and was based on three-dimensional numerical simulations and modeling.

II. Intrinsic Capacitances

Along the dynamic model development for a triple gate JNT presented in [18], it is shown that a four terminal triple gate JNT presents sixteen intrinsic capacitances and transcapacitances. All of them should be accounted for precise estimation of the dynamic operation of such devices. However, according to [20], the maximum oscillation frequency of a MOSFET can be written simply as a function of C_{gs} and C_{gd} as states expression (1).

$$f_{max} \approx \frac{f_c}{2\left(1+\frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d(R_g+R_s)+\frac{C_{gd}}{2.C_{gs}}\left(R_s.g_m+\frac{C_{gd}}{C_{gs}}\right)}}, \qquad (1)$$

where g_m is the transconductance, g_d is the output conductance, R_g is the gate access resistance and f_c the unity-gain frequency, given by $g_m/2\pi.C_{gs}$. In a first approach, R_S and R_g will be neglected in the calculus of f_{max}, in order to distinguish the effects of the intrinsic capacitances to the one of the series/access resistances. It is worth mentioning that if both IM and JNTs are fabricated through the same process, the series resistance of both devices will be similar. By neglecting R_S and R_g, (1) can be rewritten as (2)

$$f_{\max(C_{gs},C_{gd})} \approx \frac{g_m}{\frac{4\pi C_{gd}}{\sqrt{2}}\left(1+\frac{C_{gd}}{C_{gs}}\right)}. \qquad (2)$$

The effects of g_m, C_{gs} and C_{gd} on the maximum oscillation frequency have been addressed through 3D numerical simulations of IM and JNTs performed in the software Sentaurus Device [21]. The simulated devices present physical characteristics similar to the experimental ones whose transfer characteristics are shown in [22]. IM devices and JNTs present channel doping concentrations of 10^{15} cm^{-3} and 10^{19} cm^{-3}, respectively. The active silicon layer presents thickness of 10 nm, buried oxide of 100 nm and effective oxide thickness of 2 nm. Devices of two fin widths (10 and 20 nm) were considered in the simulations as well as several channel lengths varying from 30 nm up to 10 μm. In a first moment, in order to reduce R_S, the source/drain regions extension was set to 1 nm. Models accounting for the bandgap narrowing, SRH recombination, low field mobility, longitudinal and vertical electron fields as well as quantum mechanical effects have been considered along of all the simulations.

Fig. 2 presents the curves of the normalized transconductance (left axis) as a function of the gate voltage overdrive ($V_{GS} - V_{TH}$) for IM and JNTs with different channel lengths. The devices were biased at $|V_{DS}| = 0.5$ V as this value is close to the minimum applied in analog circuits and results in f_{max}

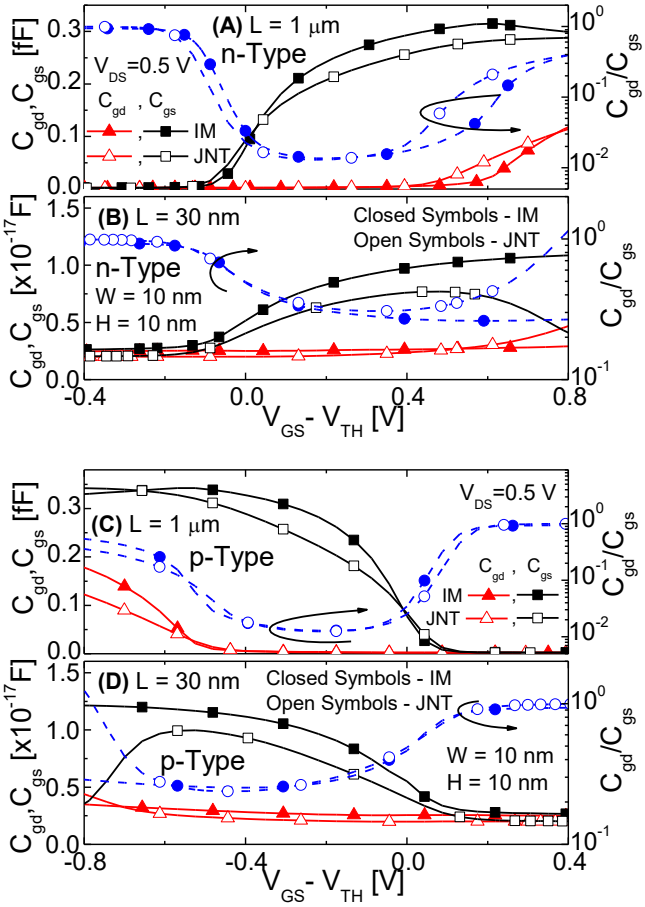

Fig. 3 Gate to drain (C_{gd}) and gate to source (C_{gs}) capacitances as a function of V_{GS}-V_{TH} for n-type ((A) and (B)) and p-type ((C) and (D)) Junctionless and inversion mode devices of different L.

lower than the one shown for larger V_{DS}. The transconductance has been normalized by L in order to allow for a comparison of devices with different dimensions. As one can perceive from Fig. 2 (A), n-type IM devices present larger g_m than JNT of similar dimensions along the entire $V_{GS} - V_{TH}$ range. This is clearer demonstrated in the right axis of Fig. 2 (A), which presents the ratio between the transconductance of both devices ($g_{m(IM)}/g_{m(JNT)}$). It can be seen that IM transistors presents g_m at least twice larger than the JNT counterpart for the entire V_{GS} interval, although it can reach eight times. These results are in accordance to different works from literature [5, 7, 8], which have attributed the lower g_m of JNTs to its reduced mobility derived from the heavily doped silicon layer. The larger normalized transconductance presented by IM devices with respect to JNTs is less pronounced for p-type transistors as it can be observed in Fig. 2 (B), since the holes' mobility is smaller than the electrons' one. Thus, the $g_{m(IM)}/g_{m(JNT)}$ ratio remains between 1 and 3 for almost the entire $V_{GS} - V_{TH}$ range for both channel lengths and decreases with L reduction.

The curves of the intrinsic capacitances C_{gs} and C_{gd} are shown in Fig. 3 (left axis) as a function of $V_{GS} - V_{TH}$ for IM and JNTs of different L biased at $|V_{DS}| = 0.5$ V. According to the figure, C_{gs} is the dominant capacitive component for the determination of f_{max}, as demonstrated in in the right axis of Fig. 3, which plots C_{gd}/C_{gs}. For practically the entire V_{GS} range, C_{gd} is smaller than C_{gs} independently on the device type. In the $|V_{GS} - V_{TH}|$ interval between 0 and 0.5 V, the difference between both capacitances can reach more than 50 times in longer devices and 7 times in the shorter one in both n- and p-type devices.

Despite presenting the same gate stack, one can note a difference between the capacitances in IM and JNTs. Above threshold, C_{gs} of the IM transistor is larger than the one shown by JNTs of similar dimensions. This phenomenon was previously observed in [23] and, in longer devices, can be attributed uniquely to the different conduction mechanisms of IM and JNTs. From threshold up to $V_{GS} - V_{TH} = 0.8$ V in the case of n-type devices (Fig. 3 (A) and (B)), and up to $|V_{GS} - V_{TH}| = 0.75$ V, in the case of p-type ones (Fig. 3 (C) and (D)), the JNT is operating in partial depletion where the conduction occurs in the body of the transistor. In this case, C_{gs} is given by the series association of the gate capacitance and the one of the depletion region formed in the silicon layer between gate dielectric and conduction path, making C_{gs} lower in JNTs. When the JNT reaches the flatband ($|V_{GS} - V_{TH}| > 0.8$ V and > 0.75 V in n- and p-type transistors, respectively), a superficial accumulation layer is formed and C_{gs} of both devices tends to the half of the gate dielectric capacitance.

As the channel length of the devices is reduced, it is possible to observe a reduction in C_{gs} in both devices due to its proportionality to the gate area. Anyway, for 30 nm-long devices, quantum and short channel effects also present strong influence on C_{gs}. The occurrence of quantum effects lead to the formation of the channel farer from the interface, reducing C_{gs}. As JNTs present bulk conduction for practically its entire operation range, the effect of quantum confinement is much more pronounced in IM transistors. Contrarily, the incidence of short channel effects induces an increase in the intrinsic capacitances of the devices as stated in [18]. Considering that the susceptibility of JNTs to SCEs is lower than the one of inversion mode transistors [10], the increase of C_{gs} in these devices is less pronounced. The superposition of SCEs and quantum effects associated to the different conduction regimes of the devices results in C_{gs} of shorter JNTs about 20-25% lower to the ones presented by IM devices at $|V_{GS} - V_{TH}| = 0.5$ V. In terms of C_{gd} it is smaller up to $|V_{GS} - V_{TH}| = 0.4$ V and up to 0.7 V in 30 nm-long n- and p-type JNTs, respectively and up to $|V_{GS} - V_{TH}| = 0.4$ V for longer devices, independently on its type.

When the ratio between C_{gd}/C_{gs} is evaluated, it is possible to observe from Fig. 3 that this parameter presents a minimum in the $|V_{GS} - V_{TH}|$ range from 0 up to 0.6V in both IM and JNTs, which consists in the best interval to bias the devices, concerning intrinsic capacitances. It can also be observed that JNTs and IM transistors present similar C_{gd}/C_{gs} along practically the entire $V_{GS} - V_{TH}$ range. Therefore, the reduced C_{gd} obtained in JNTs and the similar C_{gd}/C_{gs} exhibited by both devices are expect to partially compensate the degradation of g_m observed in JNTs in the calculus of f_{max}.

The maximum oscillation frequency of the devices has been obtained through the application of transconductance data from Fig. 2 and the capacitance ones from Fig. 3 to expression (2). f_{max} and the minimum oscillation time are presented in Fig. 4 (A) and (B), respectively, for n-type de-

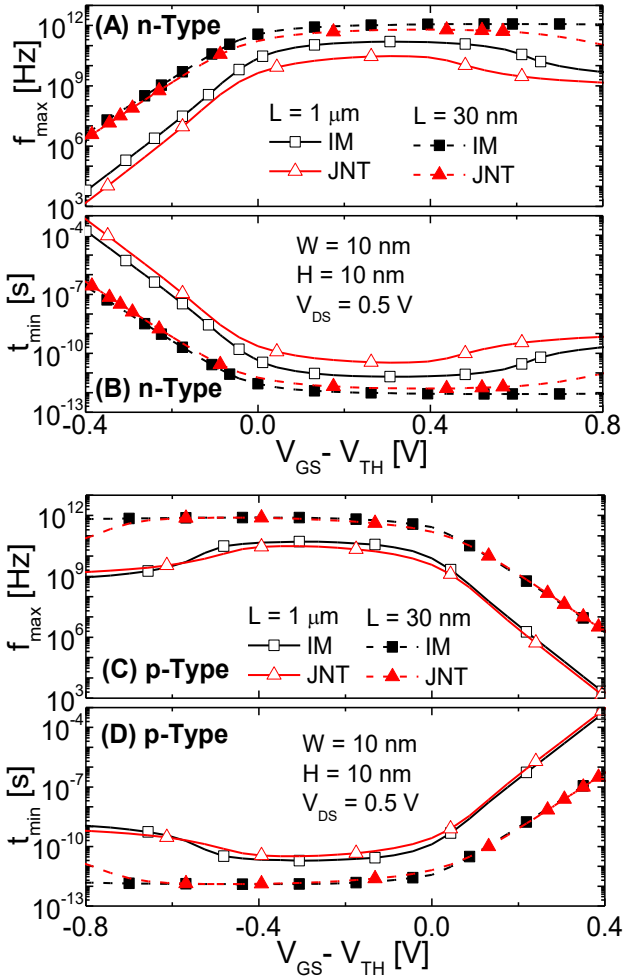

Fig. 4. Maximum oscillation frequency ((A) and (C) for n- and p-type devices, respectively) and minimum oscillation time ((B) and (D)) for IM transistors and JNTwith different L neglecting R_S.

vices and in Fig. 4 (C) and (D), respectively, for p-type ones. Both curves are presented as function of $V_{GS} - V_{TH}$ for V_{DS} = 0.5 V. As shown in Fig. 4 (A), f_{max} of n-type shorter JNTs is in the order of 620 GHz in the $V_{GS} - V_{TH}$ range between 0 and 0.5 V whereas IM devices of similar dimensions present $f_{max} \approx$ 1.1 THz in the same $V_{GS} - V_{TH}$ range. Considering that g_m of JNTs is about 2.5-3 times lower than the one exhibited by IM devices in such gate voltage interval, it can be concluded that the reduced intrinsic capacitances of JNTs have partially compensated their g_m degradation. The same behavior is observed for longer devices. In the case of p-type ones, as the larger g_m is not so pronounced due to the lower mobility of holes, f_{max} of longer devices is slightly larger in IM with respect to JNTs in practically the entire gate voltage range (at $V_{GS} - V_{TH}$ = -0.4 V, $f_{max} \approx$ 780 GHz for IM devices and ≈ 610 GHz for JNTs). It is interesting to note that the higher channel doping concentration presented by JNTs has led to a lower mobility, which is much more evident in n-type devices than in p-type ones, making f_{max} very similar in n- and p-type devices.

From Fig. 4, it can be seen that, by neglecting the effect of the series/access resistance, shorter channel n-type IM and JNTs have presented minimum oscillation times of 0.9 ps and 1.6 ps at $V_{GS} - V_{TH}$ = 0.35 V and 0.40 V, respectively. Although such values give an idea about the roles of g_m and intrinsic capacitances on f_{max} and t_{min}, they cannot be considered as a real estimative of the minimum switching time of the devices since they are expected to be severely degraded by the effect of series/access resistance, which is addressed in section III.

Table I. Series resistance extracted through the method of [24] from simulated JNTs and IM devices with different physical characteristics.

Device		R_S (kΩ)
IM	n-Type	5.59
($N_{S/D}$=5x10^{20}cm^{-3})	p-Type	6.73
JNT	n-Type	62.61
($N_{S/D}$=1x10^{19}cm^{-3})	p-Type	61.26
JNT	n-Type	7.44
($N_{S/D}$=5x10^{20}cm^{-3})	p-Type	8.23

III. Series Resistance

In other to give a more real insight on the minimum switching time shown by IM and JNTs, the effect of the series resistance has been evaluated. Although the gate access resistance can reduce the amplitude of the input signal, leading to the degradation of f_{max}, the influence of this parameter in the output characterisctics of the devices is much smaller than the one of R_S and can be neglected. Besides that, R_S affects the output conductance of the transistor, which needs to be taken into account in the f_{max} analysis. The series resistance has been extracted from simulated curves through the method proposed in [24]. For the analysis of devices considering the effect of R_S, the simulated structures present 50 nm-long source/drain extensions with doping concentrations ($N_{S/D}$) of 5x10^{20} cm^{-3} and 1x10^{19} cm^{-3} in IM and JNTs, respectively. In a second set of simulations it was considered JNTs with a source/drain doping concentration of 5x10^{20} cm^{-3} as suggested in [22, 25] in order to reduce the effect of R_S in the output characteristics of the devices, whereas channel doping concentration was kept equal to 1x10^{19} cm^{-3}.

Table 1 presents the extracted values of the series resistance for IM and JNTs with different characteristics. As one can observe, when both IM and JNTs present similar source/drain doping concentration, the absolute value of the series resistance in the JNT is about 25% larger than the one presented by the IM device. However, as the results of the applied method can be contaminated by the channel resistance and this component is higher in JNT with respect to IM transistors, the increase observed in R_S is certainly overestimated. On the other hand, when the JNT has a lower $N_{S/D}$, R_S is about 9-10 times superior to the one shown by IM devices, which can affect significantly f_{max}.

Fig. 5 shows the curves of f_{max} and t_{min} as a function of $V_{GS} - V_{TH}$ for both devices taking into consideration the effect of R_S. This analysis has been perfomred considering the worst case, in which the source/drain doping concentration of the JNTs is lighter than the one of IM transistors. In this case, f_{max} was calculated directly through the application of (1). According ot the Fig. 5 (A), the maximum oscillation frequency of shorter n-type JNTs has decreased to 250 GHz whereas the one of IM devices has been reduced to 680 GHz, which indicates a reduction on f_{max} of about 60% for JNTs and 40% for IM devices. This reduction is similar when considering longer transistors and is accompanied by a correspondent increase in t_{min} as shown

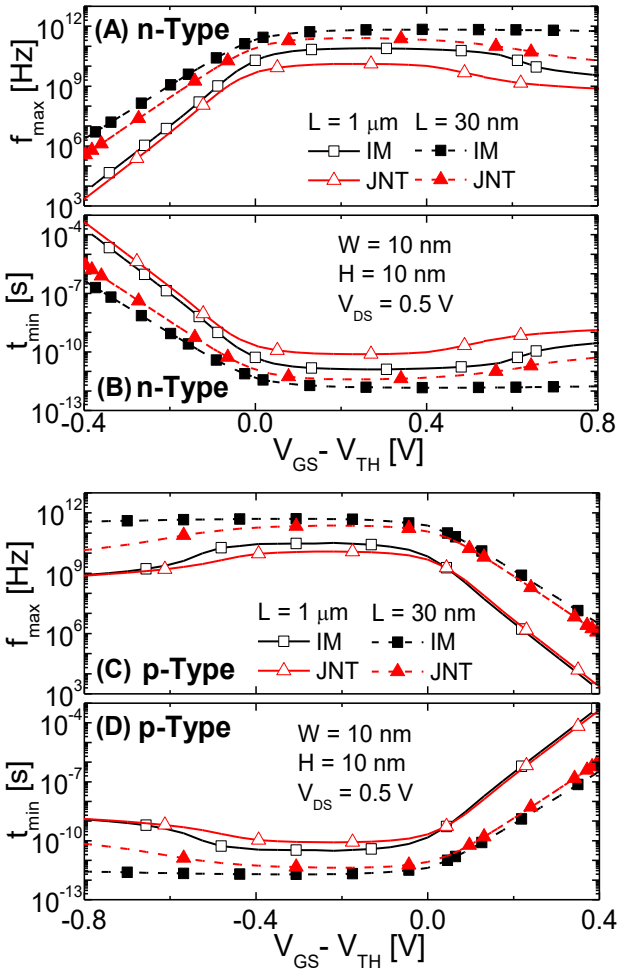

Fig. 5. Maximum oscillation frequency ((A) and (C) for n- and p-type devices, respectively) and minimum oscillation time ((B) and (D)) for IM transistors and JNTwith different L taking into account R_S.

in Fig. 5 (B). When the evaluation is performed for p-type devices in Fig. 5 (C), it is observed a f_{max} degradation of about 64% in JNTs and 35% in inversion mode transistors (f_{max} = 220 GHz for JNTs and 510 GHz for IM ones). A proportional increase on t_{min} can be observed in Fig. 5 (D) It is worth to mention that g_D was obtained as a function of $V_{GS} - V_{TH}$ for both devices and showed similar values, leading to a marginal effect on f_{max}.

IV. Transit Time

The minimum theoretical switching time of a device is given by the time that the carriers take to travel from source to drain, which is defined as the transit time ($t_{transit}$). As the time taken to charge/discharge the intrinsic capacitances in shorter devices is usually much longer than $t_{transit}$, the effect of this parameter on t_{switch} is neglected. However, when the values of t_{min} and $t_{transit}$ are in the same order of magnitude, the transit time needs to be accounted in the calculus of the minimum switching time [26]. The transit time is defined as the ratio between the conduction charge (Q_{cond}) and the drain current (I_{DS}) as indicated in eq. (3)

$$t_{transit} \approx \frac{Q_{cond}}{I_{DS}}. \quad (3)$$

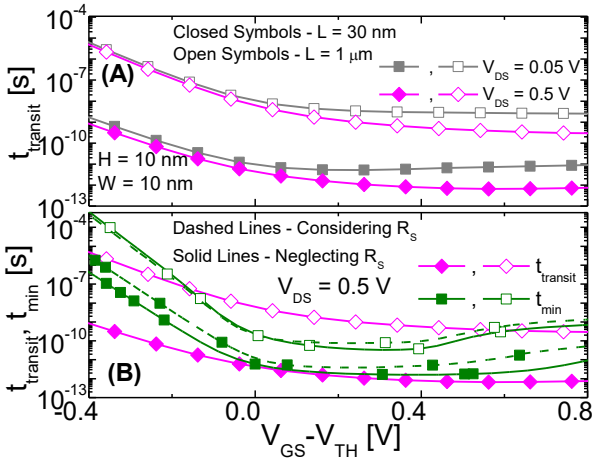

Fig. 6 Transit time ($t_{transit}$) for JNTs with two L biased at different V_{DS} (A) and $t_{transit}$ and t_{min} considering and neglecting R_S (B) for JNTs with different L as a function of V_{GS} - V_{TH}.

Although $t_{transit}$ uses to be negligible in relation to t_{min} in short channel IM devices, it is not possible to assume that assumption is true for JNTs since IM and JNTs present different conduction mechanisms and, consequently, different Q_{Cond} and I_{DS}. Indeed, JNTs present larger doping concentration than IM transistors, which is responsible for reducing its drain current and is expected to increase the carriers' transit time. In order to calculate $t_{transit}$ of JNTs, Q_{Cond} and I_{DS} were obtained through expressions (4) and (5), respectively, which have been developed for a triple gate JNT [13, 18]. Expression (4) has been employed in [18] to the calculus of the intrinsic capacitances from simulated JNTs with similar dimensions and doping concentration to the ones of the devices studied along this work, showing very good agreement. Similarly, expression (5) has been validated through experimental and simulated data in [13] for triple gate JNTs of different dimensions and doping concentrations also presenting excellent agreement.

$$Q_{Cond,y} = q.N_D.W.H - (V_{FBs} - V_B + \Phi_{SB})C_{BOX} - \left(V_{FB} - V_G + \Phi_S(V_G, V_y)\right)C_{OX}, \quad (4)$$

$$I_{DS} = \frac{\mu}{L}\left[\frac{Q_{Cond,S}^2 - Q_{Cond,D}^2}{2C_{OX}}\right], \quad (5)$$

where H and W are the device height and width, N_D is the donor doping concentration, C_{OX} and C_{BOX} are the gate and buried oxides capacitances, μ is the mobility, q is the elementary charge, V_{FB} and V_{FBs} are the front gate and the substrate flatband voltages, respectively, Φ_S is the surface potential, Φ_{SB} is the surface potential at the silicon layer to buried oxide interface, V_G and V_B are the potentials applied to the gate and substrate, respectively and V_y can be either the drain or the source bias (V_D or V_S, respectively) depending on the position of the channel in which the Q_{Cond} is calculated ($Q_{Cond,S}$ and $Q_{Cond,D}$ refer to the conduction charge density in the channel region close to the source and drain, respectively).

The calculated transit time of n-type JNTs with different L biased at different V_{DS} is presented in Fig. 6 (A) as a function

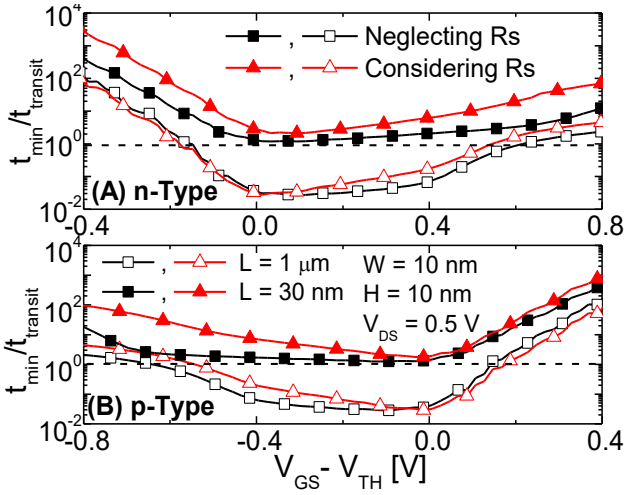

Fig. 7 $t_{min}/t_{transit}$ ratio for (A) n-type and (B) p-type JNTs with two L as a function of V_{GS} - V_{TH} biased at V_{DS} = 0.5 V.

of $V_{GS} - V_{TH}$. The curves of Fig 6 show that L and $V_{GS} - V_{TH}$ strongly impact $t_{transit}$ whereas the relationship between V_{DS} and $t_{transit}$ is weaker. As it could be expected, $t_{transit}$ reduces for shorter channel devices and larger gate voltages since both parameters present a larger influence on I_{DS} than on Q_{Cond}. The curves of both $t_{transit}$ and t_{min} are presented together in Fig. 6 (B) as a function of $V_{GS} - V_{TH}$ aiming at comparing the magnitude of both parameters. In this case, the curves of t_{min} considering and neglecting R_S are presented together in the figure. In the 30 nm-long transistor, $t_{transit}$ is smaller than the minimum oscillation time for the entire gate bias range, demonstrating that the minimum t_{switch} can be satisfactorily approached by t_{min}, independently if R_S is taken into account or not. Nevertheless, t_{min} and $t_{transit}$ present similar values in the $V_{GS} - V_{TH}$ range between 0 and 0.3 V, mainly when R_S is neglected, which indicates that t_{switch} can be slightly higher than t_{min}. On the other hand, for the 1 μm-long transistor, the transit time becomes larger than t_{min} for a wide gate voltage range, evidencing that t_{switch} cannot be approached by t_{min}.

This effect can be better observed in Fig. 7, which plots the ratio $t_{min}/t_{transit}$ for both n- and p-type transistors where it can be observed that, in longer devices, t_{min} can be lower than 5% of $t_{transit}$. This effect is explained by the exponential dependence of the channel length on $t_{transit}$ as shown in Fig. 8. It can be seen in the figure that this behavior does not depend on both the drain and the gate biases. Therefore, the calculus of the minimum switching time for longer devices can only be performed through the use of different techniques such as to consider a multiplicative factor on t_{min} to account for $t_{transit}$ or to perform the analysis considering as if a longer device were a series association of several shorter transistors [26].

The dependence of the transit time of the Junctionless transistors on the channel doping concentration and on the fin width have also been evaluated. As expressions (4) and (5) used for the calculus of the transit time are identical in n- and p-type devices and the only parameter slightly different in both transistors is the mobility, this analysis has only been performed for n-type JNTs. Fig. 9 shows the curves of $t_{transit}$ as a function of W and N_D for devices of different L. Although the transit time can vary up to 5 times

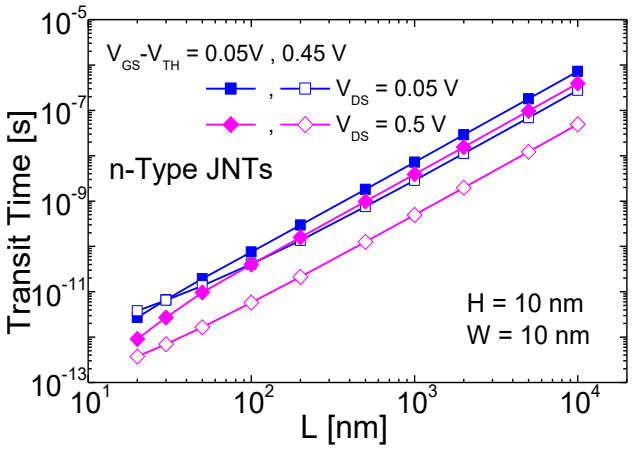

Fig. 8 Curves of the transit time as a function of the channel length for Junctionless transistors biased at different $V_{GS} - V_{TH}$ and V_{DS}.

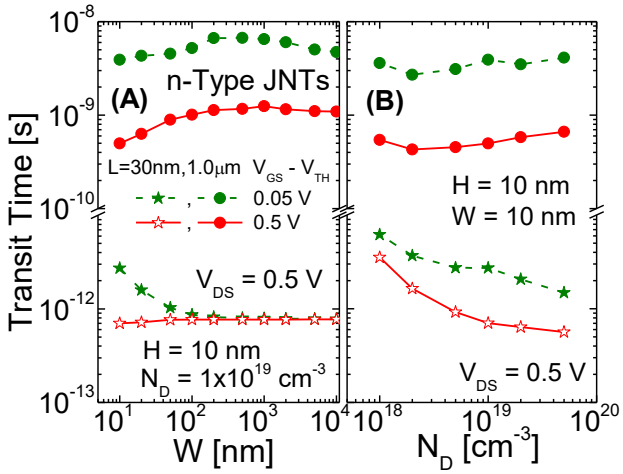

Fig 9. Curves of the transit time as a function of the channel width (A) and doping concentration (B) for JNTs of two L biased at different $V_{GS} - V_{TH}$.

with the variation of W and N_D in shorter transistors, the dependence of $t_{transit}$ on these parameters is much smaller than the one observed with L. As a result, it is possible to conclude that the minimum switching time of short channel JNTs can be adequately estimated through the calculus of their f_{max} and t_{min}, which makes it valid the application of quasi-static capacitive models such as the one from [18] to evaluate their dynamic behavior.

V. Conclusions

Along this work it was presented, for the first time, a study about the minimum switching time in n- and p-type JNTs. The evaluation has been performed in terms of the minimum oscillation time and the carriers' transit time. A comparative analysis has been carried out, in which the dynamic parameters of the JNT have been confronted to the ones of IM transistors. Although n-type JNTs present g_m about 2.5-3 times lower than IM devices, f_{max} is degraded by only 45% due to the lower capacitances and can reach up to 620 GHz when neglecting the series resistance and up to 250 GHz when considering R_S. In the case of p-type devices, f_{max} of JNTs resulted in 22% lower (≈ 610 GHz) than the one of IM devices due to the lower holes' mobility when not taking into account R_S and is approximately equal

to 200 GHz when R_S is considered. Finally, it has been shown that for 30 nm-long JNTs, the minimum switching time of the devices can be estimated directly through t_{min}, since it is larger than the carriers' transit time for any V_{GS} and V_{DS}, making it possible the application of quasi-static transcapacitance models to evaluate the dynamic behavior of JNTs. For longer devices, the minimum switching time becomes larger than t_{min}, which makes the dynamic response of JNTs a function of both parameters.

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