UTBB MOSFETs Thermal Coupling Analysis in Technological Node Level

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Abstract—**The main goal of this work is to perform a first-time analysis of the thermal cross-coupling in a system composed by some devices in an integration node degree composed by advanced UTBB SOI MOSFETs through numerical simulations, validated with experimental data from the literature. In this analysis, it could be observed that devices located on the channel length direction provoke a reduced thermal coupling and devices with their drain region next to each other suffer of an increased thermal coupling due to the lumped thermal energy. It also could be observed a degradation in some electrical parameters and in the thermal properties of a device under the influence of surrounded devices biased.**

Index Terms— **SOI, UTBB, Self-Heating, Thermal Resistance, Thermal-Coupling.**

I. INTRODUCTION

From the second half of 60´s until now, the semiconductor and microelectronic industry reached a development degree never seen before and the application of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the main character of this technological advance. In order to improve the performance and velocity of the integrated circuits, the integration density has followed the Moore´s Law [1]. The crescent miniaturization process came with an undesirable effect where the control of the charge in the channel region starts to be influenced by the depletion of the source and drain junctions, which has given rise to the so-called short channel effects (SCEs) [2].

Different technologies have been proposed to minimize the occurrence of SCEs, such as the Silicon-on-Insulator (SOI) [3], which is characterized by the presence of a dielectric layer called buried oxide (BOX), usually composed by silicon dioxide (SiO_2), which separates the active silicon layer where the devices are built, from the substrate of the wafer. Such technology enables the fabrication of shorter devices.

The SiO_2 used as electrical insulating layer in SOI devices also constitutes a thermal insulator due to its lower thermal conductivity in relation to silicon, (about 100 times smaller), and it makes the thermal dissipation in SOI poorer than in conventional bulk devices. As the substrate consists in the main path for the heat flow, the thermal insulating promoted by the dielectric layer leads to a temperature rise in the channel region, reducing the carriers' mobility. This effect is called self-heating (SHE) [4] and leads to a degradation in the devices' I–V output characteristics.

Several novel architectures based on SOI technology have been proposed and the Ultra-Thin-Body (UTB) transistor was developed. It presents reduced silicon layer thickness (t_{Si}), in the order of 6-10 nm. So that, a better capacitive coupling of the structure is reached, reducing

SCEs. However, this technology has the drawback of degrading even more the thermal conductivity of the devices, due to the smaller silicon area in the active region, increasing the SHE [5].

An evolution of the UTB SOI device constitutes in the Ultra-Thin Body and Buried Oxide (UTBB) transistor, which presents both silicon and buried oxide ultra-thin layers, where the BOX thickness (t_{box}) is in the order of 10-25 nm and t_{Si} is similar to the one found in UTBs. Due to the reduced t_{box}, the substrate bias can be efficiently used as a second gate, also known as back gate, to improve the device performance for low power analog [6] and RF applications [7]. Additionally, the smaller BOX thickness has also promoted a better thermal behavior [8-9].

It is well known that a device suffering from self-heating provokes a temperature rise in the region where it is located and, as far as we know, the effect of the thermal cross-coupling between multiple UTBB devices has not been deeply studied yet. Therefore, the main objective of this work is to analyze the electrical and thermal properties presented by a single device due its self-heating effect and the cross-heating of its neighboring devices. The work was carried out through numerical simulations validated with experimental data from the literature.

II. DEVICES CHARACTERISTICS AND APPLIED METHODOLOGY

The studied structure presents devices with channel length (L) equals to 100 and 25 nm, channel width (W) equals to 1 μm, t_{Si} equals to 7 nm, channel doping concentration of 1×10^{15} cm^{-3} and t_{box} of 10 nm. The individual devices present effective gate oxide thickness of 2 nm and elevated source and drain with 15 nm doped with arsenic with a concentration of 5×10^{20} cm^{-3}.

The work was developed through DC 3D numerical simulations at Synopsys Sentaurus TCAD [10]. Models accounting for the mobility dependence on vertical and longitudinal electric fields, carriers' generation and recombination and bandgap narrowing have been considered in all the simulations. The hydrodynamic transport mechanism has been set on in order to take into account the self-heating effect, which also considers the effect of the impact ionization in the output characteristics.

The contacts of gate, source, drain, and substrate represent the points in a simulated device that interact with the ambient with respect to the heat dissipation and thermal energy transfer. To achieve results near to the ones obtained in real devices, the thermal resistivity of the source, drain and substrate electrodes were set as 0.00016 cm^{2}K/W for source and drain and 0.00007 cm^{2}K/W for the substrate. The gate

terminal has been considered adiabatic since the passivation layer above the gate is too thick for heat removal through the gate stack [11]. The thermal resistivity at the substrate is smaller since the substrate is the main heat path for any device.

The simulations have been validated in order to obtain electrical and thermal results near the experimental ones presented in [12]. For devices with the same characteristics, it is shown that in a BOX thickness increase from 10 to 25 nm, the thermal resistance increases 1.2 times at the experimental devices and 1.15 times in the simulated ones. All the simulation results have shown errors smaller than 5% with respect to the experimental results from [12], validating the simulations. Table 1 shows a relation between the simulated results (*Sim.*) against the experimental ones (*Exp.*).

Table 1. Comparison between the simulated data and the extracted parameters presented by experimental devices with L = 100 nm in [12].

Parameter	t_{box}	Data Comparison		
		Simulation	*Experimental*	*% Error*
Drain Current [mA/μm] (@$V_{GS} = V_{TH}$ + 0.8V and $V_{DS} = 1$ V)	25 nm	0.80	0.80	0
Thermal Resistance (R_{TH}) [μm K/mW]	10 nm	69	70	1.42
	25 nm	80	84	4.34
V_{TH} [V]	25 nm	0.40	0.40	0

In the sequence, the simulations were extended to 50 nm-wide channel devices and were performed in a system composed by multiple devices simultaneously spaced 100 nm from each other, this space identified as "S" in Fig. 1. One device located at the center of the entire structure receives all the effects of the temperature rising due to the SHE effects promoted by the others around. The simulated system is composed by five devices, the central device surrounded by four others identified as A and B positioned on the X axis, in the direction of the central device channel width (W) and C and D positioned on the y axis, in the direction of the central device channel length (L). Fig.1 shows the 3D schematics with the initially adopted source and drain regions and a cut performed in the center of the structure, showing in detail the central device along with C and D devices.
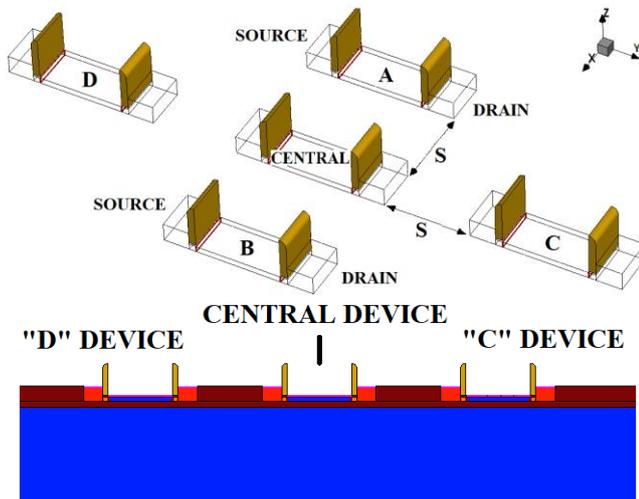

Fig.1. Structure 3D schematics above and a longitudinal cut showing the central device along with C and D devices below.

In order to take the thermal energy distribution in the whole system, the region between the devices identified as "S" in the figure was filled with insulating SiO_2, as well as the empty space in the channel width direction on the X axis below and above the transistors identified as "C" and "D" in the figure. So that, the surrounding devices were biased and some electrical parameters and the thermal resistance (R_{TH}) were extracted in the central device in order to evaluate the surrounding devices influence on the electrical and thermal properties of the central one. It is worth to mention that an adaptation of the "Hot Chuck" method [13] was applied to determine the thermal resistance of the structure.

III. ELECTRICAL ANALYSIS

To verify the influence of the temperature rise in the system, simulations were performed with each surrounding device biased individually and also for more than one simultaneously biased. Then, the electrical and thermal parameters were extracted in the central device. Firstly, for drain voltage (V_{DS}) of 1.4 V and gate voltage $V_{GS} = V_{TH} + 1$ V on the surrounding devices, it was obtained the I_{DS} x V_{GS} curves for the central device at V_{DS} = 50 mV, as shown in Fig. 2, which presents the curve of the central device biased alone and curves for the central device with the surrounding devices A and A+B also biased. It is worth to mention that the applied drain and gate voltages on the surrounding devices are higher than the limit of the considered technology in order to maximize and better visualize the studied effects. As one can observe, the central device presents changes in the off-state and in the on-state current levels as the devices A and A+B are biased along with it, presenting lower on-state and higher off-state current values which indicate changes in the threshold voltage (V_{TH}) and in the subthreshold regime (SS). By the curves, one can observe the zero-temperature-coefficient (ZTC) [3] at 0.54 V approximately. When devices A and B are biased together, a stronger thermal coupling is observed than when only device A is biased.
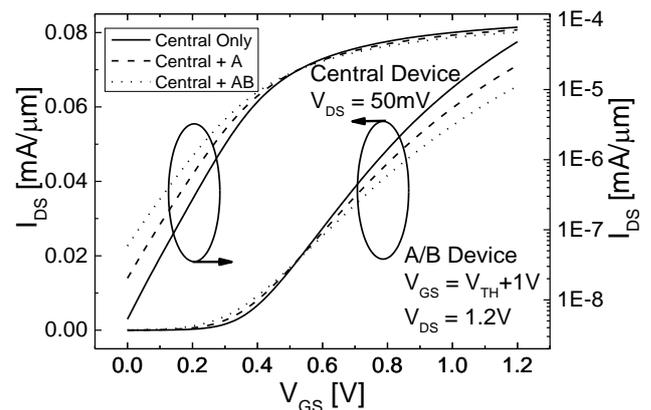

Fig.2. I_{DS} vs. V_{GS} for L= 25 nm devices with different biased devices along with the central one.

This behaviour is better seen in Fig. 3, which shows the threshold voltage (V_{TH}), extracted by the method described in [14], of the central device against the biased surrounding devices. In comparison to the central device also displayed in the figure, a reduction of V_{TH} is observed as the number of biased around devices increases. Also, it can be observed a larger effect of the biased devices positioned on the X axis direction, the A

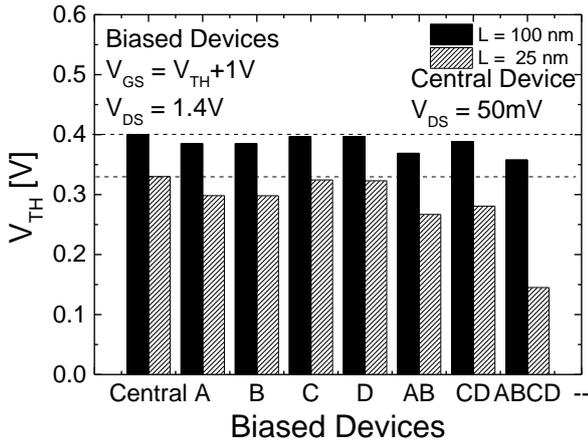and B devices, as well as they are biased separately or even when they are biased simultaneously.

Fig.3. V_{TH} vs. different biased around devices.

Fig. 4 presents the effect of the biased around devices in the subthreshold swing (SS) and one can observe that the degradation on this electrical parameter in a L = 100 nm device becomes more accentuated in the cases where the A and B surrounding devices are biased than C and D, each one or simultaneously, following the same trend of V_{TH}. It is shown an increase of 12 % in the SS of the central device when the four surrounding devices (A, B, C and D) are biased together with the central one. When analysing the results of a shorter device shown in the same figure, the degradations are even more pronounced.
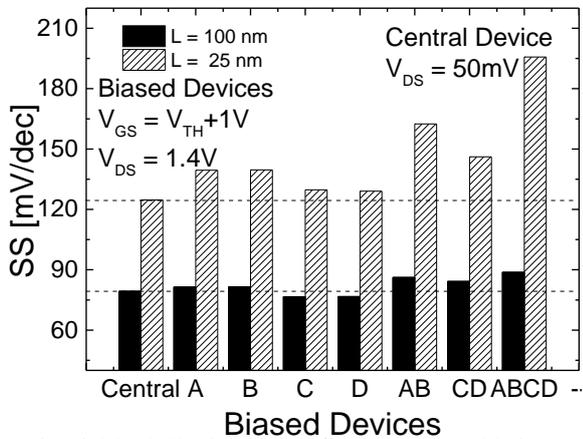

Fig.4. Subthreshold swing (SS) vs. different biased around devices.

Fig. 5 presents the same analysis for the Drain Induced Barrier Lowering (DIBL) in A, extracted by the constant current method [3], and in the maximum transconductance (g_{MMAX}) in B. One can observe that the degradations on these electrical parameters follow the same trend as observed for V_{TH} and SS. For L = 100 nm devices, the Drain Induced Barrier Lowering is 0.055 V/V in the central device alone and, when the four surrounding devices are biased along with it, DIBL increases to 0.075 V/V in A. A reduction from 2.3 to 1.9 µS/µm in the g_{MMAX} can be observed, which represents almost 20 % of degradation, when the four surrounding devices are biased along with the central one, and again, these effects are even more pronounced in the shorter UTBB. The temperature rise in the structure due to the biased around devices promotes some changes in temperature dependent parameters of the central one. Threshold voltage and the maximum transconductance, (g_{MMAX}), both present a reduction due to the change in the materials Fermi Level [15]. SS and DIBL present an increase due to the higher carriers' thermal energy, which increases the diffusion current at large temperatures [15].
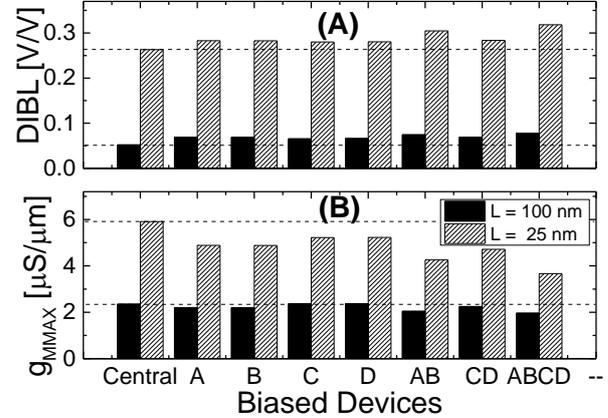

Fig.5. Drain Induced Barrier Lowering (DIBL) in (A) and Maximum Transconductance (g_{MMAX}) in (B) vs different biased around devices.

IV. THERMAL ANALYSIS

Fig. 6A shows the I_{DS} x V_{DS} curves for the both central device biased alone and with the surrounding ones also biased. A reduction of I_{DS} can be observed as the number of biased surrounding devices increases, indicating a higher influence of them on the central one. It is interesting to observe a change in the slope of the I_{DS} x V_{DS} curves as shown in the inset in Fig. 6A, which indicates I_{DS} variation between interval of 0.8 and 1 V of V_{DS} when the device is operating in saturation regime. For low V_{DS} the self-heating of the central device is negligible, but its temperature increases as the surrounding devices are biased in saturation. For large V_{DS} there is a further temperature increase due to its self-heating. As the temperature variation along V_{DS} range is higher when the central device is biased alone, it presents a flatter I_{DS} x V_{DS} characteristic in the saturation region. Fig. 6B shows g_D as a function of V_{DS}, and by the inset in Fig. 6B, one can observe the presence of a negative g_D when the central device is biased alone, and as the number of biased devices increases, g_D also increases due to the lower temperature variation in the central device as V_{DS} is raised.

In order to verify the thermal properties, R_{TH} was extracted and is shown in Fig. 7 against the biased surrounding devices for L = 100 and 25 nm. The curves show the rise of R_{TH} with the increase of the biased surrounding devices.

This effect occurs due to the temperature rising in the whole system promoted by the devices surrounding the central one suffering from SHE, which also promotes the degradations in the electrical characteristics observed in section III. In the shorter device, with L=25 nm, one can observe an R_{TH} increase from 210 to 290 K/mW when devices A and B are biased with the central one. The thermal resistance increase is lower when devices C or D are biased and increases again when A+B, C+D and A+B+C+D are biased together with the central one. It is interesting to observe a larger influence of the X axis devices (A and B) in relation to the Y axis devices (C and D).
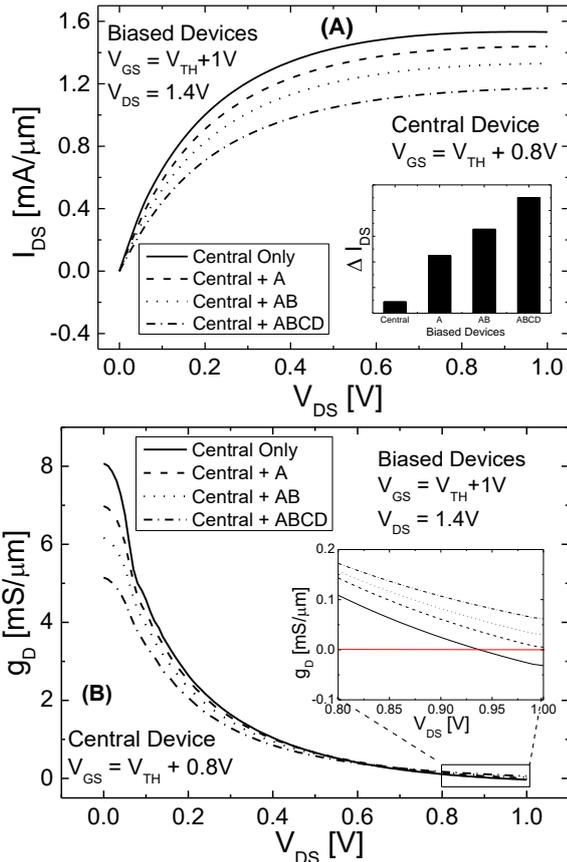
Fig.6. I_{DS} (A) and g_D (B) vs. V_{DS} for L= 25 nm devices with different biased devices along with the central one.
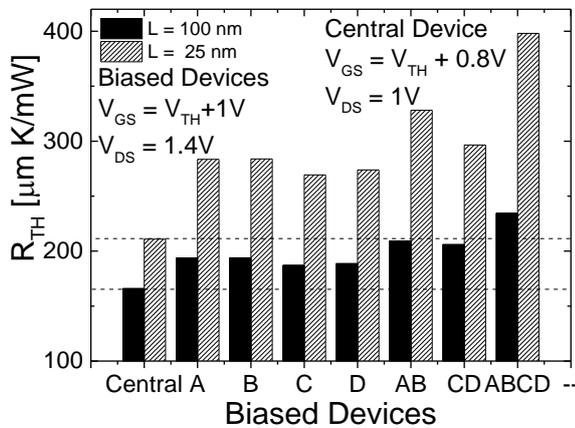

Fig.7. Thermal Resistance (R_{TH}) vs. different biased around devices.

In order to verify the behavior of g_D for I_{DS} observed in Fig.6, the output conductance was extracted and presented in Fig.8 against the biased devices.

The output conductance constitutes an important analogue figure of merit [7], which influences on device performance for analog applications as it is directly correlated to the intrinsic gain of a transistor. It is well-known that it suffers an undesirable degradation in devices presenting SHE. For severe SHE, g_D can even present negative values [16]. This indicates that the device is operating out of phase, i.e. when the drain voltage is increased, I_{DS} reduces, leading to an increment in the output bias. This effect is even worse at lower temperatures [17], where the effect of impact ionization is more pronounced and the thermal conductivity of the SOI film is reduced. Fig.8 shows a negative g_D for the central device operating alone, indicating a huge influence of the SHE on it. As the overall die temperature rises due to the biasing of the surrounding devices, the increase of the central device

temperature due to its own self-heating barely impacts the overall temperature. So that, g_D increases due to the reduction of the SHE influence, despite the I_{DS} reduction owing to the die temperature increase. It is worth mentioning that, in a L = 100 nm device, the increase in the temperature was able to shift g_D from the negative values to positive ones, and in a L = 25 nm device, which presents higher negative value, the temperature increase was not sufficient to shift g_D to positive values when C and D devices were biased. This occurs due to the lower thermal coupling promoted by C and D devices in relation to A and B.
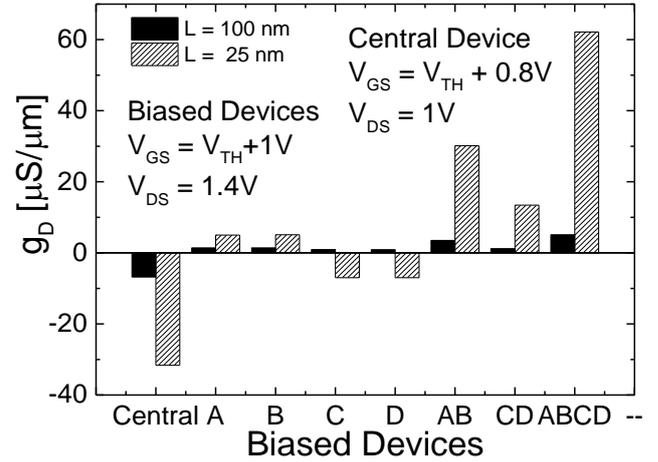

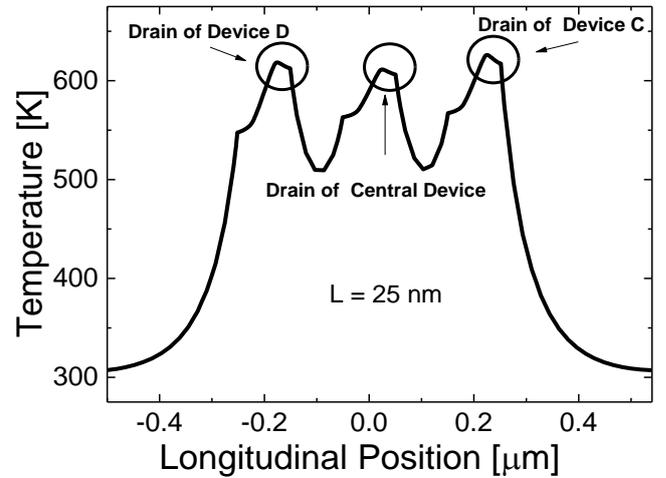Fig.8. Output conductance (g_D) vs. different biased around devices.

Fig.9. Temperature vs. system length for a L = 25 nm device die.

In order to better understand the behaviour of the surrounding devices influence on the central one, an analysis of the temperature of each device separately was performed by a longitudinal cut made in the whole die in the central of each device as shown in Fig. 9.

By Fig. 9, one can observe the highest temperature point located at the drain region of the devices. From the system schematics in Fig. 1, one can observe that devices located in the X axis are closer to the drain of the central one, separated only by the distance S, while for the devices located on the Y axis, the distance between the circled hot regions in the figure are larger, which includes, besides the distance between the devices, the channel length and the source/drain lengths. This fact explains the larger influence of devices A and B, than C and D.

To clarify the effect of the heat in the drain regions, the analysis was performed inverting the source/drain regions of A, B, C, and D devices. Fig. 10 shows, at the same previous bias condition, the results for the thermal resistance of the

central device with the surrounding ones biased with their source and drain regions inverted along with the default configuration for a comparison.
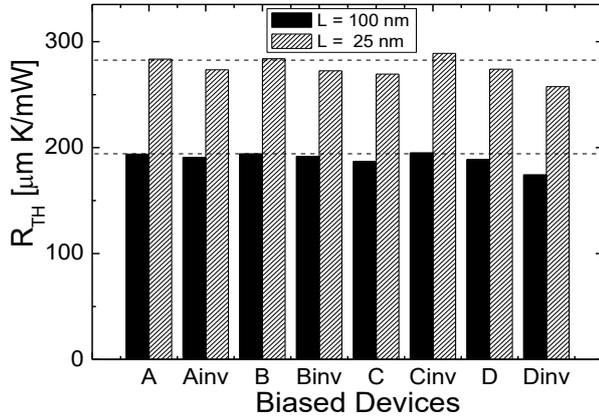

Fig.10. Thermal Resistance (R_{TH}) vs. different biased around devices.

It is interesting to note the reduction of the thermal coupling with A and B devices with their source/drain regions inverted. For the L = 25 nm device, the source/drain inversion provides a reduction of 4 % in R_{TH}. In relation to C and D devices, the inversion promotes a reduction of 8 % in R_{TH} in D device, being this, the condition which presented the weakest coupling due to the larger distance between the hotter regions. With respect to the C device, the inverted source/drain regions promote an increase of 7 % in R_{TH}, reaching values next to A and B in default condition, this occurs due to the reduced distance between the hot regions in C device inverted.

With respect to the electrical parameters, table II shows the comparison of the parameters for L = 25 nm devices in default and inverted source and drain devices and, as one can observe, the trend follows the same as the previous thermal analysis.

Table 2. Comparison between devices with their source and drain regions inverted and devices with default source and drain positions.

Surrounding Devices Biased	Data Comparison			
	V_{TH} [V]	g_{MMaX} [$\mu S/\mu m$]	SS [mV/dec]	DIBL [V/V]
A	0.2983	4.88	139.45	0.2829
Ainv	0.3012	4.903	136.72	0.2811
C	0.3255	5.221	129.71	0.2801
Cinv	0.2985	4.72	136.22	0.2890
D	0.3219	5.227	129.06	0.2804
Dinv	0.3268	5.577	127.85	0.27721

V. CONCLUSIONS.

This work has evaluated the temperature rise effects in a device positioned in the central of a wafer due to biasing of the surrounding ones. The overall analysis shows a degradation in the electrical parameters and in the thermal properties of the central device as the number of biased surrounding devices increases. It also shows that the influence becomes more accentuated with the biasing of a surrounding device located at the channel width direction. In a device with channel length of 100 nm, degradations of 9 % in V_{TH}, 12 % in SS and 36 % in

DIBL can be observed when the four surrounding devices are biased along with the central one, as well as 40% of increase in R_{TH}. In shorter devices these effects are more pronounced. These thermal degradations occur due to the temperature increase promoted by the biased around devices, and it also leads to a reduction in the harmful effects in the output conductance due to a reduced self-heating influence of the central device in the overall thermal behavior. Devices with its drain region located close to each other enhances the thermal coupling, leading to poorer performance.

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