Study of the UTBB ^{BE}SOI Tunnel-FET Working as a Dual-Technology Transistor

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Abstract— In this work we further investigate the operation of the ^{BE}SOI (Back-Enhanced Silicon-On Insulator) Dual-Technology FET, analyzing not only its behavior as a p-type Tunnel-FET when a negative back bias is applied to the structure, but also as an nMOS when a positive back bias is applied. The working principle is based on the generation of a channel of either holes or electrons by the back gate electric field, which can then be depleted through the front gate bias. TCAD device simulation was used for the proof of concept.

Index Terms— Silicon-On-Insulator (SOI), Tunnel-FET, MOSFET, Reconfigurable transistor, dual technology transistor

I. INTRODUCTION

Currently, given how costly the further scaling of transistors has become, in order to obtain performance improvements, new alternatives for the advance of the industry become more relevant, since they allow a reduction on the overall circuit area, which in turn allows the further integration of more functions in a single chip. One such alternative are the Reconfigurable Field Effect Transistors (RFET) [1]-[3], with some studies already presenting circuit design techniques optimized for such devices [4]-[5]. Among this family of devices, one recent implementation is the ^{BE}SOI (Back-Enhanced Silicon-On-Insulator) MOSFET [6]-[7], which has the advantage of few requirements on its fabrication process. This means that this device can be easily implemented on the market, without the need for state-of-the-art technologies. Using the same concept of biasing the back interface to obtain the proper charge carriers in the device's channel, but using a source doping to enable the tunneling effect controlled by the front gate bias, the UTBB (Ultra-Thin Body and Buried Oxide) ^{BE}SOI TFET was proposed [8].

As it has been shown, silicon TFET devices present good analog performance and a poor digital performance [9], since in them, the Trap-Assisted Tunneling (TAT) is strong. Consequently, there is a degradation of the subthreshold slope and a reduction on the influence of the drain voltage over the drain current, thus improving the intrinsic voltage gain. On the other hand, MOS devices on silicon can be easily fine-tuned to achieve an optimal digital behavior for instance. Therefore, combining both analog and digital high-performance in a small area could be extremely advantageous in a field such as the Internet of Things (IoT), where all devices are interconnected through wireless networks and capable of performing sensing [10], computing [11], and acting [12] functions. Ideally, such devices should present a low standby consumption, given the power constraints related to the environment where they are placed,

and high-performance when executing computationally heavy tasks, to obtain a real time response. However, thus far, most of the research was focused on the low power operation [13]-[14], to ensure the continuous operation of such devices, and when high performance computing is required, normally the information collected at the sensors is relayed to a central processing unit to be interpreted.

Therefore, in this work, we extend the results of [15], where the concept of the Dual-Technology Field Effect Transistor (2Tech-FET) was introduced. Here we present more comprehensive explanations for the operation of the device, as well as new simulations to observe the impact of gate length and drain bias on the drain current. Such a concept could enable the same silicon area to be used as either a low power, analog sensing and acting processing unit, or as a high-performance digital computing unit, offering an option to the traditional trade-off.

II. DEVICES CHARACTERISTICS

An UTBB SOI structure was simulated, with gate oxide thickness $t_{ox} = 2$ nm, source and drain doping of 10^{20} cm⁻³ and 10^{15} cm⁻³ (Phosphorous and Boron, respectively). In both cases the channel presents a concentration of 10^{15} cm⁻³ (Boron), buried oxide thickness $t_{BOX} = 10$ nm, silicon film thickness $t_{Si} = 10$ nm, and source length $L_S = 0.5$ μm. The channel and drain lengths, L and L_D , respectively, were varied during some of the simulations performed. The devices were simulated using Sentaurus Device from Synopsys [16] and the cross-section of the previously proposed UTBB ^{BE}SOI pTFET [8] is presented in Fig. 1. To simulate the TAT, the Hurkx model was used to consider the electric field influence on the Shockley-Read-Hall recombination. On the other hand, to simulate the Band-to-Band Tunneling (BTBT), the Band2Band model for recombination was adopted, considering non-local paths. On both models, some adjustments were made to the tunneling mass, obtaining a TFET behavior similar to the observed for Si devices in [9].

Fig. 1. Cross-section of the UTBB ^{BE}SOI TFET.

III. RESULTS AND ANALYSIS

As it was previously shown [8], doping only the source side with an N+ dopant and applying a negative back bias causes the formation of an accumulation layer on the back interface from the source junction until the drain contact, allowing the operation of this structure as a pTFET. It is considered to be similar to the ^{BE}SOI MOSFET presented in [6]-[7] in the sense that a back bias is required to improve its operation. However, should a positive back bias be applied to this structure, an inversion layer could form from source junction to drain contact, meaning that it would behave as an nMOSFET. Thus, through the proper back biasing, it is possible to alter not only the device type (that is, its operation as an n- or p-type MOSFET), but its whole physical principle of operation, hence the proposed name of 2Tech-FET. To understand how this device operates, two different back bias configurations will be investigated: first, a negative back bias will be applied, to better understand the working principles of the UTBB ^{BE}SOI pTFET; then, a positive back bias will be applied to observe its nMOSFET characteristics.

A. Negative back bias

To measure the influence of the negative back bias, the drain current (I_D) versus gate voltage (V_{GS}) for multiple back gate biases (V_{GB}) curves are presented at two different drain voltages (V_{DS}) in Fig. 2 and Fig. 3.

The first important characteristic of this device is that it presents a strong reduction on the ambipolar effect, as would be expected from a self-aligned TFET. The elimination of the P+ junction means that, within a given range of V_{GB} , independently of the positive bias on the gate, the bands along the channel cannot be shifted abruptly enough to allow the band-to-band tunneling on the drain side. However, should V_{GB} become sufficiently negative, some increase on the drain current can be observed for positive values of V_{GS} , starting to become significant at $V_{GB} = -3$ V.

Fig. 2. Drain current versus gate voltage for multiple negative back biases and $V_{DS} = -0.5$ V.

Fig. 3. Drain current versus gate voltage for multiple negative back biases and $V_{DS} = -1$ V.

Independently of the drain voltage applied, one important effect observed in Fig. 2 and Fig. 3 is the decrease of the on-state current (I_{on}) by almost one order of magnitude when the back bias applied is zero. Since the drain region presents only the intrinsic doping, this effect could be understood as a device with a high drain resistance, given that, in this situation, the applied back bias does not strongly invert nor accumulate the back interface of the whole device. This idea is further verified in Fig. 3, where a smaller drain length was simulated, which resulted in a higher I_{on} at $V_{GB} = 0$ V; moreover, when a negative back bias is applied, there is no change in I_{on} for the shorter L_D , meaning that the drain resistance becomes far less significant.

One remark about this simulated device is that, given the difference between gate oxide and buried oxide thickness, the region where most of the tunneling occurs is at the N+ junction on the front interface, since the thinner oxide allows a stronger bending of the bands in that region. Thus, a simplified model of the UTBB ^{BE}SOI pTFET operation is presented in Fig. 4(a). In it, the main idea is that the negative back bias creates a hole channel, connecting drain contact to the front interface channel. Although there is a weak P- region between front and back interfaces, since most of the tunneling should occur on the front interface, there is a considerable current from back to front interface in order to improve the operation of this device, by reducing the drain resistance. To confirm this, the band-to-band generation in the simulated device at $V_{GB} = -2$ V and $V_{GS} = -3$ V is presented in Fig. 4(b).

Then, to turn off the device, a sufficiently high bias must be applied to the front gate, in order to interrupt the band-to-band tunneling happening between channel and source. However, as it was previously mentioned, under the right front and back gates bias conditions, an ambipolar current is observed. A simplified model for this effect is presented in Fig. 5(a).

Fig. 4. (a) Schematic representation of the operation of the ^{BE}SOI pTFET as it was originally proposed; (b) band-to-band generation on a simulated device biased at $V_{GB} = -2$ V and $V_{GS} = -3$ V.

Since the positive front gate bias depletes the whole silicon film under it given how thin it is, the only possible region left on the device where accumulation and inversion layers are close enough to allow the band-to-band tunneling is at the very edge between front gate and undoped drain. Besides that, this effect only occurs when there is a sufficiently high potential change, resulting in a distance between accumulation on the back interface of the drain region and inversion on the front interface channel smaller than the necessary tunneling length. Confirming this, the simulated band-to-band generation ratio is presented for a significantly negative back bias of -4 V and a sufficiently high front gate bias of 2 V in Fig. 5(b).

Fig. 5. (a) Schematic representation of the operation of the ^{BE}SOI pTFET when V_{GB} is sufficiently negative to enable the ambipolar current; (b) band-to-band generation on a simulated device biased at $V_{GB} = -4$ V and $V_{GS} = 2$ V.

Fig. 6. Drain current versus gate voltage for multiple gate lengths and V_{GB} , considering $L_D = 500$ nm and $V_{DS} = -1$ V.

One other parameter that can be availed of this device is the dependence of its current with channel length, as is presented in Fig. 6. As expected from a TFET where the tunneling takes place only in a point-like region, there is no strong relation between current and channel length as long as L remains above twice the silicon thickness [17].

B. Positive back bias

The first consequence of applying a positive back bias is that the back interface will most of the time be in inversion, meaning that there is a continuous path of electrons between source and drain contact, since the source is n-type. However, depending on the front gate bias, this path can be interrupted by a depletion layer, meaning that this device could, indeed, operate as an nMOS under the proper bias conditions.

Taking this premise into account, the I_D versus V_{GS} characteristics of the UTBB ^{BE}SOI TFET operating as an 2Tech-FET under multiple positive back biases and at two different drain biases are presented in Fig. 7. In Fig. 8, the effect of using different V_{DS} is further investigated.

Fig. 7. Drain current versus gate voltage for multiple positive back biases and two different drain voltages.

Fig. 8. Drain current versus gate voltage for two different positive back biases and varying drain voltages.

When V_{GB} is grounded in Fig. 7, independently of the drain bias applied, this device does not operate as an nMOS, which is an expected result, since, with this back bias, the back interface will not be inverted. In this situation, two distinct curves are observed: when $V_{DS} = 0.5$ V, a pTFET current curve is observed for $V_{GS} < 0$ V, while a low, constant current occurs when $V_{GS} > 0$ V; when $V_{DS} = 1$ V, two current plateaus are observed, with a transition occurring around $V_{GS} = 0$ V. These characteristics suggest that a diode-like behavior is taking place under those bias conditions, since a reverse biased PN junction is required for the TFET behavior. Thus, when the higher drain bias is applied, this junction is forward biased, resulting on the much higher I_D . For the case where $V_{DS} = 0.5$ V, the difference observed between negative and positive values of V_{GS} can be understood through the regions where the tunneling takes place. For negative values, the tunneling occurs on the well-defined source junction, while for positive values it depends on the weakly doped drain. On the other hand, when $V_{DS} = 1$ V, the current difference between both plateaus can be understood as a change on the structure of the diode, from a p⁺-p⁺-n⁺-n⁺ to a p⁺-n⁺ when V_{GS} changes from negative to positive values, as illustrated in Fig. 9.

There are three curves in Fig. 7 that approximate well the behavior of a Fully Depleted (FD) SOI nMOS device, meaning that the drain current has well defined on- and off-states, and a linear subthreshold slope (in logarithmic scale): when $V_{GB} = 2$ V, for both values of V_{DS} ; and when $V_{GB} = 1$ V and $V_{DS} = 0.5$ V. In those situations, the operation occurs as illustrated in Fig. 10, that is, when $V_{GS} > 0$ V, the back bias is able to create an inversion layer on the back interface from source junction to drain contact (Fig. 10a), allowing the direct passage of current.

Fig. 9. 2Tech-FET operating under diode-like bias for (a) positive and (b) negative front gate voltages.

This means that, primarily, the current on this device will propagate through the back interface, with some of it moving to the front interface at higher values of V_{GS} , but not enough to present a strong increase in the drain current, as it was observed in Fig. 7. Then, when V_{GS} becomes sufficiently negative, the potential interaction between front and back interfaces means that the back interface threshold voltage will be affected by the variation of the front gate voltage. The decrease of V_{GS} results in a higher back gate threshold voltage. Consequently, since in this analysis V_{GB} is kept constant, the back interface is transited from inversion to depletion entirely due to the front gate voltage (Fig. 10b), meaning that there is no direct path for the electrons in the channel region, while the drain region still presents both the depletion and inversion due to the back bias. This ensures that there is no parasitic diode on direct polarization in the structure at this bias condition, effectively lowering I_{off} to negligible levels.

It is important to notice that the device does not turn off for the case where $V_{GB} = 1$ V and $V_{DS} = 1$ V because the interaction between drain and back gate electric fields causes the weak accumulation of holes in the drain region, making the device behave as a forward biased diode. Fig. 8 further demonstrates this, since the increase in V_{DS} further increases the drain current. However, since the drain resistance remains elevated, the current increase with V_{DS} does not present an exponential behavior.

Fig. 10. 2Tech-FET operating at $V_{GB} = 2$ V for front gate bias (a) above and (b) below threshold voltage.

For $V_{GB} \geq 3$ V, the back interface is strongly controlled by the back bias, which means that, even when highly negative values of V_{GS} are applied, it is not possible to completely cut-off the inversion at the back interface. This happens because, when the front interface reaches accumulation, little change is observed on the threshold voltage of the back gate, resulting in increased values of I_{off} for higher V_{GB} , independently of V_{GS} . For thin films, it might not always be possible to reach this circumstance where each interface is at a different condition, however, it has been shown that, given the proper biases and t_{BOX} , it is possible that a 10 nm film does not present supercoupling between both interfaces [18]. Thus, this indicates that this proposed 2Tech-FET requires an optimization on the biases applied for operation as an nMOS. For the back interface, it is necessary to find a balance between enabling the passage of current through it and avoiding that it is always inverted, independently of the front gate voltage. For $V_{BS} = 3$ V, the back bias is close to the threshold voltage, so the I_{off} current obtained is already above the levels obtained for smaller V_{BS} , but still only on the order of pA, thus can be considered negligible; however, at $V_{GB} = 4$ V, I_{off} is much closer to the I_{on} , so this nMOS operation would be compromised. A schematic representation of the device operating under these bias conditions is shown in Fig. 11(a), with a current density plot shown in Fig. 11(b). For the case where V_{GS} is positive, the device should operate exactly as presented in Fig. 10(a), with a direct current path from source to drain.

Fig. 11. (a) 2Tech-FET operating at $V_{GB} \geq 3$ V for front gate bias below the flat band voltage; (b) Current density for $V_{GB} = 4$ V and $V_{GS} = -3$ V.

To verify the behavior of this device when different channel and drain lengths are considered, additional simulations were performed, first considering a fixed L of $1 \mu\text{m}$, and L_D of 100 nm and 500 nm, as presented in Fig. 12; then fixing L_D as 500 nm and varying L from $1 \mu\text{m}$ down to 50 nm, shown in Fig. 13. For the devices in the subthreshold regime, it is possible to notice in Fig. 12 that the drain length causes no significant impact; however, the on-state current changes significantly, being from 2.5 up to 3 times higher on the device with shorter drain length. This is an expected result since, for low currents, there is no significant voltage drop on the associated drain resistance.

Fig. 12. 2Tech-FET simulated with two different drain lengths for multiple back gate biases.

Fig. 13. 2Tech-FET simulated with multiple channel lengths.

However, when the device is on, the voltage drop on this resistance cannot be neglected, thus, the device with a shorter drain length presents a significant increase in its drain current. Although applying a higher V_{GB} does reduce the drain resistance, allowing a more elevated I_{on} when the drain length is longer, it also increases I_{off} as previously discussed. Therefore, depending on the project restrictions, it is possible to achieve an optimization between drain length and back bias applied to obtain a sufficiently high I_{on} without compromising I_{off} .

In Fig. 13, the decrease in channel length causes little change in the on-state current, but it does affect the off-state current. Consequently, there is a slight degradation on the subthreshold swing. Once again, to understand this phenomenon, it is necessary to consider the impact of the drain resistance on the operation of this device, since it is so elevated that it becomes more critical than the resistance of the channel on the overall resistance seen from the drain when the device is on. Therefore, in terms of scaling, if higher currents and steeper subthreshold slopes are desired, the drain length of this device can be considered as important as the channel length.

IV. CONCLUSIONS

In this work, using TCAD 2D-device simulation tools, we further developed the understanding on the use of the UTBB^{BE}SOI pTFET structure as a Dual-Technology transistor, that is, capable of operating both as a p-type Tunnel-FET and an nMOSFET just changing its bias conditions. This ability to reconfigure the operating physics of the device was enabled by removing the doping from one side of a conventional SOI MOSFET and applying proper back gate and drain biases. The drain current versus gate voltage characteristics were analyzed for multiple substrate biases, providing insight on the operational details of this device, and revealing that some optimization is required when choosing the biases to be applied for proper operation. For the nMOSFET this optimization is even more critical than for the pTFET, since a proper bias is required to effectively disable the parasitic diode, while simultaneously avoiding to force the back interface to an always on-state, given that

both conditions increase the off-state current. Considerations were made on two important physical dimensions of this device, its channel and drain lengths, showing that its drain resistance cannot be neglected, due to its low doping, to the point where scaling the drain length becomes more critical than reducing only the channel length.

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