FinFET Inverter Designs: Behavior and Challenges of Process Variability

Leonardo B. Moraes[1], Alexandra L. Zimpeck[2], Cristina Meinhardt[3], Ricardo Reis[1]

[1] PGMicro/PPGC, Universidade Federal do Rio Grande do Sul - UFRGS, Brazil
[2] Centro de Ciências Sociais e Tecnológicas - PGEEC, Universidade Católica de Pelotas - UCPel, Brazil
[3] Departamento de Informática Aplicada e Estatística, Universidade Federal de Santa Catarina - UFSC, Brazil
{lbmoraes, reis}@inf.ufrgs.br, alexandra.zimpeck@ucpel.edu.br, cristina.meinhardt@ufsc.br

Abstract— Technology scaling is, alongside the increasing process variability impact in modern technology nodes, a main reason to control deviations over metrics in IC nanometer designs. Schmitt Triggers are traditionally used for noise immunity enhancement and have been recently applied to mitigate radiation effects and process variability impact. The main contribution of this work is to trace the relationship between transistor sizing, supply voltage, and process variability to achieve a low energy consumption circuit while still keeping low levels of deviations due to the impact of process-induced variability. It is shown that a cost-benefit analysis can highlight sets of sizing and supply voltage where it can provide a 37.51% decrease in energy consumption while only increasing its sensibility by 7.42%. Furthermore, it is presented that the relation between the supply voltage and the circuit's sensibility to process variability is not directly proportional in all cases, with slight decreases in the supply voltages, bringing overall smaller metric deviations. Overall, the traditional CMOS inverter is still the fastest and most energy-efficient circuit. The TIST presents the highest hysteresis ratios and output gains while presenting appropriate measures for slopes and noise margins at the lowest supply voltage of 0.1 V, while also presenting a smaller layout area than the 6T ST and SIG. The improvements, although, may increase propagation times, energy consumption, and area.

Index Terms— FinFET; Process Variability; Schmitt Trigger; Microelectronics

I. INTRODUCTION

Technology scaling, as stated by Moore where the transistor count in a chip should double at about every two years, is a significant factor in the ascendance of Integrated Circuits (ICs), providing higher transistor densities and voltage scaling due to the miniaturization of gate dimensions, internal capacitance, and resistance. Such improvements provided the IC designers with plenty of processing power per area unit of a chip and energy efficiency, making it the perfect combination for the usage of ICs in mobile applications [1].

As devices shrank, several transistor characteristics became severe problems for the modern semiconductor industry, alongside some new challenges. As the transistors got smaller, the supply voltage decreased and accommodated appropriate currents to an evermore smaller channel. Although, as the supply voltage decreases, the noise margins got narrower, with lower currents and capacitance curbing the circuit ability to mask the transients caused by external noise and radiation-induced soft errors [2].

Furthermore, variations in the device's geometrical and electrical parameters were always a reality, introducing minor, if not negligible, variations into the circuit behavior. Even though those geometrical variations did not scale down at the same rate as the devices, it has gotten increasingly difficult to produce smaller light waves to print such small patterns correctly. Additionally, modern devices are so close to the atomic limit that even variations in the scale of few units to few hundreds of atoms can exert influence on the device behavior, decreasing yield [2].

One of the industry responses to the challenges related to the semiconductor industry's improvements is the Fin Field Effect Transistor (FinFET) technology. FinFET devices present superior channel control due to the reduced Short Channel Effects (SCE) and low impact of Random Dopant Fluctuation (RDF) due to the fully depleted channel [3]. Although, at deep technology nodes, variability is one of the most challenging factors, even in FinFET devices. In technology nodes below 90 nm, the impact of random process variability is becoming increasingly decisive in determining the yield performance and consequently production cost. Process variability introduces more significant metric deviations, turning more circuits unpredictable and not suited for operation [4, 5]. Furthermore, process variability may affect the circuit aging profile, hastening the loss of performance [6].

Variations in physical parameters became alarming at ultra-deep sub-micron (UDSM) nodes because the node scaling was accompanied by a supply voltage scaling, making the circuits more susceptible to noise and electromagnetic interference due to the deterioration in the Static Noise Margin (SNM) [7]. Given that, this work explores four types of inverters, where three of them are considered STs due to their hysteresis characteristic. This work evaluates the inverter design behavior through process variability. The analysis will consider the means, standard deviations, and normalized standard deviations for the delays, energy consumption, and hysteresis. The noise margins and slopes will only be considered their respective measures without the respective variability impact. The main contributions of this work are: 1) bring a new discussion Three Inverter Schmitt Trigger (TIST) circuit, highlighting the particular constraint of transistor sizing, 2) discuss the pros and cons of each inverter design about process variability mitigation, power, and delay; and 3) trace the relationship between transistor sizing, supply voltage, and process variability to achieve a low energy consumption circuit observing process variability effects.

This work is divided into five further sections: Section II, Process Variability Mitigation, presents related work about Schmitt Trigger applications and designs. Section III, In-

verter Designs, describes the considered circuits. Section IV, The Methodology Section, explains the experimental setup which was employed to generate the results. Two results sections are presented: Section V concerning the inverter analysis, and Section VI concerning the analysis of the inverter replacement on Full Adders. Lastly, in Section VII, the conclusions concerning both analyses are presented.

II. PROCESS VARIABILITY MITIGATION

The main challenges to process variability mitigation are related to the manufacturing process. However, some transistor-level or circuit-level approaches can be explored to mitigate process variability impact. The Schmitt Trigger (ST) circuit has been pointed as an alternative for the classical 2-transistor inverter to improve the circuit robustness to such impact. Schmitt Triggers (ST) are commonly used as internal circuits on systems to provide enhanced noise tolerance, and robustness against random variations in the input waveforms [8]. On a standard input (non-ST), its binary value will switch simultaneously on the rising and falling edges. With a slow rising edge, the input will change near the threshold point. When the switching occurs, it will require current from the supply source. With current being pushed from the supply, it can cause a voltage drop across the circuit, causing a shift in the threshold voltage. If the threshold shifts, it will cross the input causing it to switch again. It can go switching indefinitely, causing oscillation. The same thing can happen if there is noise on the input. STs are applied in these cases to filter noise, introducing superior and inferior threshold voltages. STs circuits present a hysteresis characteristic. This hysteresis exists in the presence of two switching V_T. If the input level is within the hysteresis region, the ST shall not switch. Such characteristic gives a higher static noise margin (SNM) in comparison to traditional inverters, ensuring a high noise immunity. A variety of CMOS STs has been proposed and implemented over the years based on different requirements. The new proposed STs are frequently compared with the most traditional circuit, that is the ST 6T, presented in Fig. 1(a). The related work improvements are described in comparison with this ST 6T cell.

To improve the performance of the traditional ST, a different design is proposed to achieve a smaller load capacitor value and to decrease the slew rate of the ST internal node [9]. A ST with a programmable hysteresis is proposed in [10]. The programmable hysteresis is achieved by adding a P and N transistors in series with the 6T ST P_F and N_F transistors, respectively, both receiving the same gate signal. In [11], it is proposed a 10T ST whose hysteresis interval does not depend on transistors width/length ratios being, consequently, more robust to process variations compared with the ST 6T.

A low-power ST is proposed with low short circuit current achieved by the presence of only one path to each power rail, being recommended for low power, very low-frequency applications [12]. Also in [13], it is proposed a low-power ST by having only one transistor transmitting (at stable output values), considerably reducing power consumption compared with the traditional ST circuit. STs can be optimized

by adequate sizing as well as stated in [14] where the optimization of the transistor sizing presented the best metrics for low power applications, in accordance to [15].

In [16], a voltage-booster is applied in the traditional 6T ST in order to replace its pull up network and reduce the number of PMOS transistor to only one. It was simulated on 32 nm bulk CMOS technology and was revealed to present 168.68% less deviations than the CMOS inverter considering process variability. It is essential, though, to highlight its 4.315x higher leakage power and potential higher area, given Finfet technology restrictions considering the higher number of NMOS transistors (5) in comparison to the traditional 6T ST (3).

In [17], a novel technique based on the replacement of Full Adders internal inverters with low voltage STs for process variability robustness improvement is originally introduced and applied on seven different FA designs. The simulations were performed using the 16nm bulk CMOS predictive technology model in SPICE. It presented significant variability improvement up to 4.8x in energy consumption. The improvements occur at the cost of an increase in the area and power dissipation of each design. This technique is tested in other works: the ST technique is applied on four FAs at 16nm technology [18]. The adoption of ST in the outputs of the full adders presented promising results regarding the power deviation due to the process variability with a decrease of up to 79% with a drawback of a significant increase in average energy consumption. The ST technique applied to 4 different FAs layouts at 7nm FinFET has reached 64.74%, and 66.6% reduction in delay and power deviation compared to the full adders without the ST technique [19].

A novel Schmitt-trigger-based single-ended 11 Transistor SRAM cell shows reduction on the energy consumption per operation with the smallest leakage power and a 6.9x higher I_{ON}/I_{OFF} ratio [20] compared with the classical SRAM 6T cell. Further process variability simulations confirmed the robustness of the design regarding reading and writing operation. The simulations were carried in 22 nm predictive technology using SPICE.

A ST buffer using CNFET is explored resulting in, on average, 68% higher critical charge and 53% lower energy consumption and a huge gain considering process variability robustness as compared to its most efficient CNTFET-based counterparts. The simulations were carried in 16 nm Stanford CNFET model using SPICE [21].

In a previous work, we show how Schmitt Trigger circuits can be explored to process variability mitigation [22]. Observing the characteristics of a minimum energy-oriented FinFET design, we report that, on average, the supply voltage decreases in layouts with a smaller number of fins while maintaining acceptable robustness in high variability scenarios. Exploring voltage and transistor sizing made possible a reduction of about 24.84% of power consumption in comparison to a traditional transistor sizing [23]. Also, comparing ST with Stacked-Inverter Gates, the accurate adjustment of the supply voltage and transistor sizing, at a high variability scenario, can decrease the energy consumption up to 32.19%. It was possible to show a considerable difference concerning the Schmitt Trigger noise-immunity characteris-
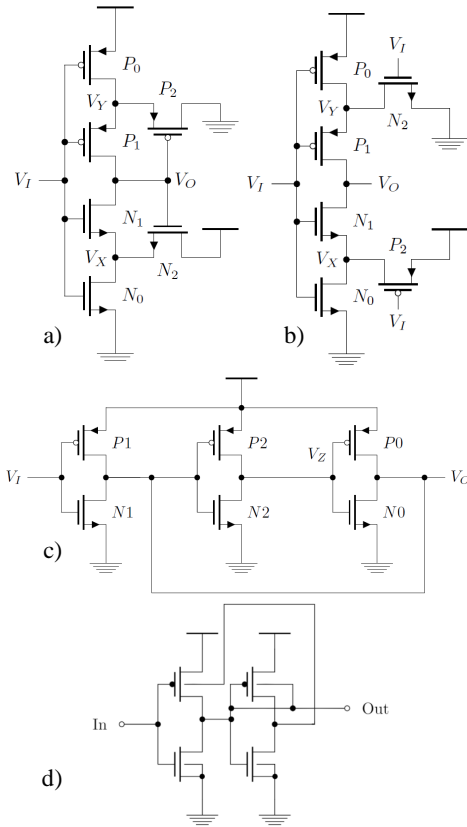
Fig. 1: Considered inverter designs: a) 6T ST, b) SIG, c) TIST, and d) LPST.

tics compared to other designs, over supply voltage and variability scaling. In comparison to previous works, this paper aims to deliver a full analysis over circuit metrics, including the TIST circuit, which, as will be shown in the methodology, requires a particular sizing.

III. INVERTER DESIGNS

Variations in physical parameters became alarming at ultra-deep sub-micron (UDSM) nodes because the node scaling was accompanied by a supply voltage scaling, making the circuits more susceptible to noise and electromagnetic interference due to the deterioration in SNM [7]. Given that, this work selected four different inverter circuits, where two of them are considered STs given their hysteresis characteristic, to evaluate the effectiveness in diminishing the impact of variability into the metrics according to an overall overview in the current literature as shown in Fig. 1.

A. Traditional 6T ST

The 6T traditional ST main feature is the presence of P_F and N_F devices, responsible for a feedback system which originate its hysteresis effect [24]. The 6T ST was chosen due to promising results at [25], where a 6T ST-based 8x8 multiplier was presented, with the ST greatly improving the on-to-off current ratio. In [26] an SRAM based on 6T ST is proposed working at 160mV and showing improvements of both robustness and static noise margins compared to a traditional inverter-based solution.

The main effect of process variability is a shift on the voltage transfer curve (VTC) due to the threshold voltage variation. Usually, the input voltage, where a device starts de-

livering current, is directly dependent on the V_T. Thus, the variability impact on VTC is reduced in the ST due to the strong influence of the gate-source voltage of the inner transistor (N_I and P_I) over its switching point [25].

B. Three Inverter Schmitt Trigger (TIST)

The TIST is a ST implementation, most common in textbooks. It consists of a CMOS inverter followed by a latch. According to [27], the TIST can provide hysteresis from a supply voltage as low as the classical inverter unity gain. However, for higher supply voltages, the hysteresis interval will grow excessively to a point where the cell locks itself in a random state (low or high), which cannot be changed. Furthermore, it was shown that the hysteresis interval and the minimum supply voltage for it to appear greatly benefit from increasing the ratio between the latch and inverter transistors. Given so, to tackle some of that problem, the inverter transistors were sized with a higher number of fins in comparison to the latch. Still, it shows the TIST viability to work at sub 100 mV supply voltages, which will be explored in future works.

C. Stacked Inverter Gate (SIG)

SIG is a circuit composed of unbalanced inverters without positive feedback, referred to as stacked or redundant, inverters. It presents improvements over the CMOS inverter regarding voltage gains [28, 29]. Originally, it was applied on replacing the inverter of a ring-oscillator working at a sub-50mV supply voltage, presenting 30% higher gains, claiming that energy harvesting techniques based on the body-to-ambient temperature gradient can leverage such oscillator to achieve self-startup.

D. Low Power Schmitt Trigger (LPST)

The following circuit is not compared to the previous ones, although being applied on the following analysis considering the replacement of FAs internal inverters. It was not applied in the comparison between inverter circuits due to technology restrictions, which did not permit the connection of the NMOS devices back-gates to specific nodes. The LPST inverter circuit used in this work was inspired by [30] and modified in [17] to achieve the desired inverting characteristic. It is designed for operation at a supply voltage of 0.4V to achieve low power consumption, and consists of two inverters where the output from the second one will be the bulk for the first one.

IV. METHODOLOGY

This work evaluates the following four topics to provide an extensive exploration of the process variability impact over the behavior of the circuit:

1) Four inverter circuits. The traditional CMOS inverter, the 6T ST, the TIST, SIG, and LPST;

2) The influence of transistor sizing where all transistors have the same number of fins (except for the TIST);

3) Multiple levels of supply voltage, from 0.1 V to 0.7 V (nominal);

4) Multiple levels of process variability observing the workfunction fluctuation (WFF) from 1% to 5%, in steps of

1%. This variation is inserted into the simulations following Gaussian distributions.

Given the set of possible scenarios, this work aims to provide a case-study to show the potential of using these circuits as a technique to mitigate process variability effects.

The design flow was divided into two steps: the layout design and electrical simulations. After finishing the layout design process, each layout was passed through validation, consisting of a Design Rule Check (DRC) and the Layout Versus Schematic (LVS) verification.

The transistor sizing exploration evaluates layouts from 1 to 5 fins through 1-fin steps for the CMOS inverter, the 6T ST, and the SIG. It is important to highlight that the ST behavior presents some challenges at low voltage [31][32]. So, it is important to clarify that a sizing modification was mandatory to ensure the correct behavior of some Schmitt Trigger circuits operating at the near-threshold regime. Adopting other sizings, the Schmitt Trigger does not work properly, presenting an unexpected behavior of being locked in a logic level. This phenomenon happens at near-threshold operation and is related to the transistor sizing. This reinforces the demand for careful sizing of this kind of inverter. This phenomenum happens in the TIST circuit, that did not present an acceptable behavior with its P and N devices presenting the same number of fins, with its output value getting stuck. Thus, for the TIST, a different approach was adopted. The TIST consists of a traditional inverter (transistors P_1 and N_1) followed by a latch (transistors P_0, P_2, N_0 and N_2). Given so, the inverter transistors were resized following a proportion between their size and the size of the latch transistors. It was adopted two proportions: 2:1 and 3:1, resulting in five different layouts. Three layouts follow a 2:1 proportion with the inverter transistors containing 2, 4, and 6 fins and the latch transistors containing 1, 2, and 3 fins, respectively. Two layouts follow a 3:1 proportion with the ST transistors containing 3 and 6 fins and the latch transistors containing 1 and 2 fins, respectively.

All circuits were designed using the Virtuoso Electronic Design Automation (EDA) tool from Cadence®with the Process Design Kit (PDK) of 7nm FinFET of Arizona State Predictive PDK (ASAP7) from the Arizona State University in partnership with ARM [33]. It is the only open-source and free 7nm PDK available for educational use. This PDK was chosen due to realistic design conjecture regarding the current design competencies. FinFET technologies present the width quantization aspect [34]. With a 27nm fin pitch, a high-density layout is achieved with 3-fins transistors. Otherwise, there is a lower density and routing complexity [35]. The main PDK rules and lithography assumptions considered in this work are shown in Table I. To exemplify the PDK layers, the 3-fins transistors 6T ST is shown in Fig. 2.

The simulations are carried out using HSpice, and the netlist obtained after the physical verification flow and the parasitic capacitances extraction. The device geometry deviation impacts the electrical parameter WF causing high fluctuations [15]. It happens due to the orientation of metal grains that are randomly aligned in the FinFET manufacturing process. So, WFF represents the most significant variation beyond the other parameters [36]. The process variabil-

Table I. Key layer lithography assumptions, widths and pitches [33]

Layer	Lithography	Width (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

Table II. Parameters applied in the electrical simulations [33]

Parameter		7nm
Nominal Supply Voltage		0.7 V
Gate Length (LG)		21nm
Fin Width (WFIN)		6.5nm
Fin Height (HFIN)		32nm
Oxide Thickness (TOX)		2.1nm
Channel Doping		$1 \cdot 10^{16} cm^{-3}$
Source/Drain Doping		$2 \cdot 10^{16} cm^{-3}$
Work Function (eV)	NFET	4.372
	PFET	4.8108
Threshold Voltage (V)	Saturation NFET	0.17
	Saturation PFET	-0.16
	Linear NFET	0.19
	Linear PFET	-0.19

ity evaluation adopted 2000 Monte Carlo (MC) simulations [34] varying the WF of devices according to a Gaussian distribution considering a 3σ deviation. The reference values from ASAP7 technology for electrical simulations are shown in Table II.

The WFF level for all simulations were ranged from 1% to 5% with 1% steps on nominal values [37]. For each step on WF variation, all simulations were carried from 0.1 V to 0.7 V supply voltage, with 0.1 V steps. This work adopts as a figure of merit the deviation provided by the normalized standard deviation (σ/μ) to allow a comparison of designs with different means and standard deviations. This metric represents the sensibility of a cell to process variability, where the lower it is, the highest is the robustness of the circuit to the impact of process variability. Thus, for all experiments, it is observed the mean (μ), the standard deviation (σ) and the normalized standard deviation (σ/μ) for the delays, energy consumption, and hysteresis interval. The noise margins, slopes, and output gains is shown as well, although, without the analysis of the impact of process variability.
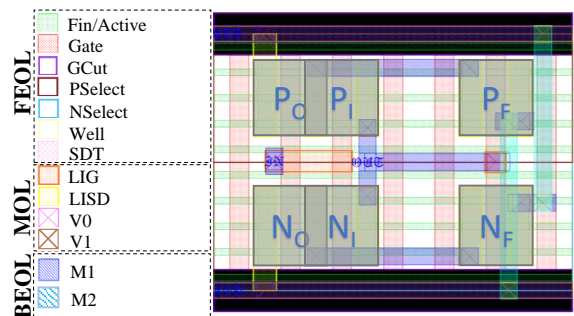

Fig. 2 Technology layers and 3-fins transistors 6T ST layout

The noise margin values were calculated following Equation 1 where V_{IL}, V_{OL}, V_{OH}, and V_{IH} values were extracted from the VTC curve points where the derivative/slope is -1. The slopes were calculated following the Equation 2, while the output gains were extracted from the maximum derivative value. The output gain can be understood as a measure of a circuit's ability to increase the amplitude of a signal from the input to the output. Given so, in an ideal scenario, even a small change in the input signal should bring a considerable change in the output signal value. The output slope describes, in average, how fast the output will change its value concerning the input changing its value as well.

$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH} \quad (1)$$

$$Slope = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad (2)$$

It is considered a scenario where the Device Under Test (DUT) receives the signal passing through two inverters in series and having a 1 fF output capacitance. It is essential to consider some details such as: the same supply voltage is applied in the entire test-bench, only the DUT suffers from variability, the inverters are the same (3-fins transistors) for all experiments, and they are, like the DUT, simulated from the extracted layout.

Due to the variability impact, a circuit may present performance degradation. This work considers a 10% maximum failure threshold in the Monte Carlo simulations to determine the maximum frequencies for the evaluated layouts. Failures are defined as cases where a pair of operations (high-to-low and low-to-high) propagation times do not fit into the determined frequency. In the case of a number of failures above 10%, the frequency is decreased. If the frequency falls below 50 kHz, it is considered to be a non-viable scenario. The value is arbitrary, and it was chosen considering the usage of resources and time for the respective simulations.

A. ST technique on Full Adders

To provide an analysis of the impact of the replacement of FAs internal inverters with STs, it was considered four different types of Full Adders topologies to evaluate their robustness to process variability. In order to analyze such impact, all FAs were analyzed with the same sizing (3 fins), each FA have 3 versions: the traditional (internal inverters not replaced), the FA with its internal inverters replaced by LPST, and the FA with its internal inverters replaced by the 6T ST. It is considered only one level of variability of 5% WFF, following a Gaussian distribution, and there is considered two levels of supply voltage: nominal (0.7 V) and near-threshold (0.4 V).

The Full Adders listed below have been chosen due to their promising results in related and previous works [17, 19]. All FAs designs are shown in Fig. 3, with the respective internal inverters to be replaced by the LPST, and 6T ST highlighted in red: Complementary MOSFET Mirror Adder (Mirror), Transmission Gate Adder (TGA), Transmission Function Adder (TFA), and Hybrid Full Adder.
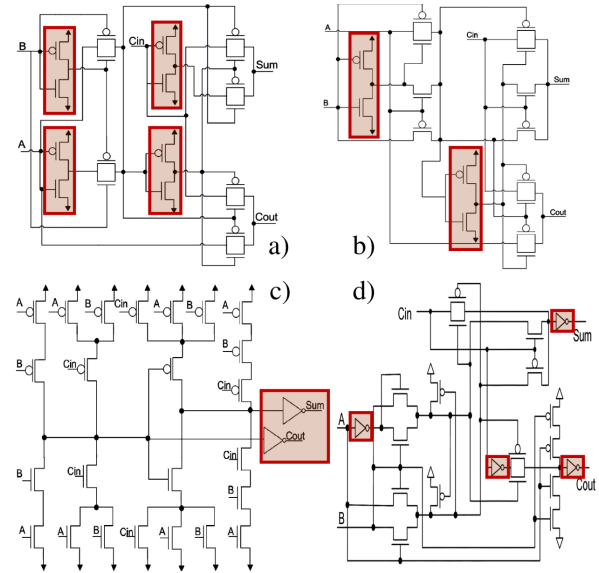

Fig. 3: Full Adders with internal inverters to be replaced highlighted. Transmission Gate Adder (a), Transmission Function Adder (b), Mirror CMOS Adder (c) and Hybrid Full Adder (d).
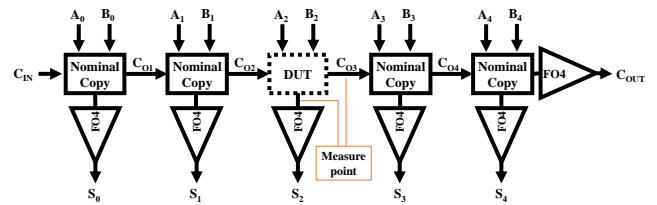

Fig. 4 Test-bench for the Full Adders simulation.

For the metrics, it was considered the mean, the standard deviations, and the normalized standard deviations for the energy and delay measures. The test-bench applied consists of a 5-bit Ripple Carrier Adder with each output (Sum outputs for each FA and last Carry Out) connected to a fan-out of 4 inverters, with the FA in the middle as the DUT, as shown in Fig 4. In this analysis, the FAs have a FO4 output capacitance simulated with a larger Inverter connected to the SUM output. To extract the delay and energy measures, an input vector was applied to trigger a pair of transitions (high-to-low and low-to-high) for each output (Sum and Carry Out) in relation to each input (A, B, and C).

V. ANALYSIS OF INVERTER DESIGNS

A. Frequency and Delays

As the variability level scaled and the supply voltage decreased across the simulations, to maintain the percentage of failures below 10%, the circuit's frequency was reduced. For the traditional inverter, 6T ST, and SIG, the considered *non-viable* scenarios (when the viable frequency of operation is below or at 50 KHz) started to appear at 200 mV, for any scenario above 4% WFF, and 100 mV for any scenario above 5% WFF.

The TIST presented a particular behavior, with its hysteresis interval growing too large as supply voltages increased. The TIST got the same subset of *non-viable* scenarios of the previous designs, although due to its hysteresis, sub- to near-threshold supply voltages did not work correctly.

The TIST 2:1 designs did not present any viable scenarios at 0.2 V and 0.3 V, with only low-variability scenarios (1% and 2% WFF) working at 0.4 V and 0.5 V. The TIST 3:1 designs presented a slight improvement with viable scenarios at 0.2 V and 0.3 V at 1% WFF. For 0.4 V and 0.5 V, the TIST 3:1 presented to be more viable, although not working at a high to medium level of variability (3% 5% WFF).

On average, the 6T ST, SIG, and TIST 2:1 maximum frequencies stayed at about half the inverter frequency (47.61%, 50.50%, and 49.71%, respectively). The TIST 3:1, due to its wider transistors, capable of higher currents, less resistance, and lower hysteresis (as will be shown further on), presented on average 65.72% of the inverter frequencies. The difference between the other designs and the traditional inverter is higher at near and sub-threshold supply voltages.

The decrease in the operating frequencies of the inverters, in comparison to the traditional CMOS inverter, happens due to the hysteresis effects of the 6T ST and TIST designs and the higher parasitics present in designs with a higher number of transistors, vias, and wire length, and the effects of threshold voltage variations into the circuit's behavior. There are scenarios where, due to variability, the threshold voltage will increase, making the transistor switching process slower. Given so, the frequency at which the circuit is working must englobe the worst-case scenarios.

The frequency decrease over the variability levels considering the average value, for all the voltage range considered, is shown in Fig. 5. A robust design must maintain its frequency level as high as possible, even as the influence of process variability on circuit metrics arises from sizing or supply voltage tuning. For this reason, considering the impact of variability on the frequency retention, the inverter, 6T ST, SIG, TIST 2:1, and TIST 3:1 presented 40.03%, 48.81%, 48.20%, 59.40%, and 53.17% average frequency decrease. The decrease is calculated by comparing a best-case scenario (1% WFF) with a worst case scenario (5% WFF) circuit frequency at the same supply voltage. Although, if the designer concern is propagation delay, the traditional inverter is the best choice considering the high speed operation reached with this circuit. Even in its worst-case scenario, traditional INV is still much faster than the SIG and ST alternatives.
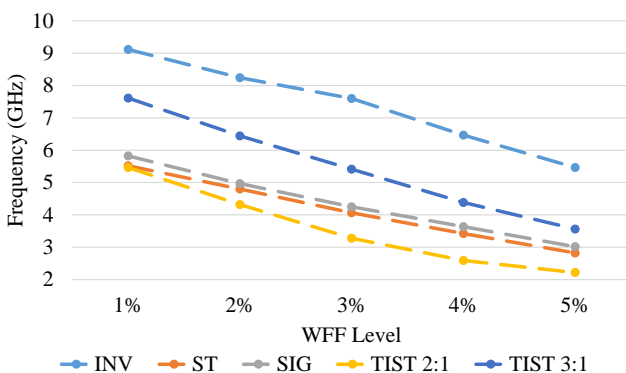

Fig. 5 Frequency decrease over variability scaling for each design.

Related to the frequencies, the propagation times will deviate according to the threshold voltages variations and their effects on the currents. Propagation times deviations will directly influence the circuit frequency, increasing the time guardband necessary to include the worst cases at the circuit frequency.

Given so, propagation times deviations for each design compared to the inverter was 36.36% and 43.21% lower, for the 6T ST and SIG, while the TIST 2:1 and 3:1 designs presented 72.89% and 103.26% higher deviations, as shown in Fig. 6. These results are calculated considering the normalized deviation for all scenarios, even when the design did not work correctly, to do not deflate the results for the TIST designs.

Calculating the average normalized deviations only considering the cases where each design works properly puts the inverter at the lowest normalized deviation while the 6T ST, SIG, TIST 2:1, and TIST 3:1 presented 8.54%, 7.04%, 146.15%, and 36.28% higher sensibilities. By calculating the average normalized deviation this way, a fair comparison can be made between designs, given that only the subset of scenarios, where all designs work, is considered.

B. Energy Consumption

For a circuit operating on a battery-oriented application or even using energy harvesting methods to power itself up, the energy consumption should be stable. Deviation in energy consumption will influence the device battery-life and even leave energy-harvesting circuits non-operational. The energy consumption absolute value should also be as minimal as possible to preserve battery lifetime and make energy-harvesting methods feasible.

Among the considered inverter designs, when comparing average energy consumption measures for the scenarios where each design worked adequately, the 6T ST and SIG presented 173.07% and 50.74% higher energy consumption than the inverter, while the TIST 2:1 and 3:1 designs presented 480.68% and 310.83% increases. With energy being a factor of propagation times (and consequently the frequency) and power drawn from the supply rails, some factors will influence the circuit propagation times or the power consumption. Influencing the propagation times, there is the transistor count, increasing the parasitic capacitances of the circuits, which increases its time to charge/discharge its signal correctly, and for the circuits that present it, the hysteresis effects will make the circuit take longer to change its output value, decreasing its frequency. It influences power consumption, a by-product of how much current is being drawn
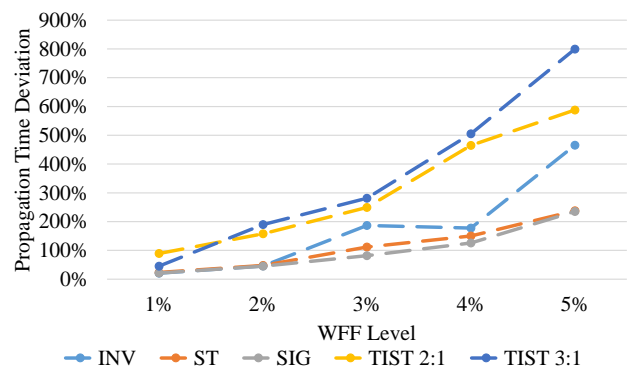

Fig. 6: Propagation times deviation for each design in relation to the WFF level considering all scenarios.

from the supply rail.

When comparing the average energy consumption measures for all scenarios, in comparison to the inverter, the 6T ST and SIG presented 174.21% and 95.84% higher energy consumption, while the TIST 2:1 and 3:1 designs presented 1303.38% and 993.77% increases. This result shows the much higher impact of variability in the cases where the circuits could not work at the minimum frequency of 50KHz, for the SIG and TISTs designs. Given the larger transistor count, the hysteresis effect, and the number of paths from source to ground, it is expected an ascending increase in energy consumption from the inverter, SIG, 6T ST, and TIST designs.

Isolating each variable, the impact of each extra fin starts from a maximum of 145.75% energy consumption increase from 1 to 2 fins to 18.70% from 4 to 5 fins, with diminishing energy increases alongside the number of fins. The higher energy consumption increase at a lower number of fins is due to the higher relative increase in transistor area, given that from 1 to 2 fins, the area is doubled, while from 4 to 5 fins the area increases by 25%, with the SIG presenting the lowest increase overall.

Considering each level of variability, on average, there was a maximum energy increase of 576.60%. Fig. 7 shows the energy increase resulting from the long switching time due to the frequency reduction of circuits to operate at low voltages and large WFF. As shown in Fig. 7, in all cases, it can be observed a descending increase in energy consumption except when increasing the WFF Level from 4% to 5%. Those measures do not consider the supply voltage interval from 0.1 V to 0.2 V since, operating at those voltages, the circuits did not present expected behavior at specific WFF levels. In this analysis, it is possible to observe an unexpected behavior of the TIST 3:1 for 3% and 4% of WFF. One possible reason for this behavior is related to the drastic increase in the number of times the circuit fails to operate at minimum frequency and the fact that we are not removing the outliers values found from the Monte Carlo simulations, to show how process variability can impact severely the circuit operations in specific conditions.

The impact of supply voltage on energy consumption is shown at Fig. 8. Highlighted in blue, for the inverter, 6T ST, and SIG, and in red, for the TIST 2:1 and 3:1, respectively, are the clusters of scenarios operating at the minimum frequency due to the increasing variability impact as supply
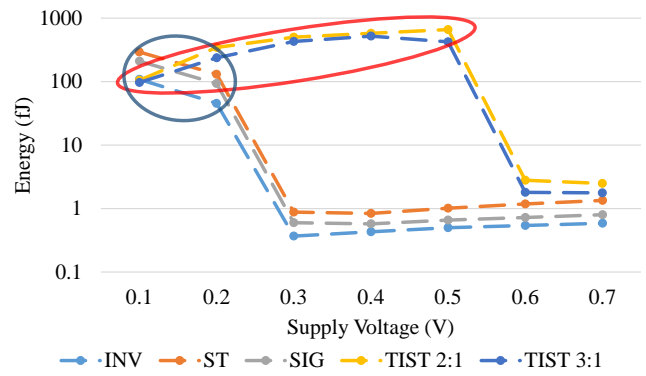

Fig. 8 Energy measures in function of the supply voltage for each design.

voltage decreases. As shown, there are up to 2-order of magnitude increases due to the decrease of supply voltage, revealing sub-300 mV supply voltage operations to be highly susceptible to the variability effects, while the TIST remains at low-frequency operation due to its higher incidence of errors at near and below-threshold operation. This happens due to its exaggerated hysteresis interval, which locks its output signal, making it unable to charge or discharge.

Depending on the focus of the application, there could be several kinds of objectives. Overall, for low energy consumption applications, the focus should be on the circuit design directives to achieve circuits with the minimum possible energy consumption. Much of these directives aim to decrease currents, like the increase of the transistor's channel length and the decrease of supply voltages. Although, such techniques will further decrease the circuit robustness to the effects of variability and radiation.

Given so, trying to achieve a balance between given applications, three types of analysis were performed, where the most appropriate subset of characteristics involving transistor sizing and supply voltage for each level of process variability is identified for the 1) lowest energy consumption, 2) highest robustness to the effects of process variability and 3) the most Cost-Benefit (CB). The lowest energy layout is identified through the energy measures - the product of the supply rail drained current through the simulation and the supply voltage. The higher robustness layout is identified by the lowest normalized standard deviation concerning energy consumption, and the CB layout is identified by the lowest value considering the product between the energy consumption and normalized standard deviation (EDP - Energy Deviation Product). The results are shown in Table III. Some results will show more than one appropriate layout/supply voltage to provide flexibility, considering values up to 5% higher than the minimum considered value.

When isolating the influence of the number of fins and supply voltage over the frequency behavior over variability, it can be observed in Table III clear advantages for fin count above 1 fin and supply voltages above 0.3 V. From 1 fin to 2 fins it was observed an increase of 10.62% over frequency retention. However, above 2 fins, the increase on retention for each extra fin kept steady at 0.77%. For the supply voltage, each 0.1 V increase from 0.1 V to 0.3 V increased the frequency retention by 3.66%, while each 0.1 V increase from 0.3 V to 0.7 V improved the frequency retention by 13.79%,
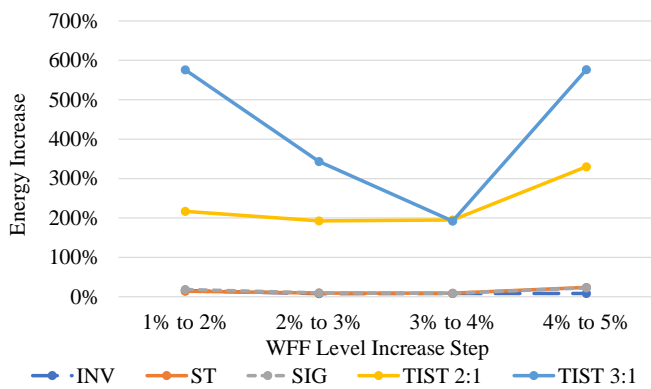

Fig. 7 Energy increase for each WFF level step.

Table III.: Recommended layout and supply voltage for each design and variability level.

Design	WFF	Minimum Energy		Highest Robustness		CB	
		Supply (V)	#Fins	Supply (V)	#Fins	Supply (V)	#Fins
INV	1%	0.1	1 or 2	0.7	1	0.7	1
	2%	0.1	1	0.3	4 or 5	0.2	2 to 4
	3%	0.2	1	0.3	5	0.3	3 to 5
	4%	0.3	1 or 2	0.4	5	0.4	5
	5%	0.3	1	0.4	1	0.4	1
6T ST	1%	0.1	1	0.7	5	0.7	1
	2%	0.2	1	0.7	5	0.7	1
	3%	0.2	1	0.7	4 or 5	0.3	1
	4%	0.3	1	0.4	2	0.4	1 or 2
	5%	0.4	1	0.5	2 to 5	0.5	1 or 2
SIG	1%	0.1	1	0.7	2	0.7	1
	2%	0.2	1	0.3	3 or 4	0.7	1
	3%	0.2	1	0.3	3	0.3	1
	4%	0.3	1	0.4	3	0.4	2 or 3
	5%	0.4	1	0.5	2 or 3	0.5	2
TIST 2:1	1%	0.1	2F1F	0.7	4F2F	0.7	2F1F
	2%	0.1	2F1F	0.6	4F2F	0.6	2F1F
	3%	0.7	2F1F	0.6	2F1F	0.6	2F1F
	4%	0.7	2F1F	0.7	4F2F	0.7	2F1F
	5%	0.7	2F1F	0.7	6F3F	0.7	2F1F
TIST 3:1	1%	0.1	3F1F	0.7	6F2F	0.7	3F1F
	2%	0.1	3F1F	0.7	6F2F or 3F1F	0.7	3F1F
	3%	0.7 or 0.6	3F1F	0.6 or 0.7	6F2F or 3F1F	0.7	3F1F
	4%	0.7 or 0.6	3F1F	0.6	6F2F	0.6	3F1F
	5%	0.7 or 0.6	3F1F	0.6	3F1F	0.6	3F1F

on average. Given so, if performance is a priority, the number of fins should be kept above 2, and if trying to improve robustness, the increase of supply voltage from 0.1 V to 0.3 V will not provide considerable gains.

It is possible to identify patterns concerning the minimum energy and highest robustness layouts. As a general rule, the minimum energy layouts will contain only a few fins, if not only one, and lower supply voltages. Both low values aim to lower currents and increase resistance, therefore decreasing energy consumption. As variability rises, the supply voltage rises as well. That is due to the lower frequencies applied in those scenarios and the consequent increase in propagation times, given that energy is the by-product of power and time. A higher supply voltage will decrease propagation times, followed by a decrease in energy consumption. The TIST designs present a steep increase in supply voltage, from 0.1 V to 0.6 V/0.7 V, due to the lack of possible mid-term (0.2 V to 0.5 V) viable scenarios.

The robust layouts present a shift in supply voltage. At low variability scenarios (1% to 3%), the nominal supply voltage will persist at a nominal value (0.7 V). As the variability level rises, the supply voltage will abruptly fall into the near-threshold region (0.3 V to 0.4 V) and increase as the variability level increases. For the CB layouts, what can be observed is the adoption of supply voltages similar to the high robustness layouts, with earlier adoption of near-threshold supply voltages, as variability rises, and the adoption of a fin count similar to the low energy layouts, although slightly higher.

Considering the averages, for the low energy layouts, the inverter presented the lowest energy consumption, followed by the SIG (34.61% higher), 6T ST (68.32% higher), TIST 3:1 (358.84% higher), and TIST 2:1 (487% higher), respectively. The TIST layouts showed the highest robustness, with the 2:1 variants presenting a 22.93% average energy deviation and the 3:1 variants showing a minor increase with its 23.62% average energy deviation. Following the TIST layouts, the 6T ST, SIG, and inverter present a 29.34%, 33.25%, and 51.55% energy deviation, respectively. However, the inverter presents the highest energy deviation, mainly due to its spike on deviation at 5% WFF.

The energy consumption difference between designs follows the same behavior for the high robustness spectrum, although with much broader differences. Compared to the inverter energy consumption, each design presented an average increase of 43.52%, 263.24%, 382.12%, and 555.21%, for the SIG, 6T ST, TIST 3:1, and TIST 2:1, respectively. The deviation metrics presented a similar behavior, although the 6T ST presented the highest deviations. The TIST designs presented the lowest deviations with 3.56%, and 5.55% for the TIST 2:1, and 3:1, respectively. The SIG, inverter, and 6T ST, presented 6.23%, 6.93%, and 7.81% deviations. In this case, the inverter is a strong candidate, with the lowest energy consumption and acceptable robustness.

Lastly, for the CB layouts, the energy consumption scaling through the designs follows the same pattern, although with smaller differences. Compared to the inverter, the SIG, 6T ST, TIST 3:1, and TIST 2:1 presented average increases of 18.84%, 47.74%, 281.85%, and 379.60%. The TIST designs presented the lowest deviations with 4.07% and 5.80% for the 2:1 and 3:1 proportions, respectively. The SIG, inverter, and 6T ST, presented respectively, 6.72%, 7.05%, and 8.74% deviations on energy. In this case, the SIG presents a higher energy consumption and a much bigger layout; it only provides a minor improvement over deviations (4.91%, relative to the inverter). The 6T ST presented higher energy and a more significant area, with an increase in deviations (1.69%, absolute and 23.97% relative increases, compared to the inverter), although it still presents hysteresis. The TIST designs consume considerably more energy, with less deviation (although, as stated before, those numbers are deflated), more significant layout area, and less viable scenarios to work with it.

It is shown that the CB layouts present similar energy deviations in comparison to the high robustness layouts while maintaining a lower energy consumption, for the 6T ST and SIG, except for the inverter. The inverter presents a high deviation for its minimum energy layout at 5% WFF (1 fin layout with a supply voltage of 0.3 V). Although, with a little increase in supply voltage, from 0.3 V to 0.4 V, matching the CB layout, the inverter presents an 8.95% increase on energy consumption while decreasing its energy deviation by 93.49%. The 6T ST presented similar results at 3% WFF where a 0.1 V increase, from 0.2 V to 0.3 V of supply voltage, provided a reduction of 85.01% in energy deviations while increasing the energy consumption by 7.86%. For the SIG, at 3% WFF as well, it was possible to decrease the deviation by 90.88% while increasing the energy consumption by 22.09%, with the same supply voltage increase performed for the 6T ST.

At the same time, it is essential to analyze the drawbacks of a CB approach. The CB layouts for inverter and TIST layouts presented higher increases in energy consumption than the 6T ST and SIG designs. The higher average increase is directly related to the shift of a supply voltage from 0.1 V to 0.7 V, at 1% WFF. The inverter's supply voltage switch is due to the considerable decrease in energy deviation (from 25.83% to 5.04%) of 5.12x, while the energy consumption

Table IV. Noise Margins for each design as supply voltage scales.

Design	NM (V)	Supply Voltage (V)						
		0.1	0.2	0.3	0.4	0.5	0.6	0.7
INV	NM_L	0.025	0.074	0.122	0.171	0.217	0.253	0.277
	NM_H	0.025	0.073	0.121	0.169	0.216	0.259	0.299
	Avg.	**0.025**	**0.073**	**0.122**	**0.170**	**0.216**	**0.256**	**0.288**
SIG	NM_L	0.025	0.074	0.122	0.171	0.217	0.253	0.277
	NM_H	0.025	0.073	0.121	0.169	0.216	0.259	0.299
	Avg.	**0.025**	**0.073**	**0.122**	**0.170**	**0.216**	**0.256**	**0.288**
6T ST	NM_L	0.036	0.111	0.178	0.244	0.310	0.376	0.440
	NM_H	0.036	0.077	0.111	0.144	0.178	0.213	0.248
	Avg.	**0.036**	**0.094**	**0.144**	**0.194**	**0.244**	**0.294**	**0.344**
TIST 2:1	NM_L	0.061	0.161	0.245	0.292	0.319	0.337	0.359
	NM_H	0.014	0.007	0.010	0.038	0.079	0.131	0.189
	Avg.	**0.037**	**0.084**	**0.128**	**0.165**	**0.199**	**0.234**	**0.274**
TIST 3:1	NM_L	0.051	0.150	0.233	0.277	0.300	0.314	0.341
	NM_H	0.022	0.017	0.022	0.056	0.108	0.173	0.235
	Avg.	**0.036**	**0.084**	**0.128**	**0.167**	**0.204**	**0.244**	**0.288**

Fig. 9 Output gain value across voltage scaling.

increased 3.60x. For the TIST, the higher energy increases are related to the lack of working scenarios at near-threshold and the sudden increase in supply voltage, similar to the inverter. When observing the increases in energy deviations comparing the CB and high robustness layouts, the CB layouts can bring up to a 32% increase in energy deviations, although causing a 79% decrease in energy consumption, highlighting the differences between applications.

C. Noise Margins

The noise margin of a circuit should be as high as possible to provide more noise tolerance. The noise is defined by any extraneous voltage amplitude added to the signal in consideration. The circuit noise tolerance is defined by the circuit's ability to receive this extraneous voltage amplitude summed with the *noise-free* signal without causing it output voltage to deviate from the allowable logic voltage level. In this case, the noise margins were measured considering each design VTCs at different supply voltage levels. This characteristic becomes increasingly critical for low consumption devices, as supply voltage decreases and noise amplitudes, which accounted for only a fraction of the device supply voltage, can now be comparable to the total value of the supply voltage.

The evaluation of the noise margins is shown in Table IV. The inverter and SIG presented identical margins. The TIST designs presented higher margins than the inverter and SIG at sub-threshold levels. The 6T ST presented higher noise margins overall. In comparison to the inverter, SIG, and TIST 3:1 - which presented the same average margin of 0.164V - the TIST 2:1 presented 2.60% lower noise margins, while the 6T ST showed 17.50% higher margins. The 6T ST presents the most significant differences at low supply voltages, with 41.91% and 28.23% higher margins at 0.1 V and 0.2 V, respectively, comparing to the inverter. It is crucial to clarify that the respective NM_L and NM_H appear to be asymmetrical in some cases due to the hysteresis characteristic, which displaces the VTC curve to the right when the input is transitioning from low to high and vice-versa.

D. Output Gains and Slopes

The output gain and slopes will determine how much and how fast the output will change and respond to changes in the input. The gain will measure how much more the output will change its value than a small change in the input. The slopes will determine how fast the output takes to change its
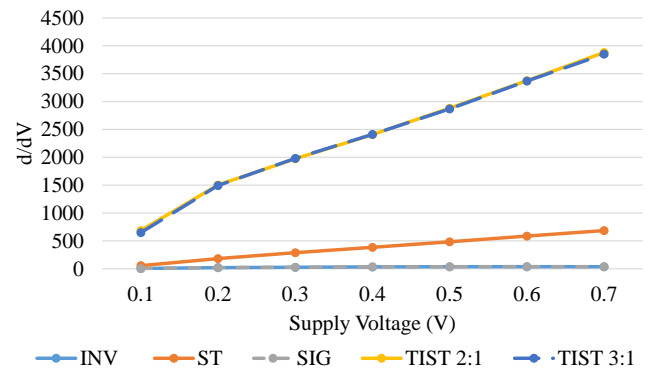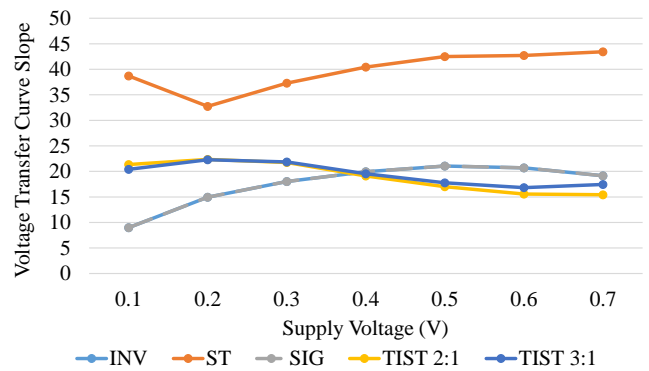

Fig. 10: Voltage Transfer Curve slopes through supply voltage scaling for each design.

value. A circuit can present a high gain, which means that at a specific point in the VTC curve, a small change in the input value is changing the output value drastically. Although, it can present low slope values as well, which means that the time the output takes to change its value is relatively high. In an ideal scenario, the circuit should show both high gains and slopes, making the output change as fast as possible, approaching its output signal to an ideal square signal.

It was considered the output gain values for each design, as shown in Fig. 9. These measures present the most broader difference across all designs. The TIST and 6T ST designs presented, on average, values up to 8300.60%, and 1246.50% higher, respectively, in comparison to the inverter and SIG designs, which presented the same gains. Furthermore, the curve slope measures are shown in Fig. 10, where lower slopes can be observed for the TIST, SIG, and inverter designs compared to the 6T ST. The 6T ST and TIST designs presented 126.24% and 9.43% higher average slopes, respectively, compared to the inverter and SIG designs that showed identical measures.

E. Hysteresis

For the designs that present it through circuit-level methods, the hysteresis characteristic will improve the circuit noise margins through the insertion of upper and lower threshold voltages. The hysteresis does not improve the noise margins through enhancing the signal - by making it closer to an ideal square signal - although, through the two threshold voltages, it will make necessary higher noise am-
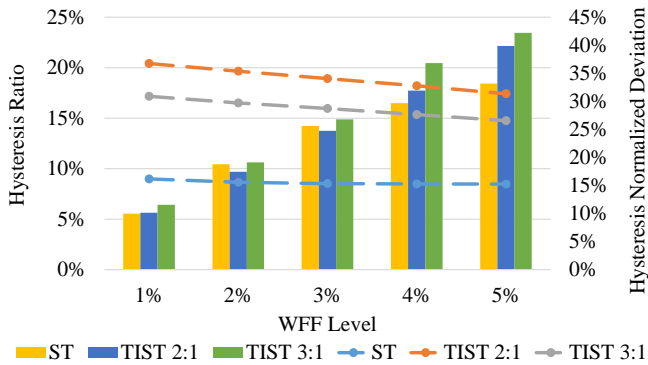
Fig. 11: Design hysteresis ratio comparison (left, doted lines) and hysteresis ratio normalized deviation (right, bars), across variability scaling.

plitude to kickoff the value change of the output signal.

The hysteresis ratios averages across all considered supply voltages for all designs, which present hysteresis, are shown in Fig. 11. The hysteresis ratio is the ratio between the hysteresis interval (V) and the supply voltage (V), which will result in a percentage of the current supply voltage. Given so, the TIST designs presented higher average ratios of 18.92% and 15.95% for the 2:1 and 3:1 designs, respectively, with the 6T ST presenting an average ratio of 8.62%. It is important to highlight the ratio losses as well, the TIST designs presented ratio decreases up to 14.68%, and the 6T ST presented a better response with a 5.68% decrease.

The average hysteresis ratio deviations for each design were 23.44%, 24.83%, and 27.30% for the 6T ST, TIST 2:1, and TIST 3:1. The hysteresis average ratio deviation measures did not present considerable differences between designs, although, at high variability scenarios (5% WFF) the 6T ST presented 16.79% and 21.40% lower deviations, in comparison to the TIST 2:1 and TIST 3:1, respectively.

VI. FULL ADDERS

The results are divided into two primary analyses, with the set of FAs operating at nominal and near-threshold. In both cases, simulations were performed with and without the ST technique. To better present the improvements (positive values) and drawbacks (negative values) of each ST, it also shows a comparison (Δ) between the normalized deviation between the traditional and the circuits with the applied technique. For the sake of simplicity, the LPST and traditional 6T ST were renamed ST1 and ST2, respectively.

A. Nominal Operation

The results concerning propagation times at nominal levels are shown in Table V. The propagation times deviation remains almost the same for ST1 the TFA and TGA due to the pass-transistor logic and low transistor number of the ST1. Although, for the ST2 variants it can be noted a huge increase in not only deviation but absolute values as well. The only exceptions are the Hybrid, which presented higher deviation increases both for ST1 and ST2 designs, and the Mirror FA presenting minor improvements given its mirroring-based logic with many paths to source and ground.

For the energy results, it was observed considerable improvement over robustness in the Mirror, TFA, and TGA, as shown in Table VI, despite the increase on the mean energy measured. There was a considerable worsening over the Hybrid energy robustness. It is mainly due to its number of transistors, comparable to the Mirror FA, but it is not entirely based on complementary logic, and the four internal inverters replaced, further increasing its area and signal degradation. Overall, for designers that prioritize energy regularity, the adoption of ST based approaches can reduce the impact of process variability on energy consumption. The traditional TFA presented the best performance and, by far, the lowest energy consumption and energy normalized deviation at nominal operation. However, it presented the highest delay deviations.

B. Near-Threshold Operation

At near-threshold operation, observing mean and standard deviation, the traditional Mirror is the best alternative considering delay, and the TFA presents a low power solution with considerable energy reduction and low standard deviation. However, considering process variability, during the operation at reduced voltage, slopes and voltage gains are decreased. Given so, the designs make full use of the STs' better signal characteristics, as shown in Table VII. It can be observed a superior robustness improvement with the ST2, given its smaller area, and consequently, lower signal degradation. In the case of the TFA it seems that due to its few paths to source and ground, the higher parasitic capacitance and resistance present in ST2 brings higher deviation, with the ST1 presenting better results.

For the energy results, shown in Table VIII, ST1 showed superior robustness improvement for the TFA and TGA, which can be explained by their pass-transistor-based logic the ST1 smaller parasitics, in comparison to the Mirror and Hybrid FAs, which showed no improvement whatsoever.

Table V. Delay measures for nominal voltage operation

FA	ST	Delays							
		SUM				CARRY OUT			
		μ(ps)	σ(ps)	σ/μ(%)	Δ(%)	μ(ps)	σ(ps)	σ/μ(%)	Δ(%)
Mirror	-	22.83	4.82	21.11	-	22.60	4.39	19.44	-
	ST1	27.38	5.75	20.98	0.6	25.31	4.79	18.94	2.59
	ST2	42.28	8.57	20.28	3.93	41.48	7.96	19.19	1.26
TFA	-	20.76	5.51	26.54	-	19.75	4.70	23.82	-
	ST1	24.24	6.43	26.52	0.09	22.50	5.51	24.50	-2.87
	ST2	42.36	76.87	181.49	-583.82	26.91	6.86	25.48	-6.97
TGA	-	21.56	4.30	19.92	-	22.96	4.70	20.47	-
	ST1	25.32	5.36	21.18	-6.31	26.39	5.41	20.51	-0.16
	ST2	97.92	210.62	215.10	-979.55	32.80	7.85	23.92	-16.84
Hybrid	-	24.02	5.31	22.10	-	23.58	4.89	20.73	-
	ST1	60.96	64.91	106.48	-381.86	42.07	21.84	51.91	-150.45
	ST2	69.68	40.87	58.65	-165.40	72.05	25.81	35.82	-72.81

Table VI. Energy measures for nominal voltage operation

FA	ST	Energy							
		SUM				CARRY OUT			
		μ(fJ)	σ(fJ)	σ/μ(%)	Δ(%)	μ(fJ)	σ(fJ)	σ/μ(%)	Δ(%)
Mirror	-	19.30	3.55	18.39	-	27.30	3.99	14.62	-
	ST1	26.80	4.85	18.10	1.61	37.20	5.54	14.89	-1.90
	ST2	36.50	5.50	15.07	18.08	50.80	6.54	12.87	11.91
TFA	-	4.97	1.27	25.57	-	5.15	0.72	13.90	-
	ST1	10.90	1.46	13.35	47.78	10.80	0.98	9.09	34.60
	ST2	17.00	2.02	11.91	53.42	15.30	2.02	13.23	4.82
TGA	-	14.10	3.81	27.00	-	15.70	4.44	28.28	-
	ST1	24.90	6.33	25.42	5.84	26.40	4.21	15.94	43.62
	ST2	32.40	7.49	23.12	14.34	37.60	7.35	19.55	30.85
Hybrid	-	19.30	4.10	21.24	-	26.30	4.55	17.29	-
	ST1	72.50	37.95	52.34	-146.42	94.60	48.21	50.96	-194.67
	ST2	73.20	21.25	29.03	-36.66	95.20	19.89	20.89	-20.82

Table VII. Delay measures for near-threshold operation

FA	ST	Delays							
		SUM				CARRY OUT			
		μ(ps)	σ(ps)	σ/μ(%)	Δ(%)	μ(ps)	σ(ps)	σ/μ(%)	Δ(%)
Mirror	-	103.49	63.18	61.04	-	91.62	55.41	60.48	-
	ST1	119.98	67.63	56.37	7.66	115.50	73.68	63.80	-5.48
	ST2	155.58	67.03	43.08	29.43	153.50	68.89	44.88	25.79
TFA	-	122.48	117.46	95.90	-	111.64	186.41	166.97	-
	ST1	142.18	146.61	103.12	-7.53	118.26	194.03	164.07	1.74
	ST2	215.93	222.26	102.94	-7.34	165.48	335.16	202.53	-21.30
TGA	-	130.43	109.19	83.71	-	114.78	130.53	113.73	-
	ST1	122.99	98.03	79.70	4.79	128.98	101.51	78.70	30.80
	ST2	187.84	125.13	66.61	20.43	164.06	109.19	66.56	41.48
Hybrid	-	115.90	83.02	71.63	-	111.92	82.45	73.67	-
	ST1	187.36	143.80	76.75	-7.15	116.02	71.26	61.42	16.63
	ST2	207.00	168.04	81.18	-13.33	167.50	66.72	39.83	45.93

Table VIII. Energy measures for near-threshold operation

FA	ST	Energy							
		SUM				CARRY OUT			
		μ(fJ)	σ(fJ)	σ/μ(%)	Δ(%)	μ(fJ)	σ(fJ)	σ/μ(%)	Δ(%)
Mirror	-	10.10	3.04	30.10	-	14.10	2.53	17.94	-
	ST1	13.90	4.05	29.14	3.20	18.60	4.25	22.85	-27.34
	ST2	18.40	4.34	23.59	21.64	25.30	5.73	22.65	-26.22
TFA	-	2.62	0.83	31.49	-	2.71	0.37	13.50	-
	ST1	5.67	1.34	23.63	24.95	5.69	0.63	11.02	18.40
	ST2	9.69	2.11	21.75	30.93	8.80	2.59	29.39	-117.65
TGA	-	6.87	1.56	22.67	-	8.11	2.90	35.71	-
	ST1	12.90	2.37	18.39	18.88	13.50	1.86	13.77	61.43
	ST2	16.10	3.09	19.19	15.34	17.30	2.57	14.88	58.35
Hybrid	-	9.66	3.09	31.99	-	12.80	3.17	24.80	-
	ST1	36.40	17.94	49.27	-54.04	45.80	23.63	51.59	-108.07
	ST2	35.40	12.72	35.94	-12.37	46.60	13.84	29.70	-19.77

The Mirror FA showed the lowest means and normalized deviations for the delay results, which is expected, given it is not based on pass-transistor logic, having better driving capabilities. TFA showed the lowest mean for the energy measures due to its pass-transistor logic and lower number of transistors. Although, the TFA presented the highest delay normalized deviations. Overall, the TGA showed the lowest normalized deviations in energy and the highest robustness gains concerning delay and energy measures.

C. Penalties

Since it is considered a technique with a single inverter (2 transistors) by ST1/ST2 (4/6 transistors), it is expected penalties concerning delay, energy, and area metrics. For the delays, it was observed an average 30% and 97% increase for the ST1 and ST2, respectively. Additionally, for the energy, there was a 123% and 176% average increase for the ST1 and ST2, respectively.

Concerning area penalties, the ST1 increased the FAs area by 157.71%, on average, while the ST2 area increased by 52.20%. The ST1 higher increase in area is due to the necessity to use TAP-Cells, which is a technology restriction, to explicitly connect the transistor's bulk to specific points of the circuit or source/ground, making the ST1 cell more prominent than expected. The ST2 does not apply specific bulk connections, although it was necessary to use METAL3 for cell routing, increasing parasitic capacitance and resistance.

Considering all scenarios, there can be observed no delay robustness improvement at nominal operation with the ST1 and ST2 showing, on average, 67.30% and 227.32% worsening on delay robustness, respectively. For energy robustness, at nominal operation, the ST2 presented a considerable average improvement of 9.49% while the ST1 showed an average worsening of 26.19%. For near-threshold operation, ST1 and ST2 showed 5.18% and 15.14% higher delay robustness. For energy robustness, the ST1 and ST2 presented an average 7.82% and 6.22% robustness worsening. It is important to highlight that those results are averages and do not fully represent each circuit's improvement/worsening due to the technique.

VII. CONCLUSIONS

This work presented an evaluation considering the usage of robustness enhancing circuits on specific circuits (FAs) and the study of such circuits at different sizings, deviations, and supply voltages. An analysis was performed considering three designs: 6T ST, SIG, and TIST, with the traditional inverter as a comparative perspective. This analysis's main objective was to show the viability of the replacement of the traditional inverter with the other considered inverter designs for robustness improvement upon the effects of process variability in 7nm FinFET.

The CMOS inverter presented high performance, low energy consumption, and small area while maintaining acceptable robustness, being recommended for high performance and low-noise applications. In parallel, the 6T ST presented a considerable higher gain and higher noise margins, appropriate for high-noise applications. The SIG showed no clear advantage in any one of the analyses, which is believed to be related to the transistor sizing method applied in this work. Lastly, the TIST presented the highest hysteresis ratios and output gains while presenting appropriate measures for slopes and noise margins at the lowest supply voltage of 0.1 V, while also presenting a smaller layout area than the 6T ST and SIG, respectively, showing a promising subject for future works.

This work also explores a method that consists of replacing regular internal inverters with ST inverters to increase the circuit's noise-immunity. Considering a traditional design with concern about power, timing and area, the Mirror Full adder without the ST still is a good choice, with the TFA particularly presenting good outcomes concerning energy consumption. However, process variability robustness should also be added as one of the main metrics to be evaluated when choosing an adequate circuit. The ST technique presents better improvements in near-threshold operation due to the higher variability impact present in such supply voltage. The circuit's type of logic that is used also determines the technique robustness improvement. Pass-transistor based FAs presents better results at NT voltage given the lack of paths to supply and ground to restore its signals. On average, the ST2 presented better results for energy robustness at near-threshold and nominal operations. The technique presents considerable metric and area penalties. Given so, a trade-off analysis should be made according to the purpose of the circuit.

At last, it is essential to stress the weak points of this analysis due to model limitations. If compared to related works, authors tend to tune the transistors gate length to suppress leakage currents. Although, the ASAP7 FinFET model does not permit gate lengths to be any different from 20nm. To take advantage of gate tuning, the simulations would fall into electrical simulations without layouts being taken into account. As future work, further analysis considering a more

comprehensive range of circuits will be performed in conjunction with different technology nodes. Also it is interesting to trace a trade-off of robustness by area/power, and to provide a comparative evaluation measuring the robustness given a fixed area/power.

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