Phase and Amplitude Control Integrated Circuit in 0.18 μm SiGe BiCMOS for Sub-6 GHz Phased Array Applications

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Abstract—This paper presents simulation results of the C-band transmit/receive (Tx/Rx) phased-arrays integrated circuit (IC) for sub-6 GHz communication links. It is based on 0.18 μm SiGe BiCMOS technology. Phase and amplitude control IC consists of one Tx/Rx channel. Digitally controlled phase shifter allows adjusting relative phase of the output microwave signal in the range from 0 to 360 degrees with 5.625-degree step (6-bit resolution). Digitally controlled active attenuator provides the transfer ratio adjusting from 0 to -31 dB with 1 dB step (5-bit resolution). Amplitude and phase correction system based on the integrated temperature sensor, auxiliary 4-bit phase shifter, 4-bit attenuator, and digital control unit is implemented. Correction in -60 — 85 $^{\circ}\text{C}$ temperature range with the 5-bit resolution is provided. The root mean square (RMS) phase adjustment error does not exceed 1.6 degrees. The RMS attenuation error does not exceed 0.37 dB. The noise figure in Rx mode is below 6.5 dB. The output power in Tx mode is above 6.0 dBm at P1dB. The power consumption is 375 mW and 525 mW in Rx and Tx modes, respectively.

Index Terms—AESA, BiCMOS, C-band, core chip, SiGe

I. INTRODUCTION

Active electronically scanned arrays (AESA) are widely represented in the military-industrial complex. Radars, radio navigation and electronic warfare systems are built on their basis. Extended detection ranges are attainable for AESA as compared to mechanically steerable antennas. They are more reliable than their mechanical counterparts. AESA provides reduced maintenance efforts.

Till present AESAs were less implemented for radio frequency communication systems. Civil applications of this technology in particular for future fifth-generation (5G) cellular networks are limited by the high cost of the system. It is principally defined by the number of active transmit/receive (Tx/Rx) modules based primarily on the high-cost A3B5 microwave monolithic integrated circuits.

Application of integrated transceivers (core chips) based on silicon (Si) or silicon-germanium (SiGe) technologies can reduce the cost of AESA based systems, especially in mass production. The selection of the SiGe BiCMOS process solves the integration problem of the core chips analog and digital parts and reduces its fabrication cost. Moreover, SiGe technologies have better power added efficiency as compared with standard CMOS processes. This parameter vastly affects the performance of the core chip.

During recent years research and design of the integrated beamformers have become a highly relevant field for scientists involved in radio- and microwave integrated circuit design for 5G transceivers implementation [1].

Thus sub-6 GHz band, where wireless communications are currently operated, provides a good tradeoff between the main characteristics of the communication equipment:

size, area coverage, and capacity. As can be seen from [1], most countries will use some frequency ranges in the 3.3—7.1 GHz band. While spectrum above 6 GHz will provide additional capacity and higher data rates.

Unfortunately, complex multifunctional MMICs for amplitude and phase control in phased-array systems based on Si and SiGe technologies for sub-6 GHz applications are not yet widely represented on the global semiconductor industry market [2]—[20].

The design of the Tx/Rx phase and amplitude control integrated circuit for sub-6 GHz active electronically scanned arrays in 0.18 μm SiGe BiCMOS technology is presented in this paper.

II. CORE CHIP DESIGN

Block diagram of the designed phase and amplitude control IC is shown in Fig. 1.

Fig.1 Simplified block diagram of the core chip

A three-port “common leg” architecture [21] is used in the designed core chip. Digitally controlled attenuator (ATT-1) provides the possibility to adjust the transfer ratio of the circuit in the range from 0 to -31 dB with 1 dB step (5-bit resolution). Digitally controlled phase shifter (PS-1) allows adjustment of the relative phase in the range from 0 to 360 degrees with 5.625-degree step (6-bit resolution). Commutation between Rx and Tx modes is provided by single pole double throw microwave switches (SW-1, SW-2, SW-3). Low noise amplifier (LNA) and power amplifier (PA) compensate losses in receive and transmit paths and provide additional amplification while processing the microwave signal. Integrated temperature sensor (TS) as a part

of parameters correction system generates temperature-dependent voltage and converts it into digital codes. Based on these codes, the digital control unit (DCU) generates the control signal for changing states of auxiliary phase shifter (PS-2) and attenuator (ATT-2).

A. Phase shifter

Digitally controlled phase shifters are designed following integrated vector modulator topologies. Designed phase shifter consists of single to differential input converter (S2D), PS core, and digital to analog converter (DAC). It provides 360 degrees phase adjustment range with the 5.625-degree step. Schematic diagram of the PS core is shown in Fig 2.

Fig.2 Schematic diagram of the phase shifter core

Input S2D converter with gain factor 2.5 dB in the frequency range 3.4—7.1 GHz splits the input signal into differential components. Differential signal from S2D converter passes through voltage to current converter based on differential stage (Q9 and Q12 in Fig. 2). Negative feedback (resistor R8 and capacitor C1) compensates the capacitive input impedance of quadrature signal generator (QSG) I1 (three-stage polyphase filter). Relative phase and amplitude errors of the QSG are below 0.8 degrees and 50 mdB, respectively.

Output microwave signal with the required phase is generated from the quadrature input signal in dual vector adder based on Gilbert cell topology (pairs of transistors Q5 and Q6, Q7 and Q8, Q10 and Q11, Q13 and Q14). Non-linear load (transistors Q1, Q3, Q15, and Q17) compensates non-linear PS control characteristic. Output buffer stages (transistors Q19 and Q21) lower output impedance and increase the load capacity of the dual adder. Eight-bit DAC current producing scheme is used to control the gain factor in each of the four channels of the vector adder. Cascaded current mirrors are used to define the value of DAC current resolution.

Parasitic amplitude modulation of the PS output signal is eliminated by the amplitude error correction scheme. A non-linear control signal is produced by the digital control interface to decrease parasitic amplitude modulation according to post-layout simulation results from 3 dB to 0.2 dB.

Phase and amplitude root mean square (RMS) errors of the designed PS in the operating frequency range are below 1.5 degrees and 0.3 dB, respectively.

B. Attenuator

Digitally controlled main ATT is based on programmable gain amplifier (PGA) topology [22]. It consists of the PGA core and gain control circuit. Simplified schematic diagram of the PGA core is shown in Fig. 3.

Fig.3 Schematic diagram of the attenuator core

PGA core consists of differential stage based on transistors Q2, Q4, and resistive load R1 and R2. Transfer ratio of this stage depends on the bias current, which is provided by the exponential current generator Q5. Use of the cross-coupled floating-emitter transistor dummy pair Q1 and Q3 expands the dynamic range of the PGA at high frequencies for high attenuation states. Buffer stages at the output of the PGA core provide matching to the next functional block of the core chip. Temperature compensation circuits are integrated into the gain control circuit to diminish the changes in the transfer ratio of the PGA core.

Main ATT-1 attenuation range is around 31.3 dB. Transfer ratio unevenness is lower than 1.5 dB. Absolute attenuation error does not exceed 0.5 dB, RMS error is lower than 0.18 dB in the operating frequency range.

C. Switches

Single pole double throw switches schematic diagram (see Fig. 4) is based on two series-connected transistors (M1, M2) and parallel-connected shunt transistors (M3, M4). These transistors are controlled in pairs: M1 with M4, and M2 with M3. Time of switching between Rx and Tx modes is below 0.5 ns. Insertion losses are less than 2.1 dB. Isolation between channels is above 37 dB. Input and output return losses are better than 15 dB. Output 1 dB compression point is around 10.7 dBm.

Fig.4 Schematic diagram of the microwave switch

D. Amplifiers

Simplified schematic diagram of the LNA is shown in Fig. 5. Input impedance matching with 50 Ohm port impedance in a wide frequency range is provided by the power limiter functional block [23].

Fig.5 Schematic diagram of the low-noise amplifier

LNA provides higher than CMOS-based analogues [24] signal gain (around 20 dB) with a comparable noise figure of about 4.5 dB according to post-layout simulation. The unevenness of the transfer ratio in the operating frequency range does not exceed 0.5 dB. Input 1 dB compression point is about -8.8 dBm. Power consumption from a 5 V voltage source is 13.8 mW.

The medium power amplifier (see Fig. 6) provides minimally distorted core chip output signals with the required power level. PA circuit includes common-emitter amplifier stages (first and third stages) and common-collector scheme (second buffer stage). Negative feedback resistors R6, R7 provide temperature stabilization and first stage biasing. The opportunity to switch to standby mode is implemented on transistors Q1, Q2.

Fig.6 Schematic diagram of the power amplifier

Class A power amplifier provides more than 30 dB signal gain with 1 dB compression point around 8 dBm and 5.8 % power added efficiency in the frequency range 3.4—7.1 GHz. Power consumption from the 5 V voltage source is 250 mW.

E. Parameters correction system

Core chip parameters correction system based on DCU, integrated TS, auxiliary PS and ATT is implemented for ensuring high accuracy of the phase state and attenuation setting regardless of chip temperature and technology process variations [25].

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DCU controls the condition of the main and auxiliary phase shifters and attenuators based on the external digital codes and TS measurements data. Communication between the core chip and external control device (microcontroller) is provided via a serial peripheral interface.

Auxiliary PS-2 and ATT-2 are schematically similar to the primary amplitude and phase control blocks. Auxiliary circuits provide reduced resolution and range of the output signals adjustment to 4 bits, 8 degrees, and 4 dB, respectively.

F. Layout

The layout of the designed core chip is shown in Fig. 7. The core chip layout area with input/output pads, electrostatic discharge protection circuits, and seal-ring does not exceed 6.0 mm². Since the variability of the individual devices built on the chip is the most critical to mixed-signal IC layout design segmenting and interweaving techniques are implemented to cancel such variations. A common centroid technique is also applied to reduce negatory effects on the designed IC.

Fig.7 Designed core chip layout

III. SIMULATION RESULTS AND DISCUSSIONS

Complete core chip post-layout simulation includes modeling of the IC packaging, which consists of complex routing, interconnections, and embedded passives [27]. The parameterized model of the 24 lead quad-flat no-leads (QFN) package was configured and simulated with AWR Analyst tool.

Frequency dependencies of the core chip Rx/Tx-mode characteristics are shown in Fig. 8—15.

Fig.8 Rx-mode S-parameters and noise figure for 0 dB attenuation and 0° phase shift state of the designed core chip

Rx-mode transfer ratio unevenness is below 1.5 dB in every 1 GHz band for 3.4—6 GHz frequency range. Input and output return losses are better than 8 dB in 3.4—7.1 GHz frequency range. Noise figure for all phase states does not exceed 6.4 dB.

Fig.9 Rx-mode output 1 dB compression point (P1dB) and output third order intercept point (OIP3) for 0 dB attenuation state

Rx-mode output P1dB is above -27 dBm while OIP3 exceeds -10 dBm.

Fig.10 Rx-mode frequency dependence of the absolute phase error from the control code

Rx-mode absolute phase error does not exceed 7° in the entire frequency range. Calculated rms phase error is around 1.5°.

Fig.11 Rx-mode frequency dependence of the absolute attenuation error from the control code

Rx-mode absolute attenuation error does not exceed 0.8 dB in the entire frequency range. Calculated rms attenuation error is around 0.19 dB.

Fig.12 Tx-mode S-parameters for 0 dB attenuation and 0° phase shift state of the designed core chip

Tx-mode transfer ratio unevenness is below 2.5 dB in every 1 GHz band for 3.4—6.5 GHz frequency range. Input and output return losses are better than 9 dB in 3.4—7.1 GHz frequency range.

Fig.13 Tx-mode output 1 dB compression point (P1dB) and output third order intercept point (OIP3) for 0 dB attenuation state

Tx-mode output P1dB is above 2.8 dBm in the entire frequency range while OIP3 exceeds 26 dBm.

Fig.14 Tx-mode frequency dependence of the absolute phase error from the control code

Tx-mode absolute phase error does not exceed 6° in the entire frequency range. Calculated rms phase error is around 1.6° .

Fig.15 Tx-mode frequency dependence of the absolute attenuation error from the control code

Tx-mode absolute attenuation error does not exceed 1.2 dB. Calculated rms attenuation error is around 0.36 dB.

Tx-mode timing diagrams are shown in Fig. 16—17.

Fig.16 Tx-mode timing diagram of the main attenuator digital control

Most significant parameters that characterize beam-former IC are shown and compared with the nearest known analogues in Table 1.

Rx/Tx-mode phase shifter and attenuator switching time does not exceed 40 ns.

Fig.17 Tx-mode timing diagram of the main phase shifter digital control

Table I. Phased arrays core chips comparison.

	[28]	[29]	[30]	[28]	This work
Freq. range (GHz)	2—4	2.5—4	4.5—6.5	5.3—5.5	3.3—7.1
Tx/Rx gain (dB)	8	33	−12	15/5	34.4/21.5
Rx NF (dB)	n/a	2.5	n/a	4.8	<6.5
Tx OP1dB (dBm)	0	20	20	24	6.7
RMS phase error ($^\circ$)	n/a	1.5	2	1	<1.6
RMS attenuation error (dB)	n/a	0.7	0.5	0.3	<0.37
Tx/Rx channel isolation (dB)		n/a	40	n/a	>64
P _{DC} Tx/Rx (mW)	75	5400	100	n/a	375/525
MMIC area, mm ²	3.9	29.9	17.94	n/a	6
Technology	0.13 μ m CMOS	GaAs pHEMT	0.18 μ m GaAs pHEMT	CMOS	0.18 μ m SiGe BiCMOS

IV. CONCLUSION

Output signals amplitude and phase control is carried out through changing states of the digitally controlled phase shifters and attenuators. IC parameters correction system based on the integrated temperature sensor, auxiliary phase shifter and attenuator allows ensuring the stability of the core chip characteristics in the wide range of operating temperatures.

The achieved value of the noise figure in Rx-mode according to the post-layout simulation results is below 6.4 dB. Output 1 dB compression point in Tx-mode is above 2.8 dBm in 3.4—7.1 GHz frequency range. Power consumption in Rx and Tx modes does not exceed 375 mW and 525 mW, respectively. The core chip layout area is 6.0 mm².

Accuracy of the technological library models used in the design flow approaches to the design selected circuitry and

layout solutions, as well as stability of the technological process, make it possible to predict affirmative results right after the first iteration of the production of the integrated circuits.

Original block and schematic diagrams of the core chip functional blocks allow reaching characteristics comparable to the best nearest known analogs of the microwave phase and amplitude control integrated circuits designed in Si and SiGe processes.

ACKNOWLEDGEMENTS

The reported study was funded by RFBR, project number 19-37-90128.

REFERENCES

- [1] I. A. Rumyantsev and A. S. Korotkov, "Survey on Beamforming Techniques and Integrated Circuits for 5G Systems," in *2019 IEEE International Conference on Electrical Engineering and Photonics (EEEPolytech)*, St. Petersburg, Russia, Oct. 2019, pp. 76–80, doi: [10.1109/EEEPolytech.2019.8906842](https://doi.org/10.1109/EEEPolytech.2019.8906842).
- [2] T. Hagiwara, S. Shinjo, M. Kagano, and E. Taniguchi, "An L-band SiGe BiCMOS core chip MMIC for transmit/receive modules," in *2014 9th European Microwave Integrated Circuit Conference*, Rome, Italy, Oct. 2014, pp. 73–76, doi: [10.1109/EuMIC.2014.6997794](https://doi.org/10.1109/EuMIC.2014.6997794).
- [3] M. C. M. Soer, E. A. M. Klumperink, D.-J. van den Broek, B. Nauta, and F. E. van Vliet, "Beamformer With Constant-Gm Vector Modulators and Its Spatial Intermodulation Distortion," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 735–746, Mar. 2017, doi: [10.1109/JSSC.2016.2639545](https://doi.org/10.1109/JSSC.2016.2639545).
- [4] J.-C. Jeong, "An S-Band Multifunction Chip with a Simple Interface for Active Phased Array Base Station Antennas," *ETRI Journal*, vol. 35, no. 3, pp. 378–385, Jun. 2013, doi: [10.4218/etrij.12.0112.0400](https://doi.org/10.4218/etrij.12.0112.0400).
- [5] N. Billstrom, H. Berg, K. Gabrielson, E. Hemmendorff and M. Hertz, "T/R "core chips" for S-, C- and, X-band radar systems," *34th European Microwave Conference*, 2004., Amsterdam, The Netherlands, 2004, pp. 1029–1032.
- [6] H. Thiesies and H. Berg, "A phase and amplitude control front end chip in SiGe for phased-array c-band radar applications," in *IEEE MTT-S International Microwave Symposium Digest*, 2005., Long Beach, CA, USA, 2005, pp. 561–564, doi: [10.1109/MWSYM.2005.1516660](https://doi.org/10.1109/MWSYM.2005.1516660).
- [7] F. E. van Vliet and A. de Boer, "Fully-integrated core chip for X-band phased array T/R modules," in *2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535)*, Fort Worth, TX, USA, 2004, pp. 1753–1756, doi: [10.1109/MWSYM.2004.1338936](https://doi.org/10.1109/MWSYM.2004.1338936).
- [8] Sanghoon Sim, Byungjoo Kang, Jeong-Geun Kim, Jong-Hoon Chun, Brian Jang, and L. Jeon, "A four-channel bi-directional CMOS core chip for X-band phased array T/R modules," in *2015 IEEE Radar Conference (RadarCon)*, Arlington, VA, USA, May 2015, pp. 1198–1201, doi: [10.1109/RADAR.2015.7131176](https://doi.org/10.1109/RADAR.2015.7131176).
- [9] A. A. Barov and A. V. Kondratenko, "X-band GaAs MMIC core chip," 2013 23rd International Crimean Conference "Microwave & Telecommunication Technology", Sevastopol, 2013, pp. 70–71.
- [10] P. Lohmiller, R. Reber, P. Schuh, M. Oppermann, and S. Chartier, "SiGe BiCMOS X-band transceiver-chip for phased-array systems," in *2017 European Radar Conference (EURAD)*, Nuremberg, Oct. 2017, pp. 405–408, doi: [10.23919/EURAD.2017.8249233](https://doi.org/10.23919/EURAD.2017.8249233).
- [11] W. H. A. Tang and L. Smethurst, "MMIC Module for a Ku-Band Miniature Airborne Active Array Radar," 2008 IET Seminar on RF and Microwave IC Design, London, 2008, pp. 1–7.
- [12] K. Tsutsumi *et al.*, "A 15GHz 4-channel transmit/receive RF core-chip for high SHF wide-band massive MIMO in 5G," in *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Phoenix, AZ, USA, Jan. 2017, pp. 115–117, doi: [10.1109/SiRF.2017.7874387](https://doi.org/10.1109/SiRF.2017.7874387).
- [13] B. Sadhu *et al.*, "7.2 A 28GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, Feb. 2017, pp. 128–129, doi: [10.1109/ISSCC.2017.7870294](https://doi.org/10.1109/ISSCC.2017.7870294).
- [14] H.-T. Kim *et al.*, "A 28-GHz CMOS Direct Conversion Transceiver With Packaged 2×4 Antenna Array for 5G Cellular System," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, May 2018, doi: [10.1109/JSSC.2018.2817606](https://doi.org/10.1109/JSSC.2018.2817606).
- [15] T. Kanar, S. Zehir, and N. Yanduru, "Ultra-Compact and Modular 5G Phased-Array 4-Channel Beamformer Front-Ends with $<2^\circ$ RMS Phase Error," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, Philadelphia, PA, Jun. 2018, pp. 1327–1329, doi: [10.1109/MWSYM.2018.8439596](https://doi.org/10.1109/MWSYM.2018.8439596).
- [16] J. Pang *et al.*, "A 28-GHz CMOS Phased-Array Transceiver Based on LO Phase-Shifting Architecture With Gain Invariant Phase Tuning for 5G New Radio," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, May 2019, doi: [10.1109/JSSC.2019.2899734](https://doi.org/10.1109/JSSC.2019.2899734).
- [17] J. Pang *et al.*, "A 28-GHz CMOS Phased-Array Beamformer Supporting Dual-Polarized MIMO with Cross-Polarization Leakage Cancellation," in *2020 IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, Jun. 2020, pp. 1–2, doi: [10.1109/VLSICircuits18222.2020.9162882](https://doi.org/10.1109/VLSICircuits18222.2020.9162882).
- [18] J. Pang *et al.*, "21.1 A 28GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR," in *2019 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 344–346, doi: [10.1109/ISSCC.2019.8662324](https://doi.org/10.1109/ISSCC.2019.8662324).
- [19] K. Khalaf *et al.*, "A 60GHz 8-way phased array front-end with TR switching and calibration-free beamsteering in 28nm CMOS," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Leuven, Sep. 2017, pp. 203–206, doi: [10.1109/ESSCIRC.2017.8094561](https://doi.org/10.1109/ESSCIRC.2017.8094561).
- [20] A. Natarajan, A. Valdes-Garcia, B. Sadhu, S. K. Reynolds, and B. D. Parker, "SWS-Band Dual-Polarization Phased-Array Transceiver Front-End in SiGe BiCMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 6, pp. 1989–2002, Jun. 2015, doi: [10.1109/TMTT.2015.2422691](https://doi.org/10.1109/TMTT.2015.2422691).
- [21] A. D. McLachlan and M. Rhodes, "Vector control for airborne phased array radar," in *IEE Colloquium Electronic Beam Steering*, London, UK, 1998, vol. 1998, pp. 2–2, doi: [10.1049/ic:19980869](https://doi.org/10.1049/ic:19980869).
- [22] I. D. S. B. Júnior, R. C. Silverio Freire, and E. D. S. Procopio Venueto, "Design of a Programmable Gain Amplifier (PGA) for Bluetooth Low Energy (BLE) in 0.13 μm CMOS," *JICS*, vol. 15, no. 1, pp. 1–9, May 2020, doi: [10.29292/jics.v15i1.101](https://doi.org/10.29292/jics.v15i1.101).
- [23] V. Budnyaev, I. Filippov, and I. Vetrov, "Microwave Limiter Design in 180 nm SiGe BiCMOS Technology," in *2019 Ural Symposium on Biomedical Engineering, Radioelectronics and Information Technology (USBEREIT)*, Yekaterinburg, Russia, Apr. 2019, pp. 398–400, doi: [10.1109/USBEREIT.2019.8736577](https://doi.org/10.1109/USBEREIT.2019.8736577).
- [24] F. Rangel de Sousa and P. M. Moreira e Silva, "Design, Analysis and Measurement Results of a Fully-Integrated Low-power LNA Presenting Faults," *JICS*, vol. 8, no. 1, pp. 32–42, 2013.
- [25] I. Filippov, V. Vertegel, and Y. Gimpilevich, "Parameters Correction System for Phased Array Front-end Chip," in *2019 Ural Symposium on Biomedical Engineering, Radioelectronics and Information Technology (USBEREIT)*, Yekaterinburg, Russia, Apr. 2019, pp. 401–404, doi: [10.1109/USBEREIT.2019.8736624](https://doi.org/10.1109/USBEREIT.2019.8736624).
- [26] I. F. Filippov, D. A. Snegur, and V. V. Vertegel, "Design of Integrated Temperature Sensor for Aesa Transceiver Parameters Correction System," in *2018 International Conference on Actual Problems of Electron Devices Engineering (APEDE)*, Saratov, Sep. 2018, pp. 487–492, doi: [10.1109/APEDE.2018.8542365](https://doi.org/10.1109/APEDE.2018.8542365).
- [27] H. M. Cavalcanti and L. T. Manera, "A Simulation Methodology for Wirebonds Interconnects of Radiofrequency Integrated Circuits," *JICS*, vol. 10, no. 3, pp. 181–186, 2015.
- [28] *RFCore Product Selection Guide*, RFCore, Seongnam: 2020, 12 p..
- [29] *XZ1001-BD Datasheet*, M/A-COM Tech Asia, Hsinchu, Taiwan: 2010, 11 p..
- [30] *CGY2175BUH/C1 4-Port C-Band Integrated Core Chip Datasheet*, OMMIC, Limeil-Brévannes, France: 2010, 15 p..