Exploring Multi-Level Composition and Efficient SCM Schemes for an Energy-Efficient Wavelet Haar Architecture

Henrique Seidel¹, Morgana da Rosa¹, Guilherme Paim²,
Eduardo A. C. da Costa¹, Sergio Almeida¹, Sergio Bampi²

¹Graduate Program in Electronic Engineering and Computing - Catholic University of Pelotas (UCPel), Pelotas - Brazil

²Graduate Program in Microelectronics (PGMicro) - Federal University of Rio Grande do Sul (UFRGS), Porto Alegre - Brazil

e-mail: {gppaim, bampi}@inf.ufrgs.br, {eduardo.costa}@ucpel.edu.br

Abstract— This work explores multi-level fixed-point Haar transform compositions combined with SCM (single constant multiplication) schemes for an energy-efficient hardware architecture. We investigate a set of six lower-level Haar transforms for composing a Haar-9 architecture. The multiple-level Haar transforms use as a base $M=1$, $M=2$, and $M=3$ resolution levels. The processing module (PM) of the Haar explores efficient SCM schemes. The architectures were described in VHDL and synthesized employing the ST 65nm CMOS cell library. The results show that Haar-II architecture presents the lower circuit area results since this architecture requires fewer arithmetic operators. However, the most energy-efficient Haar-9 hardware architecture employs a combination of two $M=2$ with five $M=1$ blocks with an efficient SCM architecture reduced to only two arithmetic operators.

Index Terms— Haar Wavelet Transform, SCM, Hardware Architectures, VLSI Design.

I. INTRODUCTION

In digital signal processing (DSP) applications, one of the primary operations involves using transforms. In particular, the wavelet transform is a relatively new mathematical approach that has been in evidence recently compared with other classical signal analysis techniques, such as the Fourier transform. The wavelet transform theory has excellent employment in several areas, such as analyzing seismic signals, radar, biomedical, among other applications [1–6].

Haar transform is the simplest among the wavelets [7] from a mathematical point of view. It means that its calculations require fewer arithmetic operations [8]. Due to this characteristic, Haar is suitable and commonly employed for embedded systems since the lesser complexity directly conducts less energy consumption in its hardware architecture implementation. Our key challenge is to reduce the Haar Transform's energy consumption with nine decomposition levels in this work. According to the literature [9], this level of resolution is widely used for practical cases in the adaptive filtering and image or video compression area. The paper in [10] proposed a method that adaptive identifies a frequency-rich sparse impulse response in the Haar-9 domain. The application for image or video compression is presented in [11] that discusses the compensation in terms of hardware cost and error of level 7 and 9 DWT decompositions.

We explore the wavelet Haar-9 transform hardware design in two main directions: (i) the implementations through the interconnection of blocks with lower resolution levels, (ii) the exploration of efficient SCM architectures.

We have developed six levels of decomposition to integrate the Haar level 9, using lower blocks. This significant exploration allows us to identify the most suitable arrangement for low-power design. Mainly, the blocks of Haar-1, Haar-2, and Haar-3 are the base for arranging hierarchical architectures for the Haar-9.

One of the inputs of the multipliers, in the Haar transform, is the H coefficient that is represented by $\frac{1}{\sqrt{2}}$. We implement this term by using shift-addition operation, by exploring SCM (single constant multiplication) approaches. We use SCM solutions generated by prominent Hcub, BHM, and RAG-n algorithms from the Spiral environment [12]. We also offer our solution for the SCM-based Haar architectures.

The main results show that the herein called Haar-VI (with two $M=2$ and five $M=1$ PM modules) combining with our SCM-VI proposal (with two arithmetic operators and critical path equal to 2) presenting the most negligible power dissipation among the explored architectures.

Our contributions presented in this paper are as follows:

1. An extensive exploration of multi-level composition Haar blocks for a Haar-9 transform.
2. The simplification of the Haar coefficients exploring various SCM architectures.

The rest of the paper is organized as follows. Section II makes an overview of the wavelet transform, with particular concern to the Haar transform. The SCM approach and a review of the literature are also presented in this section. Section III shows the proposed Haar architectures for 9-levels of decomposition. The synthesis methodology and the main results are shown in Section IV. Finally, Section V concludes the paper.

II. BACKGROUND

This section initially shows an overview of the wavelet transform. After the main aspects of the Haar transform are presented. It also offers a discussion about the SCM approach and discusses the main work from the literature, and puts into perspective the main contributions of this work.

A. Discrete Wavelet Transform

To obtain the discrete wavelet transforms (DWT) of a sign $f(n)$, the shift and scaling parameters are no longer continuous and become discrete [13, 14]. In general, Equation 1 represents the DWT. In the equation, ψ is the mother wavelet and parameters a and b , which respectively represent scale and translation as a function of the continuous wavelet transform, are functions of the integer parameters m and n , that is, $a = a_0^m$ e $b = nb_0a_0^m$.

$$DWT_{(m,n)} = \frac{1}{\sqrt{a_0^m}} \sum_n f(n) \psi \left(\frac{x - nb_0 a_0^m}{a_0^m} \right) \quad (1)$$

The parameters m and n are integer values, which control the dilation and translation, respectively. The constants a_0 and b_0 are the lengths of the discrete steps, with a_0 being an expansion parameter whose value is greater than 1, and b_0 a location parameter, with a value greater than zero.

Given the definition, the DWT solution consists of dividing the analyzed signal into low-frequency components, called approximation coefficients (A_n), and high-frequency components called detail coefficients (D_n). This division generates two signals with the same number of samples as the original signal, doubling the DWT complexity. Therefore, the decomposition in the DWT goes through a sub-sampling process that guarantees the approximation coefficients and details with half the original signal. Thus, the decomposition process will always act on the approximation coefficients, creating a wavelet decomposition tree shown in Figure 1, for three levels of decomposition example.

Although the example of Figure 1 shows three levels of decomposition, the procedure repeats until reaching the desired resolution level or until the signal becomes a single sample. In practice, which defines the decomposition level is the nature of the signal, or some criterion, such as entropy [7].

Fig. 1: Decomposition wavelet transform tree.

B. Haar Transform

The Haar algorithm is a particular class of the DWT [15], and it has become a valuable tool to solve problems in many science branches. The wavelet on the Haar base was the first proposed in the literature and represents the simplest of the wavelet family's functions. The Haar transform is a set of mutually orthonormal functions whose support domain is '0' to '1', represented in Equation 2.

$$\psi(t) = \begin{cases} 1 & \text{to } 0 \leq t < \frac{1}{2} \\ -1 & \text{to } \frac{1}{2} \leq t < 1 \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

From the mathematical perspective, the wavelet on the Haar basis is discontinuous and resembles a step function, as shown in Figure 2 [7].

The methodology to calculate the DWT consists of designing low-pass (L) and high-pass (H) filters with coefficients according to the chosen wavelet mother function. The

Fig. 2: Haar wavelet function [7]

Equations 3 and 4 show how to calculate the coefficients of approximation and details at the first scale, respectively [16].

$$A_1 = \frac{1}{\sqrt{2}} X_{(2n-1)} + \frac{1}{\sqrt{2}} X_{(2n)} \quad (3)$$

$$D_1 = \frac{1}{\sqrt{2}} X_{(2n-1)} - \frac{1}{\sqrt{2}} X_{(2n)} \quad (4)$$

The Haar transform can also be represented by an orthogonal matrix $N \times N$, called H_N , where $M = 2^N$. The matrices that represent the Haar transform blocks used in this work are presented in Equations 5, 6 and 7, for one, two and three levels of decomposition, respectively.

$$H_2 = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (5)$$

$$H_4 = \frac{1}{2} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ \sqrt{2} & -\sqrt{2} & 0 & 0 \\ 0 & 0 & \sqrt{2} & -\sqrt{2} \end{bmatrix} \quad (6)$$

$$H_8 = \frac{1}{\sqrt{8}} \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ \sqrt{2} & \sqrt{2} & -\sqrt{2} & -\sqrt{2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \sqrt{2} & \sqrt{2} & -\sqrt{2} & -\sqrt{2} \\ 2 & -2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 2 & -2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 2 & -2 \end{bmatrix} \quad (7)$$

C. SCM Operations

In DSP operations, the multiplication operations usually dominate the complexity of the project. This operation is the arithmetic core with the most significant impact on the circuit area, critical path delay, and power dissipation in the hardware design. In circuits with constant values multiplied (such as filters with finite impulse response and fast Fourier transform), using a complex general purpose multiplier is unnecessary if the constants were previously known. Instead, sum and shift operations replace the general-purpose multiplier in an SCM.

The sharing of common partial products, using shifts and sums/subtractions, allows a significant reduction in the number of operations and, consequently, in the circuit area and power dissipation in the SCM operations' design. Thus, the SCM problem consists of finding the minimum number of sums/subtraction operations that implement constant multiplications. The shifts in hardware use only wires, without additional costs in the area.

An example of representing the multiplication by constants using additions and shifts, in a method known as digit-based recoding [17], is shown in Equation 8. Figure 3 shows that the multiplication by a constant can be reduced to a set of shift-adders with less circuit area and reduced critical path, directly impacting power dissipation reduction.

$$\begin{aligned} 29X &= (11101)_{bin} \\ &= 2^4X + 2^3X + 2^2X + 2^0X \\ &= 2^3(2^1X + 2^0X) + (2^2X + 2^0X) \end{aligned} \quad (8)$$

Fig. 3: Single constant multiplication example.

D. Related Work

The Wavelet transform is a mathematical tool with particular characteristics, which has become popular in digital signal processing applications. Mainly, when it comes to reducing power dissipation, the wavelet transforms, in Haar basis, stand out due to its simplicity and low complexity for its implementation. These attributes make it possible to find various works in the most diverse application areas, which use the wavelet transform in the Haar base. The work in [18] treats a new algorithm for fast calculation of the Haar wavelet transform and the possibility of its application in the time-frequency analysis of the waveform. An FPGA-based solution of a de-noising using Haar level 5 wavelet transform was presented in [19].

Other studies propose using the Haar transform as a form of reducing power dissipation, such as in [20] and [21] that present algorithms using the Haar transform to process ECG signals, with a focus on portable devices and remote monitoring of cardiovascular diseases. Still, within the scope of biomedical engineering, the work proposed in [22] uses the Haar wavelet transform for analyzing electroencephalogram (EEG) signals in the detection of drowsiness.

Table I.: Related Work on Haar Wavelet Transform Design.

Related Work	A	B	C	D	E	F
[20–22, 25, 27]	×	×	×	×	×	✓
[23]	ASIC	✓	✓	×	×	✓
[24]	FPGA	×	×	×	×	✓
[28]	ASIC	×	×	✓	×	✓
[29]	ASIC	✓	✓	✓	×	✓
Our	ASIC	✓	✓	✓	✓	✓

(A) Target Device for Results, (B) Power Results, (C) Methodology for Power Analysis, (D) Using different MCM strategies, (E) Exploring hierarchical structures for Haar 9 decomposition, (F) Haar basis.

Another area of application where the Haar wavelet transform concentrates a significant amount of work is image processing and compression. An example is a work presented in [23] that offers an implementation of hardware for image compression, designed to meet the power restrictions of image communication in Wireless Sensor Networks. The work of [24] shows a hardware-oriented image encoding processing scheme based on the Haar wavelet transform.

The majority of the wavelet transform implementations, focusing on energy reduction, seek architectures with lower resolution levels to reduce complexity, and consequently, power dissipation. That is why it is challenging to find works in this area (low power), which implement architectures that reach nine resolution levels. However, it is still possible to see works, such as [25], using the Haar level 9 transform in a project of a sample of analog wavelet processor architecture for cochlear implant application. The work in [26] applies to level 11 of the Haar transform to implement an algorithm to extract important characteristics from fingerprints. Finally, in [27], a new scheme is proposed to identify the flow regime and measure the quality in gas-liquid two-phase using differential pressure signal. The flow regime is determined based on the analysis of a wavelet function in the Haar basis with nine resolution levels.

The solution of [28] proposed a Haar-9 architecture, based on three M=3 blocks, but with no power results. Furthermore, the SCM part uses only Carry Save adders (CSA). This solution was further improved in [29] using efficient adder compressors architectures in both the Processing Module (PM) and the SCM part, for an energy-efficient Haar-9 transform. However, none of both mentioned works explored decomposing in lower resolution blocks than M=3 for the Haar-9 solution, as we are proposing. Furthermore, our work explores more solutions for the SCM part than proposed in [29]. As will be discussed in the Results Section, our best-proposed architecture is more time processing and power-efficient than the best solution of [29]. Table I summarizes the solutions from the literature and puts into perspective the contributions of this work.

III. HAAR WAVELET TRANSFORM HARDWARE ARCHITECTURES

Among all DWTs, the Haar discrete wavelet transform (Haar DWT) is the simplest and most orthogonal. However, a traditional 2D DWT is applied by sequentially performing two 1D operations along the lines and the columns. In this case, there is performance degradation due to memory read and write operations involving intermediate results between row and column operations. For this reason, we propose sequential data entry for a hierarchical algorithm for Haar DWT. Thus, there is no implementation of the Haar matrix using a grid memory. We use adders and multipliers to estimate the levels of decomposition resulting from a convolution process with the Haar coefficients matrix. With this technique, we can implement a 2D Haar DWT by rearranging data, achieving the low memory needed to implement being from $O(N)$.

The proposed Haar architecture uses as bases the solution proposed in [28] for 9-levels of decomposition that used three $M=3$ blocks. However, we extended the solution to Haar-9 using other architectures with fewer resolution levels to find combinations with fewer arithmetic operations. The architectures use as bases three different $M=1$ (Figure 4-a), $M=2$ (Figure 4-b), and $M=3$ (Figure 4-c) Processing Modules (PM). Table II shows the number of additions and multiplications and the critical path for the $M=1$, $M=2$, and $M=3$ PM modules.

Table II.: Arithmetic operators and critical path to Haar transform with different resolution levels [28].

Level	Additions	Multiplications	Critical Path
$M=1$	2	2	2
$M=2$	5	1	2
$M=3$	12	3	4
$M=9$	765	7	10

To calculate the approximation coefficients and details coefficients of the Haar transform, the internal PM architectures, shown in Figures 4-a,-b,-c, include shifts registers, buffers, adders, subtractors, multipliers, and shift operators. Its operation consists of loading the input signal $x(n)$ samples in the shifts registers and storing them in the buffers. A control block, composed of counters and comparators, will be responsible for determining when these values will be available for the operative part to carry out the calculations, thus guaranteeing the down-sampling process present in the filtering. Therefore, the first decomposition needs to be down-sampling by a factor of two. Then, the architecture calculates every two samples that enter the buffer (every two clock cycles). In this way, each resolution level of the Haar transform has a different latency, i.e., each resolution level must wait a certain number of clock cycles to perform its calculation. Table III shows how many clock cycles are needed to calculate each resolution level. The values in Table III show the large number of clock cycles required to implement an entire Haar-9. On the other hand, using lower resolution levels to construct a Haar-9 can be advantageous due to the more reduced clock cycles. This work explores, mainly, the 1, 2, and 3 resolutions levels to design a Haar-9 transform.

Table III.: Latency of each resolution level.

Level	1	2	3	4	5	6	7	8	9
Latency	2	4	8	16	32	64	128	256	512

From Table II, it is clear that $M=1$ and $M=2$ levels are competitive and open a vast space of exploration for a Haar-9. The values of Table II show that these blocks present fewer additions and multiplications and less critical path than the $M=3$ level. On the other hand, Table II shows that implementing an entire Haar with $M=9$ is prohibitive, mainly due to a large number of additions and multiplications required. From these three PM modules ($M=1$, $M=2$, and $M=3$), we offer the architectures in Table IV.

Table IV.: Arithmetic operators and critical path to the proposed Haar architectures

Architecture	#Add	#Mult	Critical Path
Haar-I (Figure 4-d)	18	18	18
Haar-II (Figure 4-e)	22	6	10
Haar-III (Figure 4-f)	45	9	12
Haar-IV (Figure 4-g)	27	6	10
Haar-V (Figure 4-h)	37	9	12
Haar-VI (Figure 4-i)	20	12	14

The Haar architecture's critical path is determined by multipliers, adders, and the circuit's latency. Table IV describes the critical path, the number of multipliers (Mult) and total adders (Add) for the proposed Haar architectures. The Haar-III (Figure 4-f) uses three $M=3$ PM modules as in [28] and [29], with a total of 45 arithmetic operators (45 additions and nine multiplications), and a critical path equal to 12. Note that we consider adders and subtractors as equal since the difference between them is minimal in terms of hardware (the subtractor is easily implemented by inverting the input and adding '1' value to realizing the operation in 2's complement).

The multiplier circuit undoubtedly has the most significant influence on this requirement (critical path) from these elements. Figures 4-a,-b,-c show that, in the Haar architectures, one of the multipliers' inputs is the H coefficient. This coefficient is represented by $\frac{1}{\sqrt{2}}$. For simplifying the implementation of this coefficient, we approximate its calculation according to Equation 9. This equation enables substituting a complicated multiplication by simpler shift-addition operations in an SCM approach.

$$X \cdot \frac{1}{\sqrt{2}} = X \cdot 2^{-1} + X \cdot 2^{-3} + X \cdot 2^{-4} + X \cdot 2^{-6} + X \cdot 2^{-8} \approx X \cdot 0.70703125 \quad (9)$$

The SCM problem consists of finding the minimum number of addition/subtraction operations that implement constant multiplications. The shifts can be performed on hardware using only wires, without additional costs in the area. This work explores several solutions for implementing SCM strategies for the H coefficient calculation in the Haar transform. One solution uses the strategy of [28] and [29]. Some solutions use the algorithms of the Spiral environment [12]. Our solutions use $\frac{\sqrt{2}}{2}$ for the approximation. In this case, we

Fig. 4: Haar wavelet architectures: a) Haar level $M = 1$, b) Haar level $M = 2$ and c) Haar level $M = 3$. Haar level $M = 9$ architectures with lower resolution levels: d) with nine blocks of level $M = 1$, e) with one block of level $M = 1$ and four blocks of level $M = 2$, f) with three blocks of level $M = 3$, g) with three blocks of level $M = 2$ and one block of level $M = 3$, h) with one block of level $M = 1$, one block of level $M = 2$ and two blocks of level $M = 3$ and i) with five blocks level $M = 1$ and two blocks of level $M = 2$.

calculate $\sqrt{2}$ and shift the results one position right to obtain the division by 2. We explored the following SCM strategies to approximate the H coefficient for the 0.70703125 value:

- SCM-I (Figure 5-a): Solution proposed by [28, 29]. The solution involves four arithmetic operators (four additions), with a critical path equal to 3.
- SCM-II (Figure 5-b): Solution generated by H-Cub algorithm [30] from Spiral environment. For this solution, the H coefficient was implemented through the formulation of $181X * 2^{-8}$. The solution involves three arithmetic operators (three additions) and presents a critical path equal to 3.
- SCM-III (Figure 5-c): Solution generated by BHM algorithm [31] from Spiral environment. For this solution, the H coefficient was also implemented by using $181X * 2^{-8}$. It represents three arithmetic operators (one addition and two subtractions), with a critical path equal to 3 (one addition and two subtractions).
- SCM-IV (Figure 5-d): Solution generated by RAG-n algorithm [31] from Spiral environment. For this solution, the H coefficient was also implemented from the formulation of $181X * 2^{-8}$. The solution involves three arithmetic operators (two subtractions and one addition), and presents a critical path equal to 3 (two subtractions and one addition).
- SCM-V (Figure 5-e): Solution proposed in this work. For this solution, the H coefficient was also implemented using the formulation of $181X * 2^{-8}$ and using only three arithmetic operators (one addition and two subtractions). The solution offers a critical path equal to 3 (two subtractions and one addition).

metric operators (one addition and two subtractions). The solution offers a critical path equal to 3 (two subtractions and one addition).

- SCM-VI (Figure 5-f): Solution proposed in this work. This solution uses a different formulation for implementing the H coefficient. We used the formulation of $45X * 2^{-6}$ that involves two arithmetic operators (one addition and one subtraction), and presents a critical path equal to 2 (one addition and one subtraction).
- SCM-VII (Figure 5-g): Solution proposed in this work. This solution also used the formulation of the SCM-VI for the H coefficient implementation, i.e., $45X * 2^{-6}$. This solution involves two arithmetic operators (two subtractions) and presents a critical path equal to 2.

Regarding SCM-VI and VII architectures, there is a reduction of at least one adder about architectures I to V, which drastically reduces power dissipation, energy consumption and increases the architecture's operating frequency, enabling the calculation of a more significant amount of samples per second. There is an error of around 0.56% for the Haar coefficient, i.e., equal to $\frac{1}{\sqrt{2}}$ in the SCM-VI and VII proposed architectures. This small error rate has no impact on the efficiency of Haar-9, as at decomposition level 9, we have a frequency range from 3.90 Hz to 2000 Hz. An error in this magnitude would reduce the frequency range by 11.20 Hz, generating an amplitude ranging from 3.90 Hz to 1988.20 Hz.

Fig. 5: SCM architectures for H coefficient implementation: a) Solution from [28, 29], b) Solution from Hcub algorithm [30], c) Solution from BHM algorithm [31], d) Solution from RAG-n algorithm [31], e-g) Solutions from this work.

IV. RESULTS

This section presents the main results. Initially, we present the methodology for the power results. After, we offer the synthesis results in terms of area, power dissipation, energy per operation (EPO), and fanout. The fanout represents the number of logic gates in the critical path provided by the synthesis tool.

A. Methodology for Synthesis Results

The hardware architectures used industrial EDA tools for standard-cell CMOS hardware design for the syntheses. The architectures descriptions were in VHDL, with the adder inferred by the logic synthesis tool ('+' operator in VHDL). Cadence GenusTM tool performed the RTL to gate-level netlist synthesis and the STA. The architectures were mapped to 65nm standard cells at 1.25V voltage, aiming for their maximum frequency of 1.62GHz (with zero slack value).

Figure 6 shows the methodology for power dissipation extraction. For the simulations of all network lists, we used the Cadence Incisive, considering the SDF file for precise signal propagation delays and temporal glitches. The simulation generates a toggle count format (TCF) file, loaded into the synthesis tools for the power extraction. The power estimation methodology employs the Genus synthesis tool in PLE mode to generate the Verilog gate-level network list and the SDF Format. To perform the power dissipation results with real-world input stimuli, we stimulated the post-synthesis netlists using a discretized audio signal containing 100,000 samples.

B. Synthesis Results

Table V shows that the Haar-II architecture presents the best results in terms of total area, for all SCM combinations. It occurs because the Haar-II architecture gives the fewest number of arithmetic operators (28) among all the arrangements. However, the architecture with the best results in terms of power dissipation is the Haar-VI. This lower power dissipation is associated with the lowest fanout values presented by this architecture, as shown in Table V. Notably, this lower fanout in the Haar-VI is due to the large amount of five $M=1$ blocks used in this architecture, which is favorable for its optimization in the synthesis tool.

Fig. 6: Synthesis methodology diagram.

It is also noticeable the advantages of the Haar-VI proposed in this work regarding energy per operation. The combination of the Haar-VI with six SCM strategies (from SCM-II to SCM-VII) presents the best EPO results among all the architectures. However, when using SCM-I, the Haar-IV shows the best EPO result. It occurs because although both Haar-IV and Haar-VI present the same fanout value (303), the synthesis tool found an advantage in optimizing the architecture with the less critical path (Haar-IV).

The results in Table V indicate that using our SCM-VI solution is favorable for almost all the Haar architectures, with the best circuit area, total power dissipation, and EPO results. It occurs because this architecture presents only two arithmetic operators, i.e., one adder and one subtractor. The SCM-VI does not offer gains only when used in Haar-III and Haar-IV architectures, where the SCM-I gives the best circuit area, total power dissipation, and EPO results. However, observe that, in terms of the Haar-III, the SCM-VI solution provides almost the same total power dissipation and EPO, with less circuit area than using the SCM-I solution.

Although the SCM-VI and SCM-VII architectures present the same amount of two arithmetic operators and the same critical path, the SCM-VII involves two subtractions that impose slight more logic operations than the additions. It explains the SCM-VII presents almost the same results but with fewer gains than the SCM-VI approach for nearly all

Table V.: Synthesis results for the Haar hardware architecture investigation: Power dissipation (μW), Energy per operation (fJ/op), Circuit Area and Gate Count. Power @ 1.62GHz.

DWT		Power dissipation (μW)			Gates	Cell Area	EPO	fanout
Haar $m = 9$	SCM	Leakage	Dynamic	Total	(k gates)	(μm^2)	(fJ/op)	(number of gates)
Haar - I	SCM - I	21.65	75.31	96.96	3698	22978.80	59.73	330
	SCM - II	21.42	81.60	103.02	3438	22605.96	63.46	331
	SCM - III	22.91	85.82	108.73	4002	23452.52	66.98	333
	SCM - IV	23.43	85.23	108.66	4155	23755.16	66.93	333
	SCM - V	24.30	88.41	112.71	4561	24284.52	69.43	402
	SCM - VI	16.99	56.28	73.27	2793	15753.92	45.13	305
	SCM - VII	20.67	74.69	95.36	3588	19997.12	58.74	330
Haar - II	SCM - I	14.47	69.75	84.22	2312	15004.60	51.88	312
	SCM - II	14.55	72.76	87.31	2296	15035.80	53.78	313
	SCM - III	15.07	73.59	88.66	2476	15306.72	54.61	314
	SCM - IV	15.23	73.33	88.56	2530	15408.12	54.55	314
	SCM - V	15.48	74.22	89.70	2661	15571.92	55.26	314
	SCM - VI	13.10	67.85	80.95	2083	12807.08	49.87	306
	SCM - VII	14.34	71.44	85.78	2342	14192.36	52.84	313
Haar - III	SCM - I	25.21	92.22	117.43	3761	25025.52	72.34	401
	SCM - II	25.25	107.64	132.89	3666	24847.16	81.86	429
	SCM - III	26.07	108.76	134.83	3969	25301.12	83.06	430
	SCM - IV	26.32	111.26	137.58	4046	25465.44	84.75	432
	SCM - V	26.82	110.76	137.58	4262	25757.16	84.75	432
	SCM - VI	22.52	95.41	117.93	3296	20950.28	72.64	401
	SCM - VII	24.87	104.25	129.12	3744	23469.68	79.54	421
Haar - IV	SCM - I	20.19	56.70	76.89	2963	19470.36	47.36	303
	SCM - II	20.30	72.56	92.86	2933	19416.28	57.20	328
	SCM - III	20.86	73.55	94.41	3133	19716.32	58.16	329
	SCM - IV	21.04	73.53	94.57	3186	19826.04	58.26	329
	SCM - VI	21.34	73.85	95.19	3325	20008.04	58.64	329
	SCM - VI	18.80	68.14	86.94	2708	17066.92	53.56	315
	SCM - VII	20.08	71.28	91.36	2986	18509.92	56.28	329
Haar - V	SCM - I	23.01	83.36	106.37	3491	22979.32	65.52	332
	SCM - II	23.21	88.27	111.48	3402	22834.24	68.67	398
	SCM - III	24.03	89.63	113.66	3697	23277.28	70.01	399
	SCM - IV	24.29	90.89	115.18	3775	23434.84	70.95	400
	SCM - V	24.74	90.79	115.53	3987	23705.24	71.17	400
	SCM - VI	20.72	78.55	99.27	3054	19127.16	61.15	335
	SCM - VII	22.86	85.62	108.48	3479	21481.72	66.82	334
Haar - VI	SCM - I	19.43	58.56	77.99	3127	19714.24	48.04	303
	SCM - II	19.50	57.71	77.21	3001	19625.84	47.56	303
	SCM - III	20.46	59.99	80.45	3355	20156.24	49.56	306
	SCM - IV	20.80	59.98	80.78	3458	20358.00	49.76	306
	SCM - V	21.31	60.60	81.91	3717	20692.36	50.46	306
	SCM - VI	16.67	53.62	70.29	2578	15208.96	43.30	302
	SCM - VII	19.02	52.99	72.01	3090	17955.60	44.36	304

Total is the Total power dissipation in (μW), Area is the Circuit area in (μm^2), EPO is the Energy per operation (fJ/op).

○ Red-colored highlighted cells represents the worst results. ○ Green-colored highlighted cells represents the best results.

the Haar architectures. However, it is possible to claim that both proposed SCM-VI and SCM-VII strategies are favorable for use in the Haar architectures. It proves the efficiency of implementing the H coefficient by using a new $45X * 2^{-6}$ form.

From the results, we can identify the Haar-VI and SCM-VI with the best combination for designing an energy-efficient Haar with nine resolution levels. It shows the importance of using lower resolution $M=1$ and $M=2$ levels for implementing Haar-9. This result improves the literature, whose Haar-III proposed in [29] (with only $M=3$ blocks) presents the worst results among the Haar architectures.

While the solution of [29] operates at the maximum frequency of 300 MHz, Our solutions provide the maximum of 1.62 GHz at the same conditions of [29], i.e., considering as input the same audio signal with 100,000 samples. Therefore, the time processing of [29] is 333.33s while our solutions enable a processing time of 61.72s, which proves the efficiency of our proposed solutions. Although we are exploring different solutions for the SCM at the maximum frequency operation, we can adjust the frequency operation of our solutions accordingly depending on the target application. It is noticeable the impact on power reduction of our proposed solutions. While the best architecture of [29] offers 248.2 μ W of total power dissipation, our best Haar-VI (SCM-VI) solution provides a significant power reduction with only 70.29 μ W of power dissipation. It proves the efficiency of the proposed strategies used in this work to optimize the Haar-9 architecture.

V. CONCLUSIONS

This work presented an architectural exploration for Haar Transform, combining multi-level resolutions and SCM strategies. We explored six Haar architectures with decomposition level 9. The different schemes used blocks by Haar transform with lower resolution $M=1$, $M=2$, and $M=3$ levels for composing the other architectures. We also explored various forms of implementing the H coefficient by using the SCM approach. The synthesis results consolidated the Haar-II with the lower cell area. This architecture comprises $M=1$ and $M=2$ blocks with fewer amount of arithmetic operations. However, the best combination for the Haar-9 transform design, regarding power dissipation and energy per operation, comprises the Haar-VI architecture (with two $M=2$ and five $M=1$ blocks) and the SCM-VI approach (with only one addition and one subtraction and a critical path equal to 2). This combination offers the lowest fanout among the architectures investigated.

VI. ACKNOWLEDGEMENTS

The authors would like to thank CNPq and Fapergs Brazilian agencies for financial support to our re-search.

REFERENCES

- [1] M. Medhat, "A Review on Applications of the Wavelet Transform Technique in Spectral Analysis," *Journal of Applied & Computational Mathematics*, vol. 4, no. 4, pp. 1–6, 2015.
- [2] R. Boujelbene, Y. Jemaa, and M. Zribi, "A comparative study of recent improvements in wavelet-based image coding schemes," *Multimedia Tools and Applications*, vol. 78, pp. 1649–1683, 2018.
- [3] N. Nathaniel, E. Ashigwuike, A. Sadiq, and N. Obadiah, "Modeling, Simulation and Analysis of Automotive Radar Signal Using Wavelet Transform Technique," in *15th International Conference on Electronics, Computer and Computation (ICECCO)*, Dec 2019, pp. 1–6.
- [4] J. Wagh, S. Shinde, and R. Mudholkar, "Applications of wavelet transform and its advantages compared to fourier transform in Biomedical signal processing MATLAB domain," in *IEEE International Conference on Industrial Applications of Signal processing (ICIASP)*, Oct 2019, pp. 22–25.
- [5] B. Adhikari, D. S. M. Karki, R. Mishra, R. Dahal, S. Sasmal, and V. Klausne, "Application of wavelet for seismic wave analysis in Kathmandu Valley after the 2015 Gorkha earthquake, Nepal," *Geoenvironmental Disasters*, vol. 7, no. 2, 2020.
- [6] Y. Kankanamge, Y. Hu, and X. Shao, "Application of wavelet transform in structural health monitoring," *Earthquake Engineering and Engineering Vibration*, vol. 19, pp. 515–532, 2020.
- [7] M. Misiti, Y. Misiti, G. Oppenheim, and J.-M. Poggi, "Wavelet toolbox," *The MathWorks Inc., Natick, MA*, vol. 15, p. 21, 1996.
- [8] J. Walker, *A primer on wavelets and their scientific applications*. CRC press, 2008.
- [9] K. Ho and S. Blunt, "Rapid identification of a sparse impulse response using an adaptive algorithm in the Haar domain," *Transactions on Signal Processing*, vol. 51, no. 3, pp. 628–638, Mar 2003.
- [10] Ho, KC and Blunt, Shannon D, "Rapid identification of a sparse impulse response using an adaptive algorithm in the Haar domain," *IEEE transactions on signal processing*, vol. 51, no. 3, pp. 628–638, 2003.
- [11] Aminlou, Alireza and Refan, Fatemeh and Hashemi, Mahmoud Reza and Fatemi, Omid, "Two Level Cost-Quality Optimization of 9-7 Lifting-Based Discrete Wavelet Transform," in *2007 IEEE International Conference on Image Processing*, vol. 6, 2007, pp. VI – 217–VI – 220.
- [12] F. Franchetti, T. M. Low, D. T. Popovici, R. M. Veras, D. G. Spampinato, J. R. Johnson, M. Püschel, J. C. Hoe, and J. M. F. Moura, "SPIRAL: Extreme Performance Portability," *Proceedings of the IEEE*, vol. 106, no. 11, pp. 1935–1968, 2018.
- [13] J. Olkkonen, *Discrete Wavelet Transforms Theory and Applications*. IntechOpen, 2011.
- [14] D. Sundararajan, *Discrete Wavelet Transform: A Signal Processing Approach*. Wiley, 2015.
- [15] I. Daubechies, *Ten lectures on wavelets*. SIAM, 1992.
- [16] S. Talukder, R. Singh, S. Bora, and R. Paily, "An Efficient Architecture for QRS Detection in FPGA Using Integer Haar Wavelet Transform," *Circuits, Systems, and Signal Processing*, pp. 1–16, 2020.
- [17] M. Ercegovic and T. Lang, *Digital Arithmetic*. Morgan Kaufmann, 2003.
- [18] O. Kovalev and I. Yanchenko, "Hardware Solution for Haar Wavelet Transform in Real Time," in *2nd International Conference on Industrial Engineering, Applications and Manufacturing*, May 2016, pp. 1–4.
- [19] E. C. Kim, E. Meloni, Y. Iano, and L. Bravo-Roger, "FPGA implementation of a de-noising using Haar level 5 wavelet transform," in *IEEE 13th International Symp. on Consumer Electronics*, Sep 2017, pp. 1–4.
- [20] P. Li and et al., "A low-complexity ECG processing algorithm based on the Haar wavelet transform for portable health-care devices," *Science China Information Sciences*, vol. 57, no. 14, pp. 1–14, 2014.

- [21] E. Mazomenos and et al., "A low-complexity ECG feature extraction algorithm for mobile healthcare applications," *IEEE journal of biomedical and health informatics*, vol. 17, no. 2, pp. 459–469, 2013.
- [22] T. Silveira, A. Kozakevicius, and C. Rodrigues, "Automated drowsiness detection through wavelet packet analysis of a single EEG channel," *Expert Systems with Applications*, vol. 55, pp. 559–565, 2016.
- [23] A. Chefi, A. Soudani, and G. Sicard, "Hardware compression solution based on HWT for low power image transmission in WSN," in *ICM 2011 Proceeding*. IEEE, 2011, pp. 1–5.
- [24] F. Diaz, A. Burón, and J. Solana, "Haar wavelet based processor scheme for image coding with low circuit complexity," *Computers & Electrical Engineering*, vol. 33, no. 2, pp. 109–126, 2007.
- [25] P. Chaniyara, K. Srivastava, B. Suresha, and S. Reddy, "Design of sampled analog wavelet processor architecture for cochlear implant application," *Analog Integrated Circuits and Signal Processing*, vol. 86, no. 2, pp. 171–180, 2016.
- [26] F. Faek and J. Hamadamin, "Fingerprint Recognition using Wavelet Transform and k-NN Classifier," *Journal of Polytechnic*, pp. 1–8, 2016.
- [27] T. Sun, H. Zhang, and C. Hu, "Identification of gas-liquid two-phase flow regime and quality," in *IMTC/2002. Proceedings of the 19th IEEE Instrumentation and Measurement Technology Conference (IEEE Cat. No. 00CH37276)*, vol. 2. IEEE, 2002, pp. 1471–1474.
- [28] J. Altermann, E. Costa, and S. Almeida, "High performance Haar Wavelet transform architecture," in *2011 20th European Conference on Circuit Theory and Design (ECCTD)*. IEEE, 2011, pp. 596–599.
- [29] H. Seidel, M. Macedo, G. Paim, E. Costa, S. Almeida, and S. Bampi, "Energy-Efficient Haar Transform Architectures Using Efficient Addition Schemes," in *2020 IEEE Latin American Symposium on Circuits and Systems (LASCAS)*. IEEE, 2020, pp. 1–4.
- [30] Y. Voronenko and M. Püschel, "Multiplierless Multiple Constant Multiplication," *ACM Transactions on Algorithms*, vol. 3, no. 2, 2007.
- [31] D. Bull and D. Horrocks, "Primitive Operator Digital Filters," *IEE Proceedings G*, vol. 138, no. 3, pp. 401–412, 1991.