Designing Mixed-Signal Programmable Fuzzy Logic Controllers as Embedded Subsystems in Standard CMOS Technologies

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***Abstract*—A digitally programmable analog Fuzzy Logic Controller (FLC) is presented. Input and output signals are processed in the analog domain whereas the parameters of the controller are stored in a built-in digital memory. Some new functional blocks have been designed whereas others were improved towards the optimization of the power consumption, the speed and the modularity while keeping a reasonable accuracy, as it is needed in several analogue signal processing applications. A nine-rules, two-inputs and one-output prototype was fabricated and successfully tested using a standard CMOS 2.4μ technology, showing good agreement with the expected performances, namely: a 2.7% RMSE, from 2.22 to 5.26 Mflips (Mega fuzzy logic inferences per second) at the pin terminals (@*CL*=13pF), 933 μW power consumption per rule (@*Vdd*=5V) and 5 bits of resolution. Since the circuit is intended for a subsystem embedded in an application chip (@*CL* ≤ 5pF) up to 8 Mflips may be expected.**

***Index Terms*—Mixed Signal, Fuzzy Logic, Analog CMOS, Controller.**

I. INTRODUCTION

In the last years, the application of Fuzzy Logic has been extended beyond the classical Process Control area where it has been employed from the beginning. Signal Processing, Image Processing, Power Electronics, seem to be others niches where this soft-computing technique can meet a broad range of applications. As real-time processing mode need ever faster, more autonomous and less power-consuming circuits the choice of on-chip controllers becomes an interesting option. Digital Fuzzy Logic chips provide enough performance for general applications but their speed is limited, if compared with their analog counterparts. Furthermore, in real-time applications digital fuzzy processors needs A/D and D/A converters to interface sensors and actuators, respectively. On the other hand, pure analog processors suffer from the lack of suppleness since full analog programmability is only feasible in special technologies allowing analog storage devices (i.e.: floating gate transistors). However, in the frame of standard CMOS technologies, a trade-off between accuracy and flexibility is achieved when a finite discrete set of analogue parameters is provided. For instance, a voltage parameter can be settled by using a binary-scaled set of currents sources yielding a discrete set of voltage drops across a linear resistor. In such a case, it is possible to use a digital memory to store a given binary combination of the set of currents. This technique gives rise to the so-called Mixed-Signal computation circuits [2].

It has been shown that analogue current-mode FLCs [2] lend themselves to simple rules-evaluation and aggregation circuits that can work at a reasonable speed. If some of the unwanted current-to-voltage and/or voltage-to-current intermediate converters can be avoided, the delay through cascaded operators may be even shortened and higher speeds achieved. This is interesting when fuzzifiers [2][3] and defuzzifiers [4] circuits are being designed for these circuits interact normally with a voltage-mode controlled environment. On the other hand, to reduce die silicon area and power consumption some building blocks can be shared without altering functionality. As a result, a relatively low-complexity layout can be obtained which leads to an additional gain of speed.

In this work, a low-power digitally programmable analogue Fuzzy Logic Controller (Mixed-Signal FLC) is introduced. It aims to be embedded as a subsystem as required for several analog signal-processing applications of medium-accuracy (i.e.: non-linear filtering [1], power electronics [9], etc). Keeping in mind the above exposed issues, new operators were designed while others were optimized achieving a flexible and high performance controller notwithstanding the limits imposed by the technology that was used for the demonstrator.

II. ARCHITECTURE OF THE CONTROLLER

A Fuzzy inference arrangement intends to reproduce algorithmically the structured human knowledge by encoding it into a set of rules, which are normally expressed in the form: *"if* <antecedent> *then* <consequent>*"*. In a Fuzzy Controller, a relationship between its inputs and outputs is established after executing concurrently all rules by following three basic fuzzy operations: Fuzzification, Rules-Evaluation (Inference) and Defuzzification. Zero-Order Sugeno architecture offers a good trade-off between simplicity and accuracy given that the consequent part of any rule is just a singleton (i.e.: a constant value). Fig. 1 shows the block diagram of a 2-input 1-output controller, highlighting the above mentioned fuzzy operations. For the general case of an *m*-rule controller, a set of Complementary Fuzzy Membership Functions (CFMF) per input, being shared by several rules, take care for the Fuzzification. Since we work with complementary membership functions, the frequently used MIN inference method (T-Norm) for the Rules-Evaluation should be reformulated as:

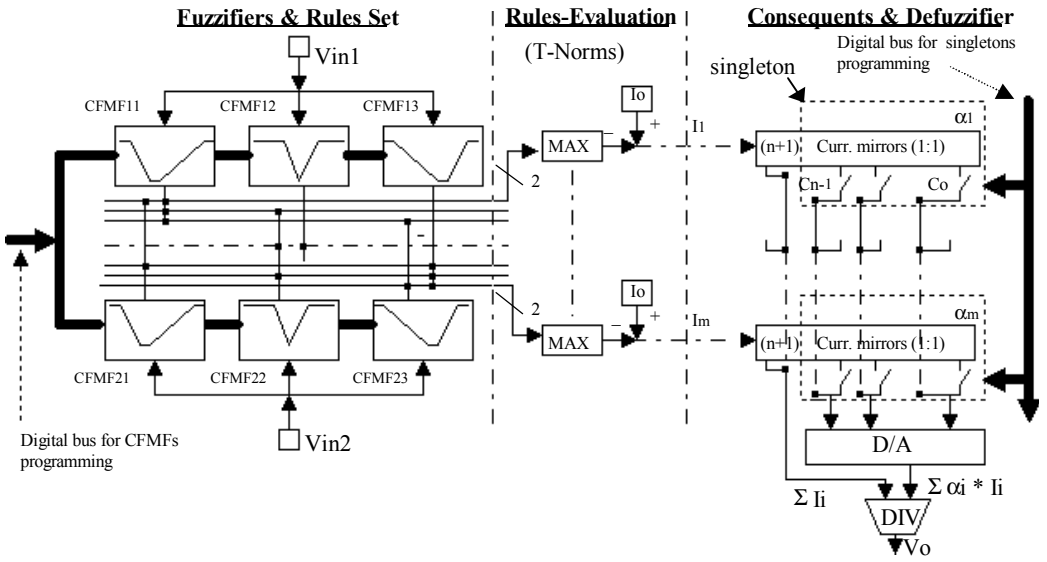


Fig.1. Block diagram of the Zero-Order Takagi-Sugeno Fuzzy Logic Controller.

MIN (A, B,...) = 1 − MAX (1−A, 1−B,…). This is performed by means of the 2-input MAX operators, whose outputs are complemented to *Io* (*Io* ≡ logical '1'). Subsequently, the 'firing degree' of each rule is provided in the form of a current signal *Ii*, as shown in Fig. 1.

At the Defuzzification stage, each current *Ii* is replicated (*n+1*) times via unit gain mirrors, where *n* stands for the resolution of a rule consequent singleton αi. The latter is discretely codified accordingly with the state of the switches *Cn-1...C0*. The *n* outputs of the singletons are column-wise summed following a 'common weighting' strategy that will be explained later.

Finally a common current-mode Digital to Analogue converter (D/A), used as a weighting operator, together with an analog divider takes care of the computation of the Averaged-Weighted Sum (AWS), rendering the defuzzified output value *Vo* equal to:

$$Vo = k \frac{\sum_{i=1}^{m} \alpha i * Ii}{\sum_{i=1}^{m} Ii}, \quad (1)$$

where *k* is a voltage-dimension constant value defined by the transfer function of the divider itself.

A. Complementary Fuzzy Membership Functions

Low-power fuzzy controllers need relatively low transconductance values for their membership function circuits. Consequently, CMOS triode transconductors can be used to meet that requirement smartly. The circuit of the complementary fuzzifier is depicted in Fig. 2 a). It is composed by two almost linear regulated-cascode transconductors (*ML1, ML3, DAL - MR1, MR3, DAR*) each one controlling one edge of the CFMF, whose shape is nearly an inverted trapezoid. Transistors *ML2, MR2* have fixed large sizes, so that their gate-voltage-overdrive (*Vgs-VTn*) can be neglected. Reference voltages *VKL*, *VKR* define the knees where conduction begins falling towards zero or rising towards *Io* respectively in each transconductor. Slopes and knees are independently programmable.

The drain-to-source voltage drops *Vds* of transistors *ML1*, *MR1* are kept constant over a wide range of the input voltage *Vin*, and their magnitudes are fixed by means of the artificially increased offset voltages of the differential amplifiers *DAL*, *DAR*. Since these offsets are smaller than the saturation drain-source voltage Vds_{sat} of transistors *ML1*, *MR1*, the last are constrained to operate in the triode region. Thus, their transconductance *gm*, defining the slopes of the trapezoid, is given by:

$$gm = \frac{\partial Id}{\partial Vgs} = \mu Cox \frac{W}{L} Vds. \quad (2)$$

In Fig. 2 b), the schematic of the differential amplifiers is shown. By sizing $(W/L)_{M1} > (W/L)_{M2}$ an artificial voltage offset between their inputs (*V- − V+ = Vds*) is established and it is linearly controlled by the voltage source *Vs* as follows:

$$Vds = \left(\sqrt{\frac{(W/L)_{M5}}{2\,(W/L)_{M2}}} - \sqrt{\frac{(W/L)_{M5}}{2\,(W/L)_{M1}}} \right) \left(Vdd - |VTp| - Vs \right). \quad (3)$$

In this way, slopes can be electrically tuned, which is an advantage when analogue storage is available compared to the typical four transistors CFMF operators as in [2][3]. In the latter, input transistors are saturated and the tail current *Io* must be fixed (*Io* ≡ logical '1'). Even if in both cases slopes are discretely programmed via a set of different sized input transistors, the ratio between the maximum and minimum transistor size needed in our case, from (2), becomes *N*, where *N* is the ratio between the maximum and minimum desirable slopes. For the second case, the latter ratio is equal to N^2. Thus, for a given range of slopes, the whole set of saturated input transistors would demand an increased amount of silicon surface. Moreover, in this ver-

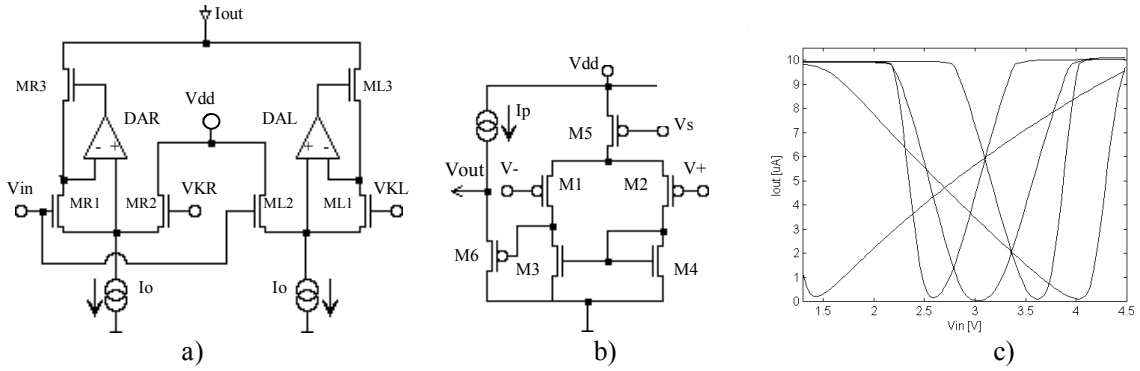


Fig.2. a) Complementary Fuzzy Membership Function (CFMF) Circuit. b) Differential Amplifiers *DAL DAR*. c) Some measured transfer functions *'Iout vs. Vin'* of the CFMF using a HP4145B instrument.

sion of the controller, we have performed a combination between a few discrete values of *Vs* and input transistor sizes in order to optimize the slopes range capability at a low cost in terms of silicon area. Finally, a piece-wise expression for the output current *Iout* of the CFMF is roughly given by (4), where gm_{L1} and gm_{R1} result from combining expression (2) and (3) for each transconductor of the CFMF. In the actual implementation each knee voltage *VKR* and *VKL* is obtained by means of a set of binary scaled currents yielding 32 equally spaced voltages drops through a MOST-only grounded linear resistor. Fig. 2 c) shows some measured curves. Note that we could easily get $N \approx 9.5$ whereas the input range of *Vin* reaches to 3V.

$$Iout \approx \begin{cases} Io; & if\ Vin < VKL - \dfrac{Io}{gm_{L1}}, \\ \left(gm_{L1}(VKL - Vin)\right); & if\ VKL - \dfrac{Io}{gm_{L1}} < Vin < VKL, \\ 0; & if\ VKL < Vin < VKR, \\ \left(gm_{R1}(Vin - VKR)\right); & if\ VKR < Vin < VKR + \dfrac{Io}{gm_{R1}}, \\ Io; & if\ VKR + \dfrac{Io}{gm_{R1}} < Vin. \end{cases} \quad (4)$$

B. Multiple-input MAX operator (T-Norm)

The Winner-Take-All circuit presented in [5] has been adopted for the MAX operator, but some modifications are introduced. The circuit depicted in Fig. 3 a) is composed by *q* current - controlled voltage sources (*M1, M2, M3, M4* and *M5*) connected to a common node *Vc* and fighting to impose their own voltage, which is proportional to their controlling current source (*I1…Iq*). Gate voltages of transistors *M1* belonging to the losers fall and those transistors switch off. Transistors *Mc1*, *Mc2*, connected as a cascoded-diode and common to all cells, convey the highest current at the output. Since transistors *M4*, *M5* are cascoded an accurate replica of the winner current is ensured. Diode-connected transistors *M2*, *M3* guarantee a voltage level of at least $2VTn$ at the gate of loser transistors *M1*. In this way, the recovering time delay of these cells (i.e. when any of them pass from loser to winner) is improved.

C. Consequents Singletons and Defuzzifier

Singletons: for the consequent of each rule a discrete singleton αi smaller than 1 is given by:

$$\alpha i = (Cn\text{-}1)_i\ 2^{-1} + (Cn\text{-}2)_i\ 2^{-2} + \ldots\ldots + (C0)_i\ 2^{-n}, \quad (5)$$

where *i* ranges from 1 to *m* and coefficients $(Cn\text{-}1)_i \ldots\ldots (C0)_i$ adopt binary values. In Fig. 1, the outputs of the $(n+1)$ current mirrors of the whole *m*-consequent set are column-wise summed to give the following $(n+1)$ values:

$$(\Sigma\, Ii);\quad (\Sigma\, (Cn\text{-}1)_i\ Ii);\ldots\ldots;\ (\Sigma\, (C0)_i\ Ii). \quad (6)$$

Except for the first term above, which becomes the denominator current at the divider (i.e.: *ID*), all the others are weighted and summed in the common D/A, whose circuit is shown in Fig. 3 b). It comprises a set of *n* independent binary scaled current mirrors that sum their outputs at a common node yielding the numerator current at the divider (i.e.: *IN*). Thus, the output current $Iout_{D/A} = IN$ from the D/A circuit is equal to:

$$(\Sigma\, (Cn\text{-}1)_i\ 2^{-1}\ Ii) + \ldots\ldots + (\Sigma\, (C0)_i\ 2^{-n}\ Ii) = \Sigma\, \alpha i * Ii. \quad (7)$$

With the common D/A used here, an important saving of silicon area is obtained compared to the local D/A approach [2][6]. Moreover, the input capacitance of each consequent is reduced by a factor $(2^n/n+1)$. Additionally, since the layout of the whole defuzzifier becomes smaller, routing capacitances are also diminished. As a result, a considerable

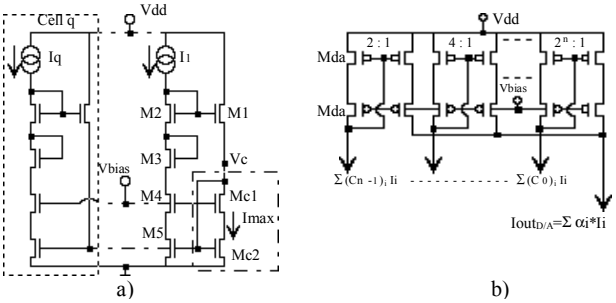


Fig.3. a) Multiple-Input MAXIMUM circuit, b) Weighting D/A circuit.

gain of speed can be achieved.

Former idea on common weighting can be found in [11]. In the latter, weighting is achieved in a pseudo-normalizer by exploiting a current division technique by means of encoding splitters (one per singleton) and a R/2R network. However, for discrete-programming singletons, splitters need two switch transistors per bit and the availability of both complementary digital programming signals (i.e. *Ci* and */Ci*) applied at the gate of the switch transistors. Thus, splitters demand more silicon area and routing space for the digital programming signals. Moreover, as a consequence of the current splitting, the defuzzified output value results *n* times more attenuated than in this case. Consequently, for a given dynamic range, the signal-to-noise figure needed at the R/2R network results more compromised.

Analog Divider: a novel current-input voltage-output divider [4] was specially designed to carry out the division operation in formula (1). The circuit is shown in Fig. 4 a). With equally sized transistors in each row of the circuit, the division is actually performed by transistors *M1*, *M2*, *M3* at the bottom layer, all of them being constrained to operate in the triode region. The drain-to-source voltage drops *Vds* of those transistors are matched thanks to common-gate connected transistors *M4*, *M5*, *M6* that convey the same current. This is guaranteed by the upper PMOS cascoded-mirrors (*M7* to *M12*). While *Vb1* and *Vbo* are fixed bias voltages, transistor *M3* gate voltage (*Vout*) is self-adjusted so that the drain current of *M6* matches the current imposed by the PMOS cascoded-mirror branch *M9*, *M12*. In this way, the following relation holds [4]:

$$(Vout - Vbo) = Vo = (Vb1 - Vbo)\frac{IN}{ID}. \qquad (8)$$

Thus, if *Vout* is referred to *Vbo* a two-quadrant divider is obtained. Since this divider behaves as a transresistor, there is no need for extra interface converter circuits neither at the inputs [6] nor at the output [7][8]. Fig. 4 b) displays some measured characteristics using a HP4145B equipment. Fig. 4 c) ilustrates the measured relative error (i.e.: $\Delta Vout/Vout$). The output offset (i.e.: for *IN*=0) is lower than 1.6mV.

III. ANALYSIS OF THE ACCURACY OF THE CONTROLLER

A comprehensive analysis of the systematic and mismatch errors for each block described above can be found in [12]. On one hand, systematic errors can be minimized by following proper design strategies. On the other hand, since they are to some extend deterministic, they can be incorporated to the ideal input-output relationships of each block. This gives rise to a more accurate model that can be directly used to fit a desired target function at the system-level design step. For those reasons systematic errors will not be considered for this analysis. In contrast, mismatch errors due to technological parameters fluctuations can only be statistically estimated [13]. Therefore, an investigation about the spreading of the controller's dc behavior becomes mandatory. For this purpose, a methodical approach based on the propagation of the random errors through the different fuzzy operators along the signal path is discussed hereafter [2][12]. This allows to quantify the incidence of the non-idealities presented by each building block on the accuracy of the controller.

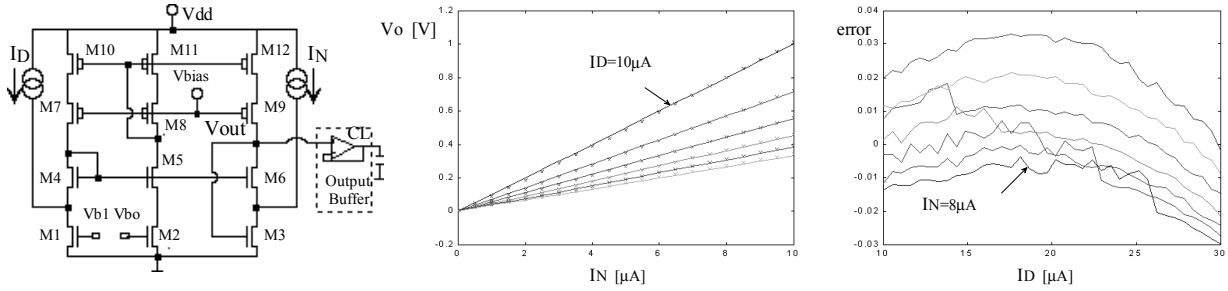
Fig. 5 shows a block diagram of the controller involving the basic operators taking part in a rule. In a first simulation, we will consider only one fired rule at the controller. Some assumptions are to be made however:

-The singleton of the consequent of the rule under consideration is set to its maximum value (i.e.: αi=1). It has been proven [12] that this situation corresponds to the maximum standard deviation at the output of the grouped blocks 'consequent singleton+D/A' shown in Fig. 5.

-Since the T-Norm plays the role of a switch selecting the minimum value among those provided by the set of membership functions in a rule, we will consider this operator as the identity function (i.e.: *f1*). Therefore, the T-Norm outputs the minimum value (i.e.: after being complemented by *Io*) delivered by only one CFMF.

-In order to evaluate the variance of the output of each circuit we considered only the mismatch due to the spreading of the two most relevant technological parameters of their transistors, namely: the threshold voltages *VT* and the current gains $\beta=\mu\, Cox\, W/L$. As in [13], we assume that the *VT* and β of all transistors are statistically independent random variables, whose variances follow the 'inverse of the transistor area' law (i.e.: $\sigma^2_{\Delta VT} = A^2_{VT}(WL)^{-1}$ and $\sigma^2_{\Delta\beta} = A^2_{\beta}\,\beta^2(WL)^{-1}$).

-Let us call the variances (i.e.: due to mismatch) of the



a) b) c)

Fig.4. a) Transresistive divider circuit. b) Measured (x) and calculated (-) Vo for 0<*IN*<10μA while *ID* ranges from 10 μA to 30 μA by 4μA steps. c) Measured relative error of the divider.

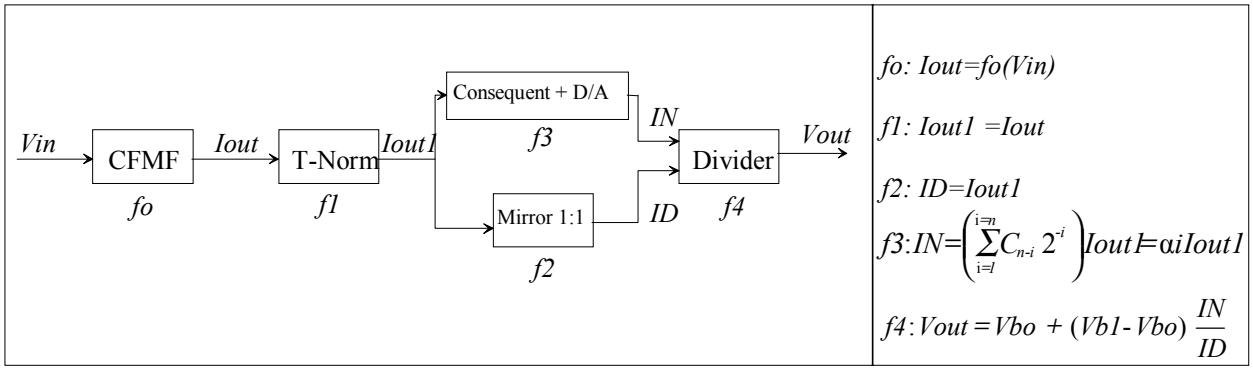


Fig.5. Simplified block diagram of the controller with only one fired rule for the estimation of the variance of its output *Vout*.

output signal of each operator in Fig. 5 as: σ^2_{div}; $\sigma^2_{cons+D/A}$; σ^2_{mirror}; σ^2_{Io} and σ^2_{CFMF}. Full expressions for the latter variances as a function of the transistors geometry, their biasing conditions and the technological parameters can be found in [12].

Bearing in mind the above considerations, we can start at the end of the signal path by writing the variance of the output signal *Vout* as:

$$\sigma^2_{Vout}=\sigma^2_{div}+\left(\frac{\partial f4}{\partial ID}\right)^2\sigma^2_{ID}+\left(\frac{\partial f4}{\partial IN}\right)^2\sigma^2_{IN}+2\left(\frac{\partial f4}{\partial ID}\right)\left(\frac{\partial f4}{\partial IN}\right)\sigma^2_{ID,IN}. \quad (9)$$

In the above equation, the second and third terms correspond to the mismatch errors carried by signals *ID* and *IN* and propagated through the divider. The last fourth term accounts for the cross-correlation between *IN* and *ID*, considering they are yielded from a common node at the output of the T-Norm (*Iout1*). Therefore, we can write:

$$\sigma^2_{IN}=\sigma^2_{cons+D/A}+\left(\frac{\partial f3}{\partial Iout1}\right)^2\sigma^2_{Iout1}, \quad (10)$$

$$\sigma^2_{ID}=\sigma^2_{mirror}+\left(\frac{\partial f2}{\partial Iout1}\right)^2\sigma^2_{Iout1}, \quad (11)$$

$$\sigma^2_{IN,ID}=\left(\frac{\partial f2}{\partial Iout1}\right)\left(\frac{\partial f3}{\partial Iout1}\right)\sigma^2_{Iout1}. \quad (12)$$

Finally, the variance of the signal *Iout1* can be calculated as the sum of the variance introduced by the T-Norm plus the one related to the membership function CFMF. The latter is propagated through the T-Norm operator. Hence:

$$\sigma^2_{Iout1}=\sigma^2_{T\text{-}Norm}+\sigma^2_{Io}+\left(\frac{\partial f1}{\partial Iout}\right)^2\sigma^2_{CFMF}, \quad (13)$$

where σ^2_{Io} is the variance of the current *Io* complementing the output of the MAXIMUM circuit (see Fig. 1), which is supplied by a mirror. From (9) to (13) we can derive a clear-cut relationship that illustrates clearly the contribution of the individual mismatch errors from each operator on the variance of the controller's output. Thus, we have:

$$\sigma^2_{Vout}=\sigma^2_{div}+a_{cons+D/A}\sigma^2_{cons+D/A}+a_{mirror}\sigma^2_{mirror}\cdots \\ \cdots+a_{T\text{-}Norm}\sigma^2_{T\text{-}Norm}+a_{Io}\sigma^2_{Io}+a_{CFMF}\sigma^2_{CFMF}, \quad (14)$$

where the analytical expressions for the '*a*' coefficients are given in Table I.

Fig. 6 a) illustrates the standard deviation of the output *Vout* as a function of the firing degree of the only rule considered. In this simulation the slopes of the membership functions CFMF were set to the minimum. Note that σ_{Vout} decreases from 80mV to 20mV as the rule is being increasingly activated. However, in any Fuzzy Controller, when only one rule is fired, its firing degree turns to be high (near 1). Therefore, to be more realistic, one should consider that σ_{Vout} in this particular simulation ranges from 20mV to 30mV. Accordingly, the attainable accuracy should range from 2% to 3% for an output voltage swing of 1V.

From Fig. 6 b) one can notice that the most important contribution to the total variance of the controller output is due to the divider, followed by the consequents+D/A and the mirror before the denominator current *ID*. In contrast, the mismatch errors of the CFMF and the T-Norm circuits are not propagated towards the output when only one rule is fired. This is due to the normalization performed by the divider that attenuates any deviation simultaneously present at both divider inputs.

Considering that the former simulation did not allow us to find out how the errors generated by the antecedent part of the rules are propagated, we carried out a second simulation assuming that two rules operate in a complementary way. This is to say: the more one of the rules is fired, the more is the other set off. This condition is frequently met in controllers whose neighboring membership functions overlap considerably. However, in order to facilitate the analysis, the mirror before the denominator *ID* and the Consequents+D/A circuits are now supposed to be error-free blocks. Consequently, the block diagram in Fig. 5 is slightly modified by adding a second membership function CFMF cascaded with another T-Norm. The output of this T-Norm is summed with the signal coming from the other rule block (i.e.: CFMF + T-Norm + *Io*) at the common node

yielding the signal *Iout1*.

The circuits used as well as their settings are the same as the ones used in the previous simulation. In this case however, while the consequent singleton was fixed to 0.9 in one rule (i.e.: $\alpha 2$), it was allowed to range parametrically from 0.1 to 0.9 (i.e.: $\alpha 1$) in the other. Simulation results are shown in Fig. 7 a) and Fig. 7 b). The main conclusions are summarized in the following:

-As the difference between the singletons values of both rules becomes large (i.e.: $\alpha 1$=0.1 and $\alpha 2$=0.9), the mismatch errors of the antecedents part of the rules (CFMF + T-Norm +*Io*) are more propagated to the output. This can be seen in Fig. 7 b). In contrast, the errors due to the antecedent part of the rules are not propagated when both singletons adopt the same values (i.e.: $\alpha 1$=$\alpha 2$=0.9). When this happens, *IN* and *ID* at the divider remain constant and the normalization attenuates the deviations coming from the previous stages.

-Note in Fig. 7 a) that σ_{Vout} ranges from 15mV (1.5%) to 25mV (2.5%). Nevertheless, these error figures should be incremented by 1% (at least) when the mismatch errors introduced by the consequents+D/A and the mirror before the denominator *ID* (neglected for this second simulation) are also considered.

TABLE I
ANALYTICAL EXPRESSIONS OF THE '*a*' COEFFICIENTS IN (14).

a	Value
$a_{cons+D/A}$	$\left(\frac{Vb1 - Vbo}{ID}\right)^2$
a_{mirror}	$\left((Vb1 - Vbo)\frac{IN}{ID^2}\right)^2$
$a_{T\text{-}Norm}$; a_{Io}; a_{CFMF}	$\left(\frac{Vb1 - Vbo}{ID}\right)^2 \alpha_i^2 + \left(\frac{(Vb1 - Vbo)\,IN}{ID^2}\right)^2 - 2\left(\frac{IN}{ID}\right)\alpha_i\left(\frac{(Vb1 - Vbo)}{ID}\right)^2$

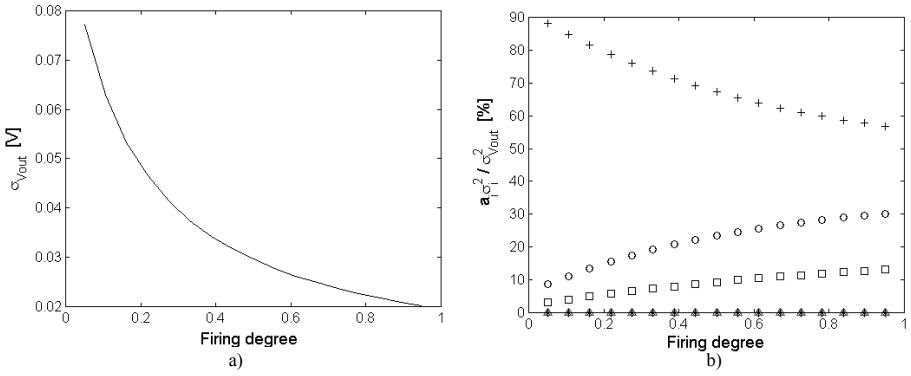


Fig. 6. a) Simulated σ_{Vout} with only one active rule as a function of the firing degree of the rule. b) Individual contribution of each building block to the total output variance: (+) divider; (o) consequent+D/A; (□) mirror before *ID*; (◊) T-Norm; (△) CFMF and (*) *Io*.

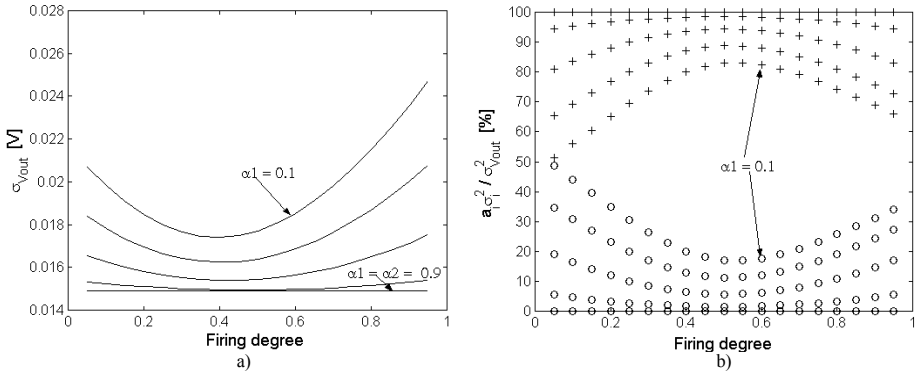


Fig. 7. a) Simulated σ_{Vout} assuming two rules fired in a complementary way. The singleton of one rule ($\alpha 2$) was set to 0.9. In the other rule the singleton ($\alpha 1$) ranges parametrically from 0.1 to 0.9. b) Individual contributions to the total output variance for different values of the singleton $\alpha 1$: (o) CFMF+T-Norm+*Io* and (+) divider.

-Fig. 7 b) attests that the main error contribution is again caused by the divider. In [12] it was proven that the maximum standard deviations of the divider take place when its denominator input current *ID* gets smaller. In this example, owing to the complementary rule activation mode, the denominator current remains constant and equal to Io=10μA. For these reasons, for a given pair of singletons values $\alpha 1$ and $\alpha 2$, σ_{Vout} in Fig. 7 a) remains almost independent of the firing degree of a rule and smaller than in Fig. 6 a). Let us reconsider the results of the previous simulation. In Fig. 6 a) when the rule firing degree gets smaller the current at the denominator of the divider becomes also smaller. This explains the larger values of σ_{Vout} for the small rule activation degrees (i.e.: firing degree < 0.4). Therefore, a good rule of thumb for keeping the mismatch errors introduced by the divider small is to avoid small currents *ID* at the denominator. This last condition is ensured as long as the contiguous membership functions overlap considerably so as to allow a complementary activation of the neighboring rules. This is normally the case in a fuzzy controller.

IV. Experimental Results

In the fabricated two-input, one-output, nine-fixed rules controller, there are three fuzzy labels available per input. Each four-parameters CFMF is 18-bit programmable (2x5 bits for knees and 2x4 bits for slopes). Consequents singletons are 5-bit programmable. Tail current Io is set to 10μA. The input voltages range from 1.5V to 4.5V. With Vbo=1.7V and $Vb1$=2.7V at the divider, its output voltage *Vout* ranges between the latter two values (i.e.: $0 < Vo = Vout - Vbo < 1$V). Fig. 8 a) and Fig. 8 b) show the simulated and measured output surfaces respectively for a particular setting of the controller. The RMSE between these surfaces remains in 27mV (2.7%). Fig. 8 c) and Fig. 8 d) illustrate the relative error surface between measured and simulated output values and the distribution of these errors, respectively. Notice from the latter figure that most relative errors are concentrated inside a band of ±3%.

The transient behavior of the controller has been typified by measuring the total input/output delay for small and large amplitude step signals, which are applied at one of the inputs while biasing the other with a constant voltage level. In Fig. 9 a) the amplitude of the input step has been set to ΔVin=500mVpp whereas the output reacts in 190ns (for the 90% of the steady state value) with a 100mVpp pulse. In Fig. 9 b) the former experience is repeated but sweeping one input over the whole input voltage range (ΔVin=3V). In this case a 500mVpp pulse is settled at the output in 450ns

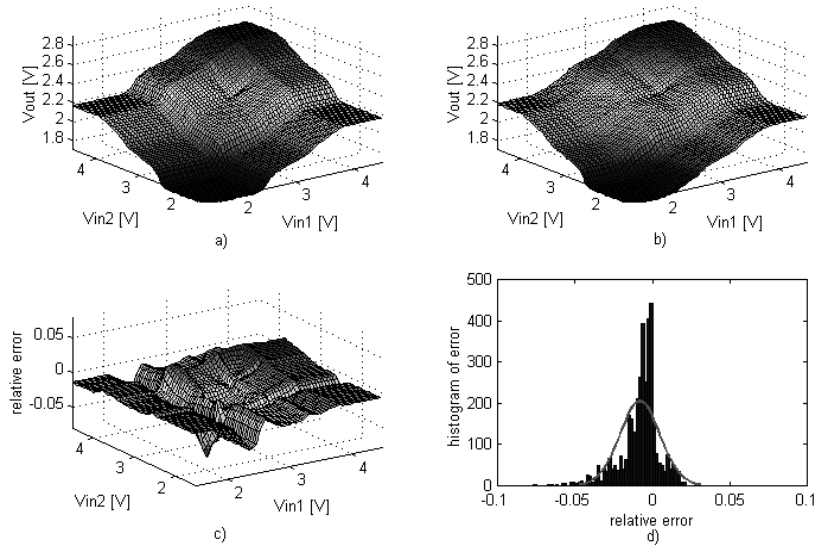
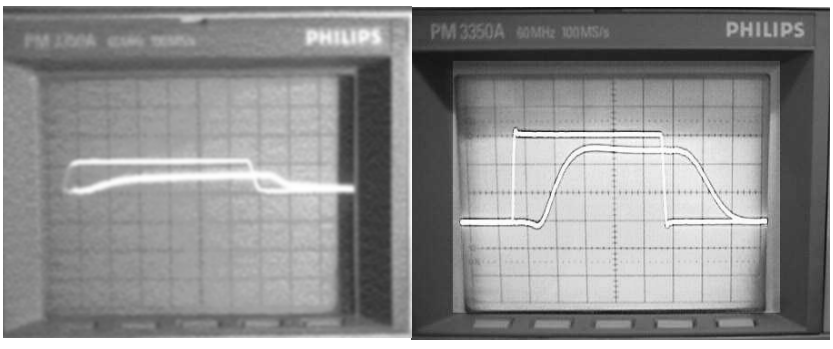


Fig. 8. dc test results: a) Simulated output surface. b) Measured output surface. c) Measured relative error surface. d) Relative error distribution.



a) b)

Fig. 9. Step response of the controller: a) Small amplitude input step (ΔVin = 500mV). Vertical scales: input = 0.5V/div - output = 0.2V/div. Time scale: 100 ns/div. b) Large amplitude input step (ΔVin = 3V). Vertical scales: input =1V/div - output = 0.2V/div. Time scale: 200 ns/div.

(90% Sty. St.). Consequently, the speed of the controller ranges from 2.22 to 5.26 Mflips for an estimated output load capacitance of *CL*=13pF. Extrapolating these results for *CL*≤5pF the delay should range from 125ns to 235ns. Hence, up to 8 Mflips could be achieved inside the chip.

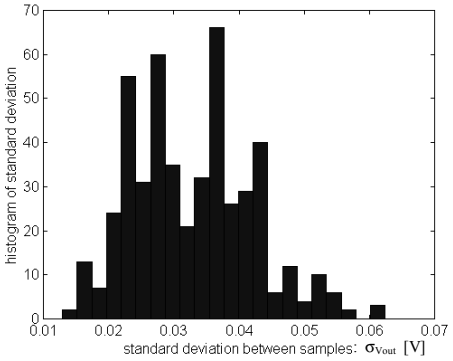
In addition, the dispersion between samples due to the process parameters fluctuations has been characterized for the dc test. The result extracted from six measured prototypes is shown in Fig. 10 a). The standard deviation of the controller's output varies from point to point over the inputs' domain while featuring a peak of 62.5mV (6.25%) and a mean value of 35mV (3.5%).

Fig. 10 b) shows the microphotograph of the controller. Its core occupies 3040 x 1500 μm^2 including digital storage circuits that represent almost the 50% of the total area. The measured power consumption rises to 13.4 mW (core: 8.4mW - buffer: 5mW) for *Vdd*=5V. Table II shows most relevant transistors sizes and circuits performances. Table III summarizes the global performance measured in this prototype.

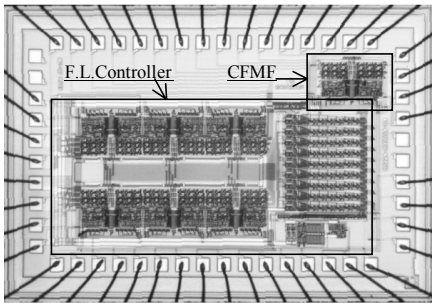
V. CONCLUSIONS

It has been shown that Mixed-Signal techniques can trade accuracy for a flexibility improvement while holding the advantages of the analog circuits for massive, parallel and fast computation together with the feasibility of digital circuits for storage. The use of widespread digital memory circuits to store the digital representation of the controller's parameters largely simplifies the on-chip programming strategy. In this way, our standard CMOS technology prototype behaves as a static RAM for programming purposes whereas the signal processing is carried out in the analog domain with a reasonable accuracy.

Sharing functional operators, particularly fuzzifiers labels and consequents weighting D/A, and performing optimal blocks interfacing by avoiding the use of intermediate signal converters (i.e.: I-to-V and/or V-to-I converters), have played an important role during the design step. Practiced in depth these general guidelines led to an improved modularity, reflected in smaller silicon area, lower power consumption, reduced need of storage capacity



a)



b)

Fig. 10. a) Distribution of the Standard Deviation of the controller's output in the dc test from six measured samples. b) Microphotograph of the chip: Fuzzy Logic Controller and testing CFMF.

TABLE II
MOST RELEVANT TRANSISTORS SIZES (IN μm/μm) AND CIRCUITS PERFORMANCES.

CFMF: Transconductor							
Input Range		Io	MR1, ML1			MR3, ML3	MR2, ML2
1.5V<Vin<4.5V		10μA	{12/12, 12/12, 20/4}			22/3.2	45/2.4
CFMF: Differential Amplifiers DAL & DAR						CFMF: Performance	
Ip	M1	M2	M3, M4	M5	M6	Current Consump.	Active Area
10μA	2 x 10/8	10/8	35/4	40/4	30/2.4	220 μA (max)	3800μm^2

2-Input MAXIMUM circuit						
M1	M2, M3	M4, Mc1	M5, Mc2	Input/Output Range	Delay	Current Consumption	Active Area
12/4	24/2.4	12/2.4	10/10	0≤ Iin, Imax ≤10μA	~50ns	40μA (max)	773μm^2

Weighting D/A					
Mda– bit 0, bit 1	Mda – bit 2	Mda – bit 3	Mda – bit 4	Current Consump.	Act. Area
5/5	10/5	20/5	28/5	30μA (max)	4672μm^2

Divider								
M1-3	M4-6	M7-12	Input Range	Vb1	Vbo	Output Swing	Current Consump.	Active Area
10/10	20/8	28/4	0 ≤ IN, ID ≤ 30μA	2.7V	1.7V	1V	30μA (max)	1452μm^2

TABLE III
SUMMARY OF THE PERFORMANCE OF THE PROPOSED MIXED-SIGNAL FUZZY LOGIC CONTROLLER

Fuzzy Logic Controller			
Technology:	CMOS-2.4µ	Programmability:	M.F.Slopes: 2x4bits M.F.Knees : 2x5bits Singletons: 5bits
Complexity:	9-rules @ 2-input @ 1-output		
Power Supply:	5 V	Total storage capacity needed:	153 bits
Power Consumption:	Core: 8.4mW Buffer: 5mW	Input/Output delay (90% steady-state):	Small signal: 190ns Large signal: 450ns
Area:	Analog: 2.3mm^2 Digital: 2.2mm^2	Standard deviation among samples: (6 Prototypes)	Max: 62.5mV (6.25%) Mean: 35mV (3.5%)
Accuracy:	RMSE: 27mV (2.7%)		

and even shortened internal delays.

Experimental results confirm that this controller is suitable for low-power embedded subsystems for applications with bandwidths below 8 MHz. The use of fast controllers with small rules count has been reported in several real-time applications [1][9][10] and their requirements are fairly fulfilled by this prototype.

VI. ACKNOWLEDGEMENTS

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