Analysis of Defects Generated by the Reflow Soldering in SMT (Surface Mount Technology) Assembly Applying the Six Sigma Method

Ana C. Bueno[1], Maíra P. Shiki[2], Valdemir R. de Lima[3], Luis G. Brandão[4], and Maurício M. Oka[5]

[1,5]Ana C. Bueno and Maurício M. Oka, Laboratory of Integrated Systems, at the Department of Electronics Systems, at the Polytechnic School of the University of São Paulo, São Paulo, S.P., Brazil, e-mail: (abueno, oka)@lsi.usp.br
[2,3,4]Maíra P. Shiki, Valdemir R. de Lima and Luis G. Brandão, Itaute/Philco, Jundiaí, S.P., Brazil, e-mail: (mairap, vronaldo, luisgb)@itaucom.com.br

***Abstract*— The Six Sigma method using the DMAIC methodology is being applied for analyzing the reflow soldering process in an SMT assembly line. The Define phase (D) and Measure phase (M) were concluded, the Analysis (A) phase is being implemented, and the Improve (I) and Control (C) phases will be the next ones. Defects generated during the reflow process were classified and measured both on assembled memory modules and on virgin laminates that were passed through the oven during the reflow of these modules. Spots of solder and flux were found on the edge connector of the modules and also on the surface of the virgin laminates. It was found that these defects are generated inside the reflow oven, indicating that the oven is contaminated. Two solder pastes were analyzed and consequently, two temperature profiles were used. The amount of defects generated by the oven was found to be independent on the temperature profile. On the other hand the amount of defects depends on the solder paste that is used. The FMEA (Failure Mode and Effect Analysis) was also accomplished. As a result, the main failure modes of the reflow process were determined, namely, the heating rate, the soak temperature, the conveyor velocity, the reflow temperature, the reflow time, and the cooling rate.**

***Index Terms*— DMAIC methodology, reflow soldering, Six Sigma, SMT.**

I. Introduction

In the 80's, SMT (Surface Mount Technology) begun to gain momentum for becoming the main board assembly technology [1, 2]. In SMT, components are soldered to the PCB (Printed Circuit Board) by wave soldering or by reflow soldering. In SMT with reflow soldering, solder paste is stencil printed over the contact islands patterned over the PCB, components are placed over these islands and then the PCB is reflow soldered. At present, reflow soldering using forced convection of hot air [3] is the dominant process.

Defects can be generated during the SMT assembly, making PCBs to be reworked or even to be discarded, increasing costs and lowering quality. In order to reduce the amount of defects, quality control methods must be implemented. Montgomery presents a timeline of Quality Methods that allows following the evolutionary process of the matter [4]. Six Sigma, which was developed by Motorola in the 80's is one of such methods. It is an SPC (Statistical Processed Control) driven approach. Six Sigma has a process capability target of 3.4 DPMO (Defects per Million Opportunities) that is achieved by reducing process variability (standard deviation) [5, 6, 7]. Statistical tools are extensively used to understand the manufacturing process, which allows predicting process results. The Six Sigma can be implemented by DMAIC methodology [8, 9] that stands for Define, Measure, Analyze, Improve, and Control. In this methodology, firstly, a product, a process, the process steps and a customer are defined, defects are identified, and the needs of the customer are found. In the second phase, key characteristics are measured. Cause and effect diagram, process map, and effect and cause matrix are made. In the third phase, the collected data are analyzed using statistical tools such as FMEA (Failure Mode and Effect Analysis), DOE I (Design of Experiment I), and DOE II. The chief causes of defects are identified. In the fourth phase, the process is improved and a process window is established. Solutions to the problem are developed, and process changes are made. In the fifth phase, the process is put under control, i.e., the process is monitored to assure that no unexpected changes occur.

In order to characterize the reflow process using a hot air forced convection oven, in the present work, the Six Sigma method is implemented by applying the DMAIC methodology.

II. Experimental Procedure

A Conceptronic HVA 102 forced convection reflow oven using hot air, is employed in the SMT process that is being analyzed. The boards are transported through the oven by a conveyor. The oven consists of seven heating zones and one cooling zone. The temperature in each heating zone is adjusted in order to reproduce, at the solder joint, the desired temperature profile. Each heating zone has a top and a bottom blower system. These blowers force the air through heaters and dispersion plates, creating jets of hot air that heat the boards. Most of the air circulates inside one zone, but part of the air passes to the next zone. At the last zone, part of the air is exhausted and the loss is compensated by the injection of fresh air. As a result there is a gradual exchange of the air inside the oven, allowing keeping the trade-off between avoiding the super saturation of the oven environment by volatile compounds and maximizing the thermal efficiency. The forced convection is characterized by the fact that the PCB and the assembled components are close to the thermal equilibrium with the hot air making it easy to adjust the temperature and to reduce the temperature variation across the board.

The first two phases of the DMAIC methodology for analyzing the reflow soldering process with the Conceptronic HVA 102 forced convection reflow oven were accomplished. As a result, defects generated during the reflow

soldering process were classified and measured. The study of such defects was carried out by the inspection of both the assembled memory modules and the virgin laminates. The third (Analysis) phase has been partially implemented. The FMEA was accomplished and the failure modes were determined.

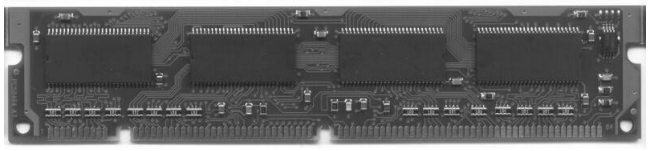


Fig. 1. Memory module selected as the product to be analyzed in this study.

A. Definition Phase

It was made a decision to apply the Six Sigma method in order to optimize the reflow process in the SMT assembly. The DDR (Double Data Rate) memory module shown in Fig. 1 was arbitrarily selected as the product to be analyzed. There are DDR memory modules with components assembled just on one of the PCB faces (single face) and on both faces (double face). In any case, each module has an edge connector with 92 pins patterned on each face with electrodeposited gold finish. Each pin is 1 mm wide and 2.4 mm long. The face that is assembled first is named "face A" and the other, "face B". Each memory module is 133 mm wide and 32 mm long.

However panels, that are sets of memory modules, rather than each memory module separately, are processed through the SMT assembly line and the modules are separated only after reflow soldering is accomplished. Each panel has 7 memory modules and it is 144 mm wide and 238 mm long. The SMT assembly flow for double face modules is shown in Fig. 2. The stencil printing process was previously optimized applying the Six Sigma method and the present work will focus on the reflow process. After the reflow, electrical tests and visual inspection are carried out. Thus, these steps are the customers for the reflow.

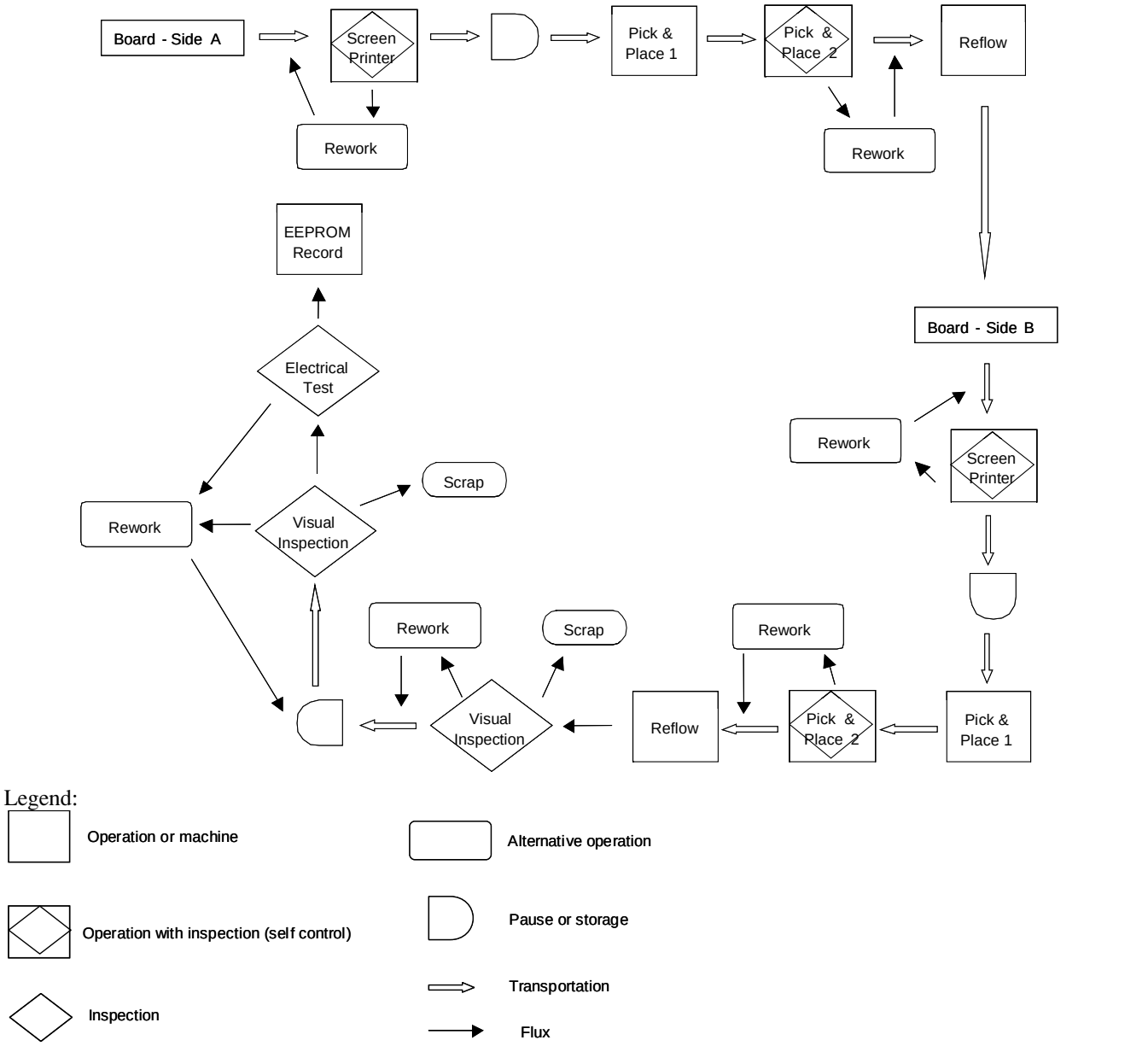


Fig. 2. SMT assembly flow for the DDR memory modules.

Two solder pastes are employed in this work, namely, solder paste C and solder paste D. The solder paste C has the following characteristics: 62Sn36Pb2Ag alloy, type 3 powder, i.e., mesh size (–325/+500), and metal load of 90.25% by weight. The solder paste D has the following characteristics: 62Sn36Pb2Ag alloy, type 3 powder, i.e., mesh size (-325/+500), and metal load of 90% by weight.

In order to achieve a reliable soldering it is key to get the temperature profile recommended by the solder paste manufacturer at the solder joint. The temperature profile is a curve of the solder joint temperature as a function of the reflow time and it is measured by thermocouples attached to a reference panel, using the M.O.L.E. (Multichannel Occurrent Logger Evaluator) Temperature Profiler from ECD Inc. The reference panel has 8 single face modules with five ICs soldered on it. Two ICs are soldered on the first module, one IC is soldered on the fifth module, and two others are soldered on the eighth module. The distributions of the ICs on the panel, as well as the locations of the solder joints where thermocouples are attached are schematically shown in Fig. 3. The purpose of this arrangement is to observe the temperature variation across the plate. The thermocouple tips are soldered with tin. The thermocouples wires are attached to the board by high-temperature adhesive tapes in order to minimize mechanical stress that could break the solder joint. Each thermocouple is connected at one channel of the M.O.L.E. equipment. As a result, five profiles are measured each time the reference board is passed through the oven. Each reference board can be used twenty times at most without degradation.

The temperature profile measured for the case that solder paste C is used is shown in Fig. 4a, and the temperature profile for the case that paste D is used is shown in Fig. 4b. For each solder paste, just one temperature profile is shown. The other four profiles for each solder paste were omitted but they were very close to the profiles that are shown.

B. Measurement Phase

In order to find the potential causes of defects in a reflow soldering process, a Cause and Effect diagram, also known as fishbone chart, was produced, as shown in Fig. 5. A brainstorming process with the participation of process engineering, characterization, test, and operation personnel produced this chart.

The cause and effect chart allows determining the variables that must be considered in the Process Map (flowchart). The process Map is shown in Fig. 6. The subprocesses of the reflow soldering are given in the column “Process Flow”, namely, the pause time, the transport by the conveyor, the preheating, the soak, the reflow and the cooling. For each step, input variables correlated to the subprocess are listed in the column “Inputs”. In the same way, the defects correlated to the sub-process are listed in the column “Outputs”. These output variables were identified in the cause and effect diagram. Typical values and ranges for the values of the output variables are also listed in the column “Output”, when available.

Key parameters were established and a Cause and Effect Matrix were generated as shown in Fig. 7. Each line of the matrix is associated with a possible cause of defect (input

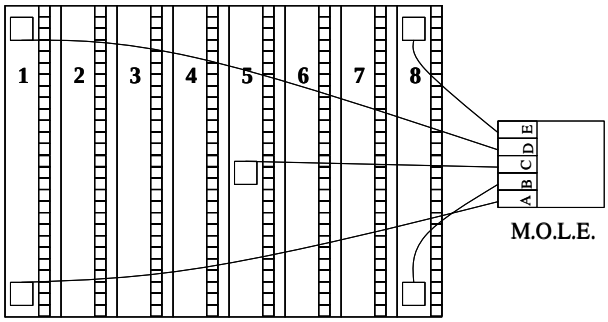
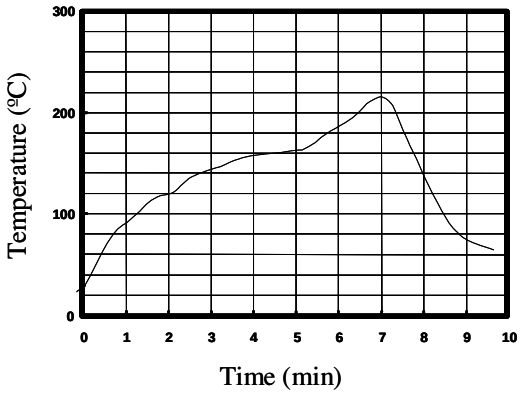
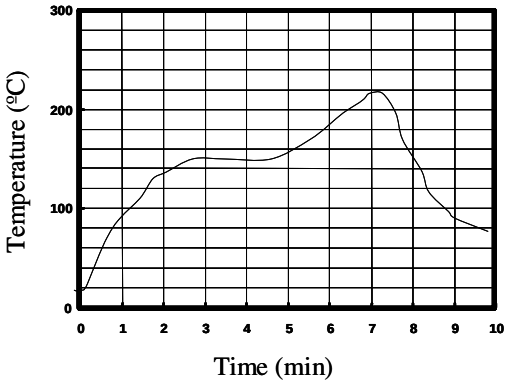


Fig. 3. Schematic of the distributions of the ICs on the panel, as well as the locations of the solder joints where thermocouples are attached.



a)



b)

Fig. 4. Temperature profile measured with the MOLE equipment. a) Profile measured when the solder paste C is used. b) Profile measured when the solder paste D is used.

variable) and each column, with a defect (output variable). In the line "priority for the customer", in Fig. 7, each element is a value between 1 and 10, arbitrarily attributed in order to indicate how harmful is the defect for the customer. The value is the largest for the most critical defect. On the other hand, each element of the matrix is a value that indicates the degree the input variable affects the defect. If the input variable is not related to the defect, grade 0 is attributed. If there is a minor possibility that the variable affects the defect, grade 1 is attributed. If it is reasonable to assume that the variable affects the defect, grade 4 is attributed. If it is certain that the variable affects the defect, grade 9 is attributed. In the column "Total", it is given the summation of the products of the values in each element by the values of the corresponding elements in the "priority for the customer" line. Then, the matrix lines are sorted according to the values in "Total" column, as shown in Fig. 7. This

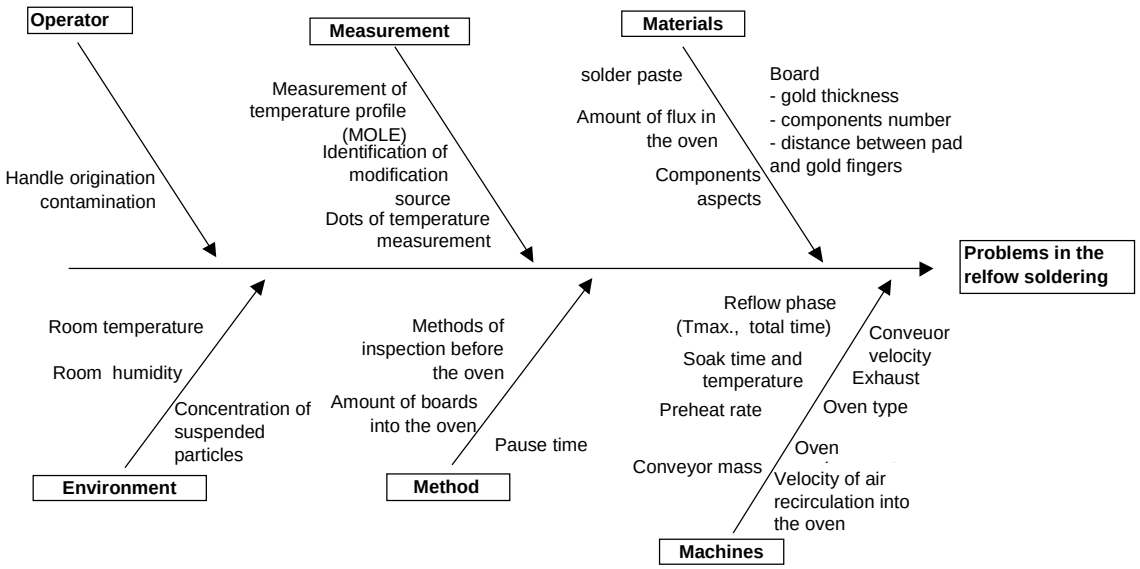


Fig. 5. Cause and Effect diagram for the reflow process.

last step will help us to accomplish the FMEA (Failure Mode and Effect Analysis) in the Analysis phase.

Now it is required to measure the actual level of defects in the reflow process (types and amount). Two SMT assembly runs with 61 single face plates and one run with 47 double face plates were carried out. One of the SMT assembly runs with 61 plates employed the solder paste D and the other two SMT assemblies, with 61 plates and 47 plates, employed the solder paste C. In order to determine the defects, all plates were visually inspected.

As the plates pass through the whole SMT process there is a possibility that the cause of a defect is not the reflow process, but rather, one of the previous processes. In order to find which defects are generated during the reflow process, 20 virgin laminates 154 mm wide and 60 mm long were passed randomly through the oven during ordinary reflow of memory modules assembled with solder paste C. Similarly, 40 laminates were passed during the reflow of memory modules assembled with solder paste D. Some of the laminates had copper on both faces and others, just on one of the faces. The laminates were analyzed using an optical microscope.

C. Analysis Phase

In this phase, firstly, the FMEA ("Failure Mode and Effects Analysis") was accomplished. The FMEA is a problem prevention tool that focus on the solution of the most critical problems. The FMEA is a technique that offers a methodology to facilitate process improvement. Part of the FMEA that was accomplished, corresponding to the preheating region, is shown in Fig. 8.

The reflow process was divided in sub-processes. In the field "process description / process objective", the sub-processes are briefly described. The potential failure modes are presented in the next field. The defects related to each mode are listed in the field "potential effect of the failure mode". It is noteworthy that a failure mode can be related to various defects. Values are attributed, in a scale of 1 to 10, to describe the severity of each defect for the consumer. The values are presented between parentheses. The value 1 indicates that the defect severity to the consumer is minimum. But when the defect severity to the consumer is considered high, the attributed value is 10. The highest of the values attributed to the defects related to each mode is transcribed to the field "severity (SEV)". In the field "potential cause", problems that can lead to the manifestation of the failure mode are listed. In the field "occurrence (OCCUR)" the rate of occurrence for each one of the problems is estimated. The score for the occurrence is related with the probability of occurrence of the problem and is a value between 1 and 10. The value 1 indicates that the probability of the problem to occur is very low. The value is larger, the higher is the probability of the problem to occur. Actions that can be taken for preventing the problem to occur, as well as methods used to monitor the problems and to act on its causes, are associated to each one of the problems as indicated in the field "current controls – detection". In the field "current controls – prevention", the actions to prevent the occurrence of the problems are indicated. For each action, a value is attributed in a scale of 1 to 10 describing the probability to detect the failure mode. The values are presented between parentheses. The value 1 indicates that the detection probability is very high, i.e., that the failure mode certainly will be detected. The value 10 indicates that the detection probability is very low, i.e., that the failure mode will certainly not be detected. The smallest value amongst the attributed to the "current controls" for each failure mode is transcribed to the field "detection (DETEC)". In the field "Risk Priority Number (RPN)", the product of severity, occurrence and detection index (or ranking) is given. The higher is the value, more critical is the associated failure mode. For the potential causes with the higher values of the RPN, the actions that will be taken to solve the problems are described in the field "recommended actions". The recommended actions have the intent of lowering the occurrence, severity and detection index (or ranking). For the FMEA carried out in this study, the process was divided in preheating region, soak region, reflow region and cooling region. The actions were ranked according to the values found in RPN. The Design Of Experiment (DOE) is the recommended actions when the potential cause is an inadequate specification of

REFLOW	PROCESS DIAGRAM & IDENTIFICATION OF THE VARIATION SOURCES REFLOW OF SOLDER PASTE	
INPUT (Variation Sources)	Processo Flux	OUTPUT (Products and Process Characteristics)
Pause time Contamination Temperature of the room Humity of the room	PAUSE	Maximum pause time: 2-3 horas Humity 30-56% Temperature 22-26%
Trail deformation Dirt on conveyor Locking of conveyor Conveyor mass	CONVEYOR Track Trail	Trail Dimension (slump)
Temperature Time Velocity Component type Amount of flux within the paste Exhaust Density of components Amount of boards within the oven Paste type	PREHEATING	Preheating Rate 2- 5 °C/s (there is not specification) End Temp. 130ºC (component cracking)
Temperature Time Velocity Component type Amount of flux within the paste Exhaust Density of components Amount of boards within the oven Paste type Flux type Oven type Velocity of air recirculation Oven environment Conveyor mass Board type Component mass Teperature profile Amount of solder paste	SOAK	Solder Paste C Temperature: 130 - 175ºC Time: 60 - 120 s Solder Paste D Temperature: 130 - 175ºC Time: 90 - 150 s Reduction of oxide (Flux Evaporation) (Make the temperature uniform)
Time Peak temperature Temperature Velocity Component type Exhaust Density of components Amount of boards within the oven Paste type Laminate type Ramp rate Board characteristics Temperature profile Board finish Moisture absorption by epoxy	REFLOW	Fulfil the standard IPC-A-610 Solder Paste C Time: 30 - 90s Temperature: 183 - 225°C Reflow Temperature: 215 +/- 10 ºC Solder Paste D Time: 30 - 90s Temperature: 183 - 225 Reflow Temperature: 215 +/- 10 ºC
Time Velocity Temperature Cooling rate Paste type Exhaust	COOLING	Cooling rate: 2- 5 °C/s (there is not specification)

Fig. 6. The Process Map for the reflow process.

Input Variables	Solder balls / Solder beading	Cracks of components	Tombstoning	Contamination by flux	Bridging	Poor wetting	Cold joints	Board warped	Solder joint cracks	Solder on the edge connector	Contamination on the edge connector	
	5	9	9	6	9	7	9	9	9	8	4	Total
Reflow Temperature	9	9	9	9	4	9	9	9	9	9	1	679
Reflow time/velocity	9	9	9	9	4	9	9	9	9	9	1	679
Amount of solder paste	9	0	9	9	9	9	9	0	0	9	0	477
Paste type	9	0	4	9	9	9	9	0	4	9	0	468
Soak time	9	0	9	9	0	9	9	0	0	9	1	400
Fux type	9	0	4	9	4	9	9	0	1	9	0	396
Soak temperature	9	1	4	9	0	9	9	1	0	9	1	373
Amount of flux within the paste	9	0	1	9	4	9	9	0	1	9	0	369
Board finish type	9	0	9	0	1	9	4	0	1	9	9	351
Component type	0	9	9	0	9	0	0	0	0	0	4	259
Preheat rate	9	9	0	4	4	1	1	1	1	4	0	252
Oven environment	1	0	0	0	0	9	4	0	9	0	9	221
Component mass	9	9	9	0	0	0	1	0	0	0	0	216
Frequency of cleaning	1	0	1	9	1	1	1	0	0	9	9	201
Contamination of the conveyor	4	0	0	1	4	1	0	0	0	9	9	177
Locking of the conveyor	1	1	0	1	0	4	4	9	0	1	0	173
Cooling rate	0	9	0	0	0	0	0	0	9	0	0	162
Humidity of the room	4	0	0	4	1	4	4	0	0	4	1	153
Velocity of air flux	4	0	1	9	0	0	1	0	0	4	4	140
Pause time	1	0	1	0	1	4	4	0	0	1	9	131
Density of components	0	1	1	0	4	4	0	0	0	4	1	118
Conveyor stretching	0	4	0	0	0	0	0	9	0	0	0	117
Exhaust	1	0	0	9	0	0	0	0	0	1	9	103
Handling	4	0	0	0	1	0	0	0	0	4	9	97
Moisture absortion by the epoxy	0	9	0	0	0	0	0	0	0	0	4	97
Type of laminate	0	0	0	0	0	0	0	9	0	0	0	81
Amount of boards within the oven	1	0	0	4	0	1	1	0	0	1	4	69
Room temperature	1	0	1	0	1	1	1	0	0	1	0	47
Conveyor mass	0	0	0	1	0	1	1	0	0	0	0	22

Fig. 7. Cause and effect matrix for the reflow process.

TABLE I
DEFECTS FOUND ON THE MEMORY MODULES BY VISUAL INSPECTION

	solder paste C		solder paste D
Face	single	double	single
# of assembled plates	61	47	61
# of defects	15	44	999

the failure mode. The failure modes that will be analyzed will be the heating rate, the soak temperature, the conveyor velocity, the reflow temperature, the reflow time, and the cooling rate. In this phase, the next action will be to define the experiments.

III. Results and Discussion

The memory modules were analyzed by visual inspection. Even though a number of defects are reported in the literature for the SMT assembly, e.g., solder balls, solder beads, tombstoning, etc, the only defects that were found on our plates were spots on edge connectors. Being the only defects found, it was decided to analyze these defects. The amounts of these defects are summarized in Table I. It is worth to mention that a single side memory module passes just once through the reflow oven, while a double side memory module passes twice. Both modules have the same edge connector pattern. The slight difference on defect density for "face A" and "face B" were considered negligible but it should be necessary to analyze a larger amount of plates to verify this assumption.

It is also important to mention that just few plates were analyzed. Thus, the present results do not show that the spots on the solder edge are the only defects generated in

PROCESS DESCRIPTION / PROCESS OBJECTIVE	POTENTIAL FAILURE MODE	POTENTIAL EFFECTS OF FAILURE	SEV	POTENTIAL CAUSES	OCCUR	CURRENT CONTROL - DETECTION	CURRENT CONTROL - PREVENTION	DETEC	RPN	RECOMMENDED ACTIONS
Preheating Region Objective: increase of the board temperature to soak temperature (130ºC)	Very high preheat rate	crack of component (6)	6	inadequate specification	10	verification of the profile through MOLE (6)	visual inspection (7)	5	300	DOE
						recommendation by paste supplier (5)				
		solder ball (4)				check list (set up) (5)				
		solder on the edge connector (4)		burnt motor	2	preventive maintenance (5)	electrical test (6)	5	60	
						visual display in the oven (5)				
						MOLE (6)				
		contamination by flux (3)		burnt fan	2	check the fan (2)		2	24	
	Dirt on the conveyor	contamination by flux (3)	3	broken or turned off exhaust	2	control panel (main switch) (9)	visual inspection (8)	6	36	
						visual display (6)				
				release of particles from the oven walls	3	periodic conveyor cleaning (each three months) (7)		7	63	

Fig. 8. The FMEA for the reflow process represented by the preheating region.

our reflow soldering process. More plates should be analyzed in order to study other types of defects.

The defects were classified in two groups: spots of solder and spots of solvent or flux. In this work we will refer to the latter type of defect only as flux spot. Solder spots observed by an optical microscope are shown in Fig. 9a and Fig. 9b and the flux spot is shown in Fig. 9c. However, solder spots and flux spots cannot be easily distinguished during the visual inspection, i.e., without using an optical microscope. Thus, in this study, where large amount of plates must be analyzed, what is feasible only with visual inspection, the two types of defects were not distinguished.

The existence of flux spots indicates three possibilities. The flux comes from the solder paste that is deposited over the patterned contact islands, there is flux residues as a subproduct of a faulty printing process, or the oven environment is super saturated with flux, even though the oven was carefully designed to minimize such effect. The latter assumption appears to be the most reasonable because the edge connector is considerably far from the contact islands and printing process has been carefully optimized.

The same analysis is valid for the solder spots, however, at first, it was somewhat difficult to accept that solder spots can be generated inside the oven and more tests were required. It would be much more reasonable to say that the stencil printing step is the source of this type of defect.

The experiment with virgin laminates allows identifying the source of the defects. Even though the laminate surface is made of copper without a gold finish, it is assumed that the mechanism for the formation of the defects is the same as on the surface of the edge connector. Transporting the laminates through the oven randomly during the reflow soldering of the memory modules will expose the copper surface to the same condition that the edge connectors are exposed.

Defects were found on the surface of virgin laminates and they were also classified as solvent or flux spots (Fig. 10a) and solder spots (Fig. 10b). They are the same defects observed on the edge connectors. These results show that solder spots appear even on laminates that were never put in contact with the solder paste. Thus it is clearly shown that solder spots can be generated inside the reflow oven, indicating that the oven is contaminated. In other words, solder spots can appear even if the stencil printing step is perfect. It was not found yet, which part of the oven is contaminated neither, if the contamination can be eliminated. There is the possibility that the contamination is inherent for the type of the oven that is used. The virtually closed environment where the air is circulated over and over may inhibit the elimination of flux spots and solder spots.

The amount of defects on virgin laminates that were randomly passed through the oven while plates with solder paste C were reflowed are shown in Fig. 11a. Assuming a normal distribution, a mean of 1.95 defects/face and a standard deviation of 1.64 defects/face were determined. Similarly, the amount of defects on virgin laminates that were randomly passed through the oven while plates with solder paste D were reflowed, are shown in Fig. 11b. A mean of 1.80 defects/face and a standard deviation of 1.64 defects/face were determined. The results show that the

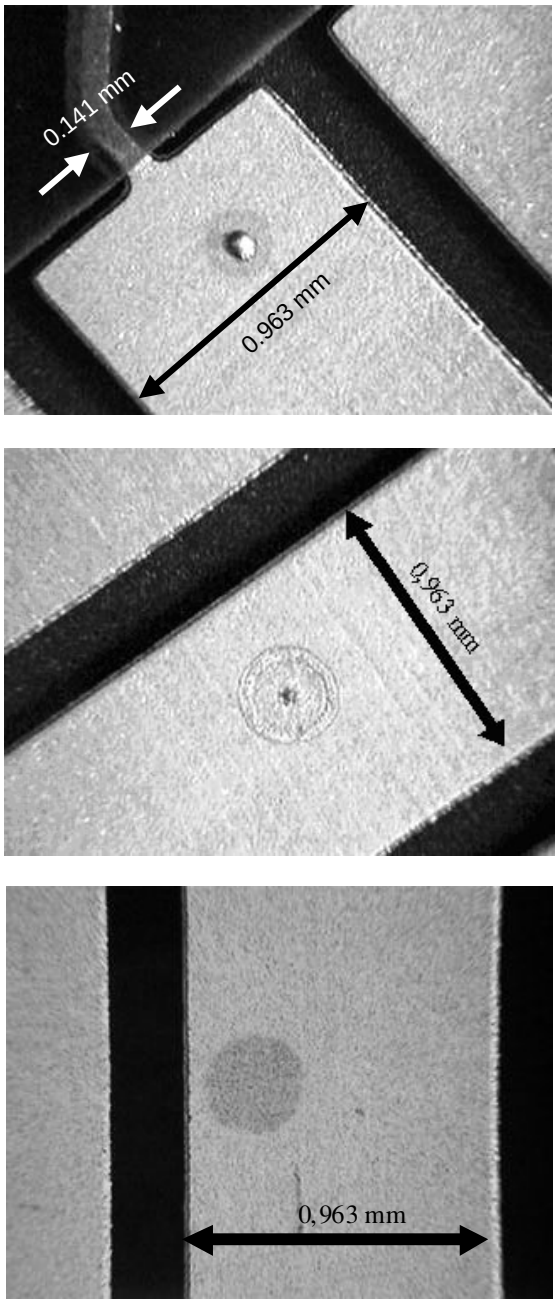


Fig. 9. Defects on the edge connectors of the DDR memory modules. a) Spot of solder. b) Spot of solder. c) Spot of solvent or flux.

amount of defects on the laminates, generated inside the reflow oven, does not change when the temperature profile changes from that for solder paste C to that for solder paste D. The amount of defects does not also change by the fact that the plates neighboring the laminates are assembled with the solder paste C or D.

The mean density of defects generated inside the reflow oven during the reflow of solder paste C is calculated as 2.11×10^{-4} defects/mm^2 and the standard deviation, 1.78×10^{-4} defects/mm^2. Similarly, for the laminates passed through the reflow oven during the reflow of solder paste D, the mean density is calculated as 1.95×10^{-4} defects/mm^2 and the standard deviation, 1.78×10^{-4} defects/mm^2. As the total area occupied by the pins of the edge connector on a plate is 3091.2 mm^2, the amount of defects generated inside the oven on the edge connector can be calculated as the product

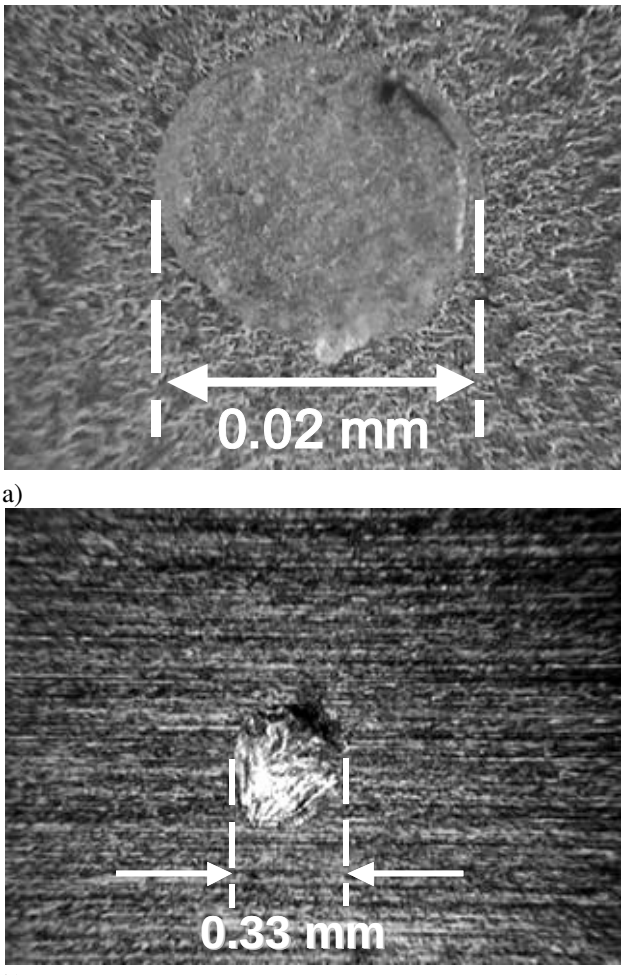


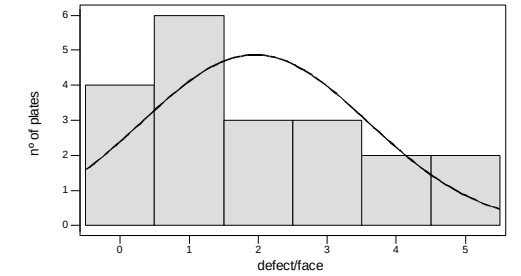
Fig. 10. Contamination found on virgin laminates after the reflow. a) Solvent or flux spot. b) Solder spot.

of the mean defect density and the area occupied by the edge connector. The values expected for each test are shown in Table II. It is worth to mention that a double face module passes twice through the oven and the amount of expected defects is twofold. When the solder paste C is used, the expected values are even larger than the experimental values. Thus, for the solder paste C we could say that all defects observed on the edge connectors are generated in the reflow oven. But when the solder paste D is used, the expected value is much smaller than the experimental.

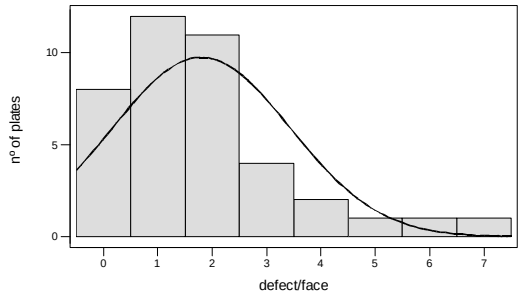
Thus the oven cannot be considered as the only source of defect for the case that the solder paste D is used. Thus it can be conclude that the amount of defects generated during the reflow soldering is dependent on the solder paste that is used. From this study, however, it cannot yet be concluded that the solder paste D generates more defects than the solder paste C during the reflow soldering. There is still the possibility that the defects are related to the solder paste printing-step. In other words, it is possible that the printing quality of the solder paste D is poorer than the printing quality of the paste C, leading to the present results.

TABLE-II
RELATIONSHIP BETWEEN THE AMOUNT OF DEFECTS EXPECTED AND THE AMOUNT OF DEFECTS OBSERVED EXPERIMENTALLY ON THE EDGE CONNECTORS.

	Amount of defects expected	Amount of defects observed Experimentally
47 double face plates with solder paste C	61±52	44
61 single face plates with solder paste C	40±34	15
61 single face plates with solder paste D	37±34	999



a)



b)

Fig. 11. Amount of defects found on virgin laminates. a) Laminates passed through the reflow oven with plates with solder paste C. b) Laminates passed through the reflow oven with plates with solder paste D.

IV. CONCLUSIONS

We have begun to implement the Six Sigma method using a DMAIC methodology for analyzing the reflow process in an SMT assembly line. The electrical test and visual inspection were determined as the customers for the reflow. The DDR memory module was chosen as the product to be analyzed. In this study, spots of solders and flux on the edge connectors of the memory modules were found to be the most abundant defects. The present study showed that the reflow oven could generate at least part of such defects. It was also shown that these defects can be strongly affected by the type of the solder paste that is used.

The design of experiment will be the next step of the analysis phase. The actions to be taken to eliminate the most critical potential causes of defect will be defined. The potential causes to be attacked will be the heating rate, the soak temperature, the conveyor velocity, the reflow temperature, the reflow time and the cooling rate.

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