A Compact Low-Distortion Low-Power Instrumentation Amplifier

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ABSTRACT

A CMOS instrumentation amplifier based on a simple topology that comprises a double-input G_m-stage and a low-distortion class-AB output stage is presented. Sub-threshold design techniques are applied to attain high figures of differential-gain and rejection parameters. Analyses of input-referred noise and CMRR are comprehensively carried out and their dependence on design parameters determined. The prototype was fabricated in standard n-well CMOS process. For 5V-rail-to-rail supply and bias current of 100nA, stand-by consumption is only 16μW. Low-frequency parameters are A_{DM}=86dB, CMRR=89.3dB, PSRR+=87dB, PSRR-=74dB. For a 6.5pF-damping capacitor, Φ_M=73° and GBW=47KHz. The amplifier exhibits a THD of –64.5dB @100Hz for a $1V_{pp}$-output swing. Input-noise spectral density is 5.2μV/ Hz @1Hz and 1.9μV/ Hz @10Hz, which gives an equivalent input-noise of 37.6μV, over 1Hz-200Hz bandwidth. This circuit may be employed for low-frequency, low-distortion signal processing, advantageously replacing the conventional 3-opamp approach for instrumentation amplifiers.

Index Terms: Instrumentation amplifier, double-port amplifier, class-AB output stage

1. INTRODUCTION

Instrumentation amplifiers (IA´s) are essential parts wherever a small differential voltage must be accurately amplified in the presence of a strong common-mode input voltage. It should thus feature high input-impedance, low input-referred noise and offset voltage, large open-loop differential-voltage gain and substantially reject variations on common-mode and power-supply voltages. For many control and low-frequency signal processing circuits, IA´s with a gain-bandwidth product (GBW) of tens of KHz would meet most of these requirements.

In many applications, such as sensor interfaces, the overall performance of the system is limited by the offset and noise of input amplifiers. In this respect, chopper modulation and auto-zeroing can be used to improve these figures [1-2]. A current-switching modulation approach that improves CMRR against EMI interference is also described in [3]. Although exhibiting good performance, such techniques demand great circuit complexity and dissipation. Current-feedback IA´s topologies can also be found in literature [4-6].

Upon very-low power consumption budget, a standard 3-opamp implementation of IA´s [7] is generally adopted, with both offset and noise minimized by properly sizing input transistors of differential pairs. Nevertheless, a 3-opamp IA still requires a significant Silicon area. Furthermore, it depends on excellent matching between several relatively large resistors to meet CMRR stringent necessities. To handle these limitations, the insertion of an auxiliary differential-pair in the input-stage of a standard opamp topology has been reported in literature. In [8], a switched-capacitor amplifier with an auxiliary input works out offset cancellation. Subjected to charge injection noise and capacitor mismatching, this solution is better applied to discrete-time applications. A good alternative is the so-called Differential Difference Amplifier (DDA) that comprises a compound of two differential-pairs [9].

This paper introduces a compact low-distortion CMOS instrumentation amplifier comprising a double-port transconductance (G_m-stage). Based on the DDA approach, the differential-pairs in this proposal are however cross-coupled with respect to incremental currents stirred by input signal. Such currents are conveyed to a summing node at G_m-stage output and converted into voltage. Additionally, a low-distortion, unity-gain output stage allows moderate capacitive and resistive load driving capability. Stability is achieved by a

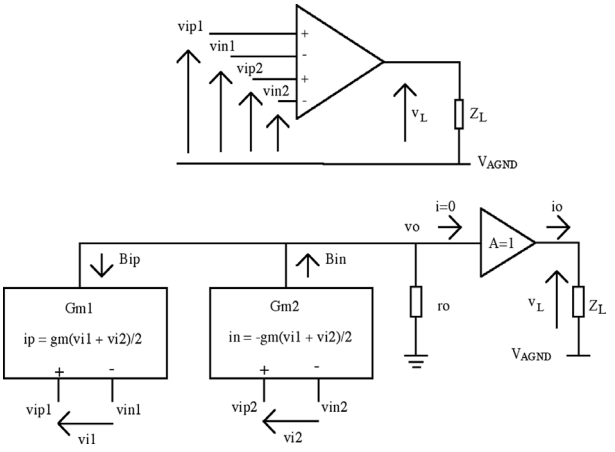

Figure 1. Instrumentation amplifier block diagram

grounding capacitor. Large values of differential gain and rejection parameters are attained at very-low current bias. A simple resistive feedback network sets the voltage gain. Additionally, first-order equations are developed for prescribing CMRR as function of mismatching, as well as for noise properties.

2. CIRCUIT DESCRIPTION

The symbolic diagram of the amplifier is depicted in Figure 1. It consists of a double-port G_m-stage and a voltage-follower output stage. Superimposed to a common-mode voltage V_{CM}, differential signals $v_{i1}=(v_{ip1}-v_{in1})$ and $v_{i2}=(v_{ip2}-v_{in2})$ are respectively applied to input ports of G_{m1} and G_{m2}. Small-signal currents Bi_p and Bi_n, respectively driven by (v_{ip1},v_{ip2}) and (v_{in1},v_{in2}), are summed up and voltage-converted at G_m-stage output.

The amplifier schematic is shown in Figure 2. G_{m1} and G_{m2} comprise differential-pairs respectively formed by transistors M_{1A}, M_{1B} and M_{2A}, M_{2B}, all operating in weak inversion. Incremental currents i_p and i_n are conveyed to the G_m-stage output node scaled by a factor B. Current mirrors M_{3A} - M_{8B} operate in strong inversion to improve accuracy. A push-pull output stage composed by transistors M_9 - M_{12} and bias sources I_{A1} and I_{A2} allows resistive loading to the amplifier. No quiescent current flows to/from the G_m-stage upon ideal matching between I_{A1} and I_{A2}. Frequency stability is achieved by a damping capacitor C_C.

Some dc and low-frequency properties of the instrumentation amplifier are now discussed. Subscripts DM and CM underline either pure differential-mode or common-mode drive, respectively.

2.1 Negative Feedback

Figure 3 shows the negative feedback to stabilize the amplifier gain. Neglecting the offset voltage, in the presence of a common-mode voltage $V_{CM}' = V_{CM} + V_{AGND}$, one has

$$V_{out} = \frac{v_{in} + \frac{1}{CMRR}\left(\frac{v_{in}}{2} + V_{CM}'\right) + V_{AGND}\left\{\frac{1}{r+1} + \frac{1}{CMRR_1} + \frac{1}{2CMRR_2}\left[1 + \frac{1}{1+(1/r)}\right]\right\}}{\frac{1}{A_{DM}} + \frac{1}{r+1}\left(1 - \frac{1}{2CMRR_2}\right)} \quad (1)$$

where A_{DM} is the open-loop differential gain, $CMRR_i$ the individual common-mode rejection ratio of G_{mi} and $r = R_2/R_1$. As in a conventional opamp, if $A_{DM} \to \infty$, and denoting $v_{out} = V_{out} - V_{AGND}$, the closed-loop gain is fully determined by the feedback network as

$$\frac{v_{out}}{v_{in}} \cong \frac{1}{r+1} = \left(1 + \frac{R_2}{R_1}\right) \quad (2)$$

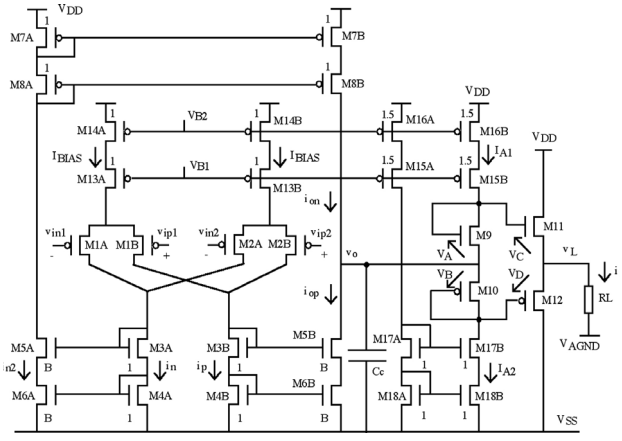

Figure 2. Instrumentation amplifier schematic.

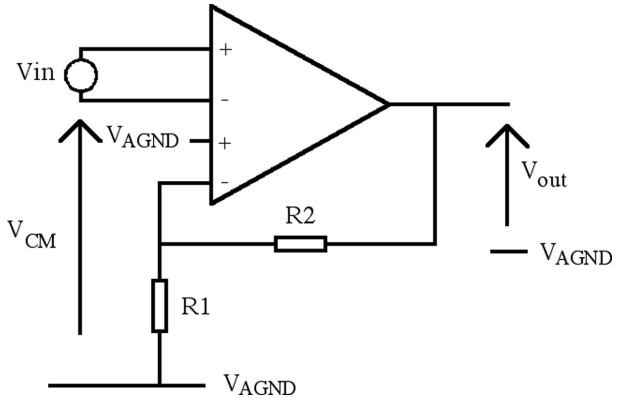

Figure 3. Gain-stabilization through negative feedback.

2.2 Open-loop Differential-Mode Voltage Gain

Let's assume transistors pair-wise matched and ideal sources I_{BIAS}. By superposition,

$$A_{DM1} = A_{DM2} = \frac{I_{BIAS}}{2\eta U_T} \frac{1}{g_o} \quad (3)$$

where A_{DM1}, A_{DM2} are the open-loop voltage gains referred to inputs v_{i1} and v_{i2}, respectively.

2.3 Common-Mode Rejection Ratio

To evaluate the response to a general common-mode drive, let's represent V_{CM1} and V_{CM2} as common-mode voltages applied to G_{m1} and G_{m2}, respectively. The low-frequency small-signal circuit of G_{m1} is illustrated in Figure 4. Finite resistance R_{B1} represents a non-ideal I_{BIAS}, whereas g_{mA} and g_{mB} replace low-impedance devices M_{3A} - M_{4B}. Input-transistors finite output resistances r_{o1A} and r_{o1B} are also considered. As a result of V_{CM1}, a common-mode current i_{CM} will flow through R_{B1}. Similar fact occurs in G_{m2}. Upon assumption of $r_{oiA}g_{m1A}>>1$ and $r_{oiB}g_{m1B}>>1$, incremental v_{i1} and v_{i2} voltages are

$$v_{i1} \cong \frac{V_{CM1}}{1+(g_{m1A}+g_{m1B})R_{p1}} \tag{4a}$$

$$v_{i2} \cong \frac{V_{CM2}}{1+(g_{m2A}+g_{m2B})R_{p2}} \tag{4b}$$

where $R_{p1} = R_{B1}//r_{o1A}//r_{o1B}$ and $R_{p2} = R_{B2}//r_{o2A}//r_{o2B}$. Incremental currents i_{CMn} and i_{CMp} are

$$i_{CMn} = i_{CM1A} + i_{CM2A} = \frac{g_{m1A}V_{CM1}}{1+(g_{m1A}+g_{m1B})R_{p1}} + \frac{g_{m2A}V_{CM2}}{1+(g_{m2A}+g_{m2B})R_{p2}} \tag{5a}$$

$$i_{CMp} = i_{CM1B} + i_{CM2B} = \frac{g_{m1B}V_{CM1}}{1+(g_{m1A}+g_{m1B})R_{p1}} + \frac{g_{m2B}V_{CM2}}{1+(g_{m2A}+g_{m2B})R_{p2}} \tag{5b}$$

Mirrored by a factor B to G_m-stage output node, these currents produce a common-mode voltage gain A_{CM}. To obtain an exploitable analysis for CMRR, different mismatching sources are assumed orthogonal. Expressions to be given are function of relative deviations in geometry and process parameters between G_{m1} and G_{m2}.

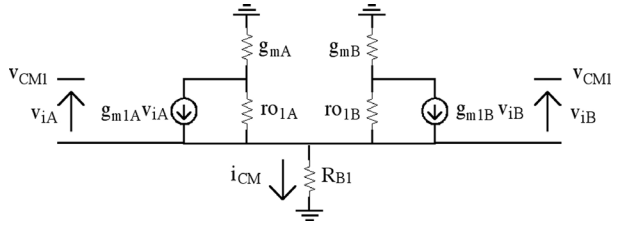

Figure 4. Low-frequency small-signal circuit of port G_{m1}.

2.4 Mismatching on Current Mirroring

Departures from ideal current mirrors are herein represented by correcting mirroring ratios through a factor $(1 + \alpha)$, where α embodies device mismatching and λ-effect. As a result,

$$CMRR_A = \frac{A_{DMA}}{A_{CMA}} = \frac{1+X}{1-X}(1+2g_mR_p) \tag{6}$$

where

$$X = \frac{1+\alpha_3}{(1+\alpha_1)(1+\alpha_2)} \tag{7}$$

and α_1, α_2 and α_3 are respectively associated with ratios i_{n2}/i_n, i_{on}/i_{n2} and i_{op}/i_p, as established by the circuit of Figure 2. $CMRR_A$ reaches then infinity as $X\rightarrow1$, which theoretically corresponds to perfect mirroring. The offset component V_{osA} due to current mirror mismatching is

$$V_{osA} = \eta U_T\left[(1+\alpha_1)(1+\alpha_2) - (1+\alpha_3)\right] \tag{8}$$

2.5 Mismatch on Threshold Voltage

Local mismatches on threshold voltages of input transistors also degrade CMRR. Although a large combination of relative mismatching between all four input transistors is possible, only two mismatch conditions are examined: between devices of a same differential pair (B_1) and from distinct input pairs (B_2).

B_1) $M_{1A} \equiv M_{2A}$ and $M_{1B} \equiv M_{2B}$: in weak inversion and denoting $\Delta V_{TH1} = V_{TH1B} - V_{TH1A}$ and $\Delta V_{TH2} = V_{TH2B} - V_{TH2A}$, it turns out

$$CMRR_{Bi} = \frac{A_{DMB}}{A_{CMBi}} = \frac{1+2g_mR_{pi}}{2}\frac{1+exp\dfrac{-\Delta V_{THi}}{\eta U_T}}{1-exp\dfrac{-\Delta V_{THi}}{\eta U_T}} \tag{9}$$

with $CMRR_{Bi}$ related to port G_{mi}. The offset component V_{osBi} is

$$V_{osBi} = 2\eta U_T\frac{1-exp\dfrac{-\Delta V_{THi}}{\eta U_T}}{1+exp\dfrac{-\Delta V_{THi}}{\eta U_T}} \tag{10}$$

B_2) $M_{1A} \equiv M_{1B}$ and $M_{2A} \equiv M_{2B}$: as tail currents are now equally split, input devices have identical $g_m=I_{BIAS}/(2\eta U_T)$. By defining $\Delta V_{TH12} = V_{TH1A}-V_{TH2A} = V_{TH1B} - V_{TH2B}$, an effective common-mode voltage $V_{CM2} - \Delta V_{TH12}$ is then applied to G_{m2}. From (5a) and (5b), common-mode currents would be canceled out at G_m-stage output node, with no first-order degeneration of CMRR.

2.6 Mismatch on Transistor Size

Similarly to previous analysis, relative mismatches on aspect-ratio (W/L) are twofold:

C_1) $M_{1A} \equiv M_{2A}$ and $M_{1B} \equiv M_{2B}$: Transconductance is unbalanced by geometry mismatch in the same differential pair. Expressing $(W/L)_{1A}/(W/L)_{1B}=k_1$ and $(W/L)_{2A}/(W/L)_{2B} = k_2$, one has

$$CMRR_{Ci} = \frac{A_{DMC}}{A_{CMCi}} = \frac{k_i+1}{2(k_i-1)}(1+2g_mR_{pi}) \quad (11)$$

with $CMRR_{Ci}$ related to port G_{mi}. The offset term V_{osCi} is

$$V_{osCi} = 2\eta U_T \frac{k_i-1}{k_i+1} \quad (12)$$

C_2) $M_{1A} \equiv M_{1B}$ and $M_{2A} \equiv M_{2B}$: Let's now assume $(W/L)_{1A}/(W/L)_{2A} = (W/L)_{1B}/(W/L)_{2B} = k_{12}$. Likewise to case B_2, a same g_m for all input transistors yields identical, but opposite current-mode currents at the stage output, so that CMRR would not be degraded by k_{12}.

Combining all described mismatch contributions, straightforward manipulation of (6) - (12) works out

$$\frac{CMRR_A V_{osA}}{(1+\alpha_1)(1+\alpha_2)+(1+\alpha_3)} = CMRR_B V_{osB} = CMRR_C V_{osC} = \eta U_T(1+2g_mR_p) \quad (13)$$

As can be observed, the product between CMRR and V_{os} components remains constant, at a given temperature. Therefore, any relative increase on V_{os} implies an identical decrease on CMRR, and vice-versa. The amplifier overall CMRR can be first-order estimated by

$$\frac{1}{CMRR} \cong \frac{1}{CMRR_A} + \frac{1}{CMRR_B} + \frac{1}{CMRR_C} \quad (14)$$

with corresponding input-referred offset voltage given by

$$V_{os} \cong V_{osA} + V_{osB} + V_{osC} \quad (14)$$

Therefore, CMRR can be enhanced by increasing the transconductance and/or accomplishing a high value for R_p association. Setting differential-pair transistors in weak inversion and implementing I_{BIAS} with long-channel cascode devices meet both conditions. Weakly-inverted input devices also reduce V_{osB}, while large geometries lower V_{osC}. The offset term V_{osA} is minimized by using cascode current mirrors in strong inversion. In addition, common- centroid and careful layout reduce V_{os}, leading to a higher CMRR. It´s worthy noticing from (6), (9) and (11) that all CMRR components would approach infinity if respective mismatch coefficients vanished, despite a finite R_p. Nonetheless, such a condition is strictly based on the assumption of an ideal cancellation of common-mode currents at the G_m-stage output node.

To provide a numerical insight, let's assume $\alpha_1 = \alpha_2 = \alpha_3 = 0.1$, $\Delta V_{TH1}=\Delta V_{TH2}=2mV$, $k_1=k_2=1.02$, $g_m=1.67\mu A/V$, $\eta=1.2$ and $R_p=1G\Omega$. It comes out $CMRR_A$= 96.9dB, $CMRR_B$=94dB and $CMRR_C$= 104.5dB, so that overall CMRR is 87.9dB.

2.7 Noise Figures

As inherent noise represents a fundamental limitation in instrumentation amplifiers, design considerations to reduce it are now discussed. Figure 5 shows noiseless devices in the single-port G_m-stage, with equivalent gate-connected noise sources v_{ni}. It's assumed that the noise produced in the output stage does not significantly contribute to the equivalent input-referred noise, as it´s divided by the high voltage-gain of first-stage.

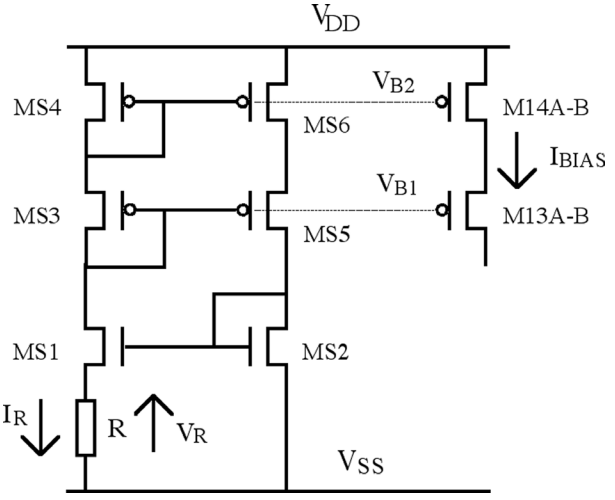

Figure 5. Noise sources in G_m-stage.

Small-signal noise gains from input to output of G_m-stage can be determined using a low-frequency equivalent circuit, where each source introduces a noise current $g_{mi}v_{ni}$. Considering matched devices M_{1A}-M_{1B}, M_{3A}-M_{4B}, M_{5A}-M_{6B} and M_{7A}-M_{8B}, noise gains associated with input transistors correspond to $A_{n1A} = A_{n1B} = A_{DM}$, and are given by (4). Noise currents due to mirror transistors in strong inversion and conveyed to the output node yield

$$A_{n3A} = A_{n3B} = A_{n4A} = A_{n4B} = \frac{Bg_{m3}}{g_o} = \frac{B}{g_o}\frac{\sqrt{\beta_3 I_{BIAS}}}{1+\chi} \quad (16a)$$

$$A_{n5A} = A_{n5B} = A_{n6A} = A_{n6B} = \frac{Bg_{m5}}{g_o} = \frac{B}{g_o}\frac{\sqrt{\beta_5 I_{BIAS}}}{1+\chi} \quad (16b)$$

$$A_{n7A} = A_{n7B} = A_{n8A} = A_{n8B} = \frac{g_{m7}}{g_o} = \frac{1}{g_o}\sqrt{B\beta_7 I_{BIAS}} \quad (16c)$$

where $\chi = \partial V_{TH}/\partial V_{BS} = \gamma/[2(2\Phi_F+V_{BS})^{1/2}]$ [10]. The noise due to transistors implementing I_{BIAS} sources is seen as a common-mode signal, and therefore, assumed to be suppressed by the amplifier CMRR. Using superposition and considering noise sources all uncorrelated, the input-referred mean-square noise is

$$\overline{v_n^2} = \overline{v_{n1A}^2} + \overline{v_{n1B}^2} + \frac{A_{n3A}^2}{A_{n1A}^2}\sum_{i=3}^{6}\left(\overline{v_{niA}^2} + \overline{v_{niB}^2}\right) + \frac{A_{n7A}^2}{A_{n1A}^2}\sum_{i=7}^{8}\left(\overline{v_{niA}^2} + \overline{v_{niB}^2}\right) \quad (17)$$

and replacing (3) and (16a) - (16-c) into (17), one has

$$\overline{v_n^2} = \overline{v_{n1A}^2} + \overline{v_{n1B}^2} + \frac{(2\eta U_T)^2}{I_{BIAS}^2}\left[\frac{\beta_3}{1+\chi}\sum_{i=3}^{6}\left(\overline{v_{niA}^2} + \overline{v_{niB}^2}\right) + \frac{\beta_7}{1+\chi}\sum_{i=7}^{8}\left(\overline{v_{niA}^2} + \overline{v_{niB}^2}\right)\right]$$

Since the drain current in weak inversion transistors is mainly due to carrier diffusion, the gate-referred equivalent shot noise power of M_{1A} and M_{1B} is [11]

$$\overline{v_{n1A}^2} = \overline{v_{n1B}^2} = \frac{q(2\eta U_T)^2}{I_{BIAS}}\Delta f \quad (19a)$$

where q is the electronic charge and Δf is the equivalent noise bandwidth. As remaining devices operate in strong inversion, flicker and thermal noise are present. Since low-frequency applications are devised, flicker noise components prevail [12], which implies

$$\overline{v_{n3A}^2} = \overline{v_{n3B}^2} = \overline{v_{n4A}^2} = \overline{v_{n4B}^2} = \frac{KF_n}{(WL)_{3A}C_{ox}^2}\frac{\Delta f}{f} \quad (19b)$$

$$\overline{v_{n5A}^2} = \overline{v_{n5B}^2} = \overline{v_{n6A}^2} = \overline{v_{n6B}^2} = \frac{KF_n}{B(WL)_{3A}C_{ox}^2}\frac{\Delta f}{f} \quad (19c)$$

$$\overline{v_{n7A}^2} = \overline{v_{n7B}^2} = \overline{v_{n8A}^2} = \overline{v_{n8B}^2} = \frac{KF_n}{(WL)_{7A}C_{ox}^2}\frac{\Delta f}{f} \quad (19d)$$

where KF_n and KF_p are flicker coefficients for n- and p-channel MOSFET, respectively. Lastly, replacing (19a)-(19d) into (18), the amplifier input-referred noise spectral density turns out

$$\frac{\overline{v_n^2}}{\Delta f} = \frac{(2\eta U_T)^2}{I_{BIAS}}\left[2q + \left(1+\frac{1}{B}\right)\frac{4\mu_n K_{Fn}}{(1+\xi)L_{3a}^2 C_{oxf}} + \frac{1}{B}\frac{4\mu_p K_{Fp}}{(1+\xi)L_{7a}^2 C_{oxf}}\right] \quad (20)$$

Noise power decreases then with bias current, mirroring factor and channel length of mirror devices. The calculated noise spectral density as a function of B and L is displayed in Figure 6, where m is a multiplying factor applied to L_{3A}=10μm and L_{7A}=9.6μm. Optimal values of B lie between 2 and 4, as a further increase has little effect on noise reduction. Such a behavior is expected since (20) has also noise components with no dependence on factor B.

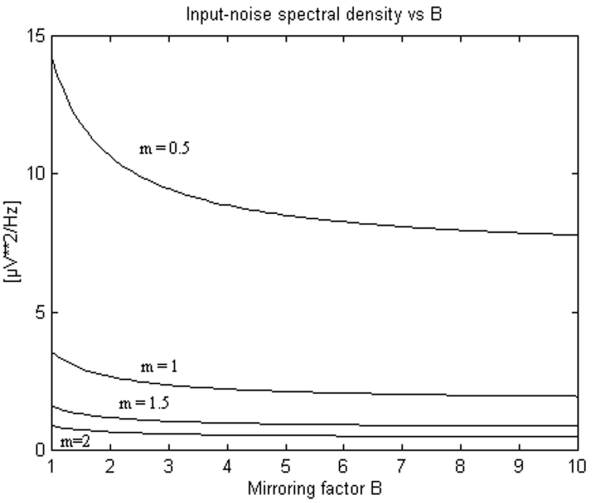

Figure 6. Spectral noise dependence on B and L_{3A}, L_{7A}.

2.8 Class-AB Output Stage

The class-AB output stage in Figure 2 meets the requirements for unity voltage-gain and appropriate bandwidth. Furthermore, it features circuit simplicity and controllability of quiescent current, essential for low-power applications. However, the use of source-followers drivers M_{11} and M_{12} intrinsically limit the output peak swing, as a voltage drop V_{GS} + $2V_{DSAT}$ is mandatory for biasing. To cancel out crossover distortion, M_{11} and M_{12} have their V_{GS} voltages balanced by voltage drops V_A and V_B of diode-connected M_9 and M_{10}, respectively. These devices are held in weak inversion by current sources I_{A1} and I_{A2}, which in turn are mirrored from I_{BIAS}. M_{11} and M_{12} operate in weak inversion with respective quiescent currents I_{Q11} and I_{Q12}. Upon ideal matching $I_{A1} = I_{A2} = I_A$, and assuming same η for both types of device and $I_D \cong I_{DO}(W/L)\exp(V_{GS}/\eta U_T)$ [13], the voltage balance in the TL loop yields

$$\ln\frac{I_A}{I_{DOn}\left(\frac{W}{L}\right)_9} + \ln\frac{I_{Q12}}{I_{DOp}\left(\frac{W}{L}\right)_{12}} = \ln\frac{I_A}{I_{DOp}\left(\frac{W}{L}\right)_{10}} + \ln\frac{I_{Q11}}{I_{DOn}\left(\frac{W}{L}\right)_{11}} \quad (21)$$

where I_{DOn} and I_{DOp} are process-dependent parameters. Imposing $(W/L)_9 = (W/L)_{11}$ and $(W/L)_{10} = (W/L)_{12}$ implies $I_{Q11} = I_{Q12} = I_Q$, so that no quiescent current flows to/from R_L. Moreover, as gate-to-gate voltage $V_{GG} = V_A + |V_B| = V_C + |V_D|$, it turns out $I_Q = I_A$. As current mirroring is reasonably accurate, good control of quiescent current is therefore achieved.

The amplifier output swing decreases as the load becomes less resistive. For a positive swing, M_{11} reaches strong inversion and linear operation still subsists as long as it remains in saturation. Defining V_{A1} as the minimum voltage across current source I_{A1}, V_{GS11} is limited to

$$V_{GS11\,max} = V_{DD} - V_{A1} - V_{Lpeak} - V_{AGND} \quad (22)$$

For low-frequency signals and given values of V_{Lpeak} and R_L, the aspect ratio of M_{11} is imposed by

$$\left(\frac{W}{L}\right)_{11} \geq \frac{2(1+\chi)}{\mu_n C_{ox}} \frac{1}{(V_{GS11\,max} - V_{TH11})^2} \frac{V_{Lpeak}}{R_L} \quad (23)$$

Similar analysis can be extended to sizing M_{12}, as determine by a negative excursion.

3. AMPLIFIER DESIGN AND SIMULATION

The circuit was designed according to a standard n-well 0.7μm CMOS process. Nominal parameters are V_{THN} = 0.83V, V_{THP}= -1.1V, $\mu_n C_{ox}$= 143μA/V², $\mu_p C_{ox}$= 41μA/V², γ_n= 0.74V$^{1/2}$, γ_p= 0.43V$^{1/2}$, $\eta_n \cong \eta_p$=1.2 and KF_n= 3.0x10^{-22}V²F and KF_p= 4.4x10^{-24}V²F. Standard deviations for V_{THN} and V_{THP} are 7mV and 25mV, respectively. A 5V rail-to-rail supply accommodates relatively large voltage drops across diode-connected transistors. The amplifier was specified for GBW = 30KHz and maximum stand-by consumption of 25μW. A preliminary analysis revealed that I_{BIAS}=100nA complies with both requirements.

Current I_{BIAS} is derived from the self-biased PTAT reference of Figure 7 [13]. As M_{S1} and M_{S2} operate in weak inversion, $V_R = I_R R = U_T \ln K$, where $K = W_{S1}/W_{S2} = 5$. Feedback produced by $M_{S1} - M_{S6}$ and internal noise would ideally build up I_R. However, a triggering path (not shown) is recommended to guarantee that the circuit starts if the supply voltage V_{DD} ramps up slowly. An off-chip resistor R in the reference-current generator gives current flexibility, whereas providing an insight on I_R dependence on V_{DD} variations. Cascode current mirrors with long-channel devices and low-level current boost the source resistance R_B, a necessary condition to a high CMRR.

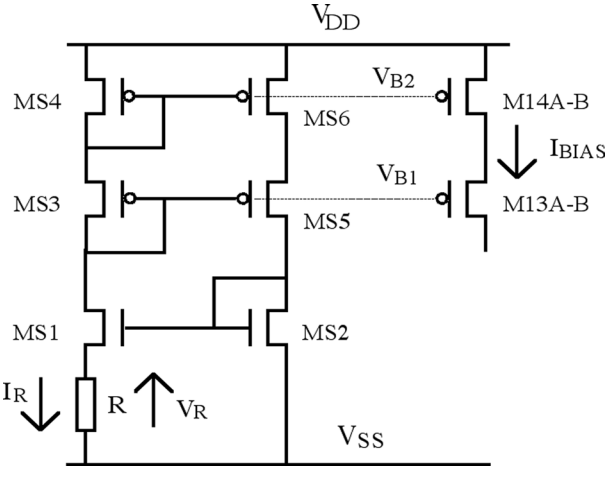

Figure 7. PTAT reference current generator.

The amplifier input-devices output conductance and their geometry mismatch are reduced by imposing a 10μm-minimum size. Their operation in weak inversion ensures a maximum g_m, while minimizing V_{osBi} terms. The maximum current in weak inversion, $I_{LIM} = 2\eta(W/L)\mu_p C_{ox} U_T^2$ [13], limits the aspect-ratio of input transistors. By choosing B=10, a trade-off between power consumption, intrinsic noise and suitable bandwidth is achieved. Again, long-channel cascode current mirrors enhance the gain-stage output resistance and lower V_{osA}. Moreover, the square-law dependence on L_3 and L_7 in (16) suggests a more effective noise reduction by adopting long-channel devices in current mirrors. Maximum length is however dictated by the output swing requirement. The push-pull stage was sized to comply with an 80μA-driving capability @R_L=10KΩ. Class-AB operation is achieved by setting the quiescent current I_Q to I_A=1.5I_{BIAS}=150nA, although simulation indicates I_Q=280nA. Apart from asymmetries on generating I_{A1} and I_{A2}, such a deviation is also credited to the body effect of M_9 and M_{11}. Since the drain current clean-exponential dependence on V_{GS} is inexact [14], the translinear (TL) loop $M_9 - M_{11}$ offsets I_Q from I_A to some extent. Additionally, an identical η factor for n- and p-type transistors is assumed.

Transistor drawn dimensions are listed in Table 1. Input transistors feature (10μm/10μm) sizing to ensure weak-inversion operation, whereas reducing offset voltage due to lithography mismatch. Loads $M_{3A} - M_{4B}$ and $M_{7A} - M_{7B}$ have long channel to lessen noise terms, as well as enhancing the voltage gain. M_{11}-M_{12} transistors have large aspect-ratio to provide relatively high current stirring, but L = 0.9μm was adopted to improve pair-wise matching of M_9-M_{11} and M_{10}-M_{12}. Long-channel $M_{15} - M_{18B}$ (L=20μm) improves the condition $I_{A1} \equiv I_{A2}$ to minimize the interference of crossover-distortion cancelation circuit on the amplifier gain stage.

Simulated results using PSPICE and Bsim3v3 models are low-frequency A_{DM}=93dB, phase margin Φ_M=55° and GBW=100KHz, for 6.5pF-damping capacitor. Closed-loop gains are in excellent agreement with (2). For a 10KΩ-load resistance, an output swing of 0.93V_{peak} and THD values of -70.5dB @10Hz and -50.8dB @100Hz are also predicted.

4. EXPERIMENTAL RESULTS

Figure 8 depicts the photomicrograph of the instrumentation amplifier, which occupies an effective area of 0.1mm². A second version of the amplifier, with an external C_C was also prototyped. On either version, access to the compensation node allows a deeper analysis on frequency stabilization. Measurements were taken with V_{DD}= 2.5V, V_{SS}= -

Table I. IA Transistor Sizing

	M_{1A} - M_{2B}	M_{3A} - M_{4B}	M_{5A} - M_{6B}	M_{7A} - M_{8B}	M_9, M_{11}	M_{10}, M_{12}	M_{13}- M_{14}	M_{15} - M_{16}	M_{17}- M_{18}
W(μm)	10	2	20	9.6	32	64	40	60	40
L(μm)	10	10	10	9.6	0.8	0.8	20	20	20

Table II. IA Experimental Parameters

Offset voltage	2.3mV (mean) , σ = 1.1mV
A_{DM}@1Hz	86dB
Φ_M	73°
GBW	47KHz
CMRR	82.8dB – 98.8dB
PSRR+	84.5dB – 91.3dB
PSRR-	71.8dB – 78.2dB
Common-Mode Input Range	-1.60V to +1.22V
THD@100Hz	-66.3dB@R_L=10KΩ , -58.7dB@R_L=1KΩ
$V_{noise}^2/\Delta f$ (input-referred)	5.2μV/√Hz@1Hz, 1.9μV/√Hz@10Hz

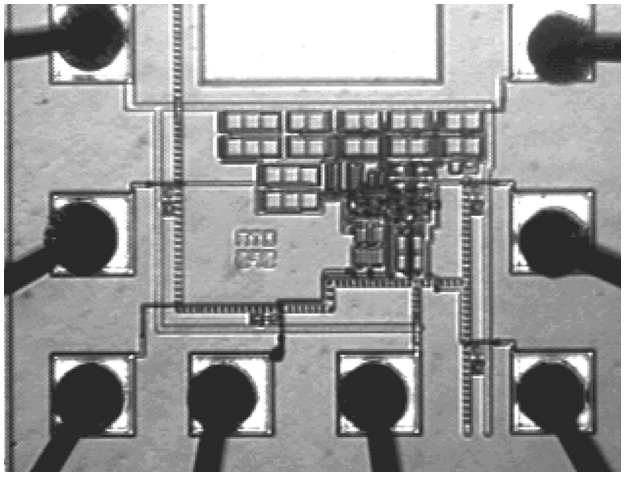

Figure 8. IA photomicrography.

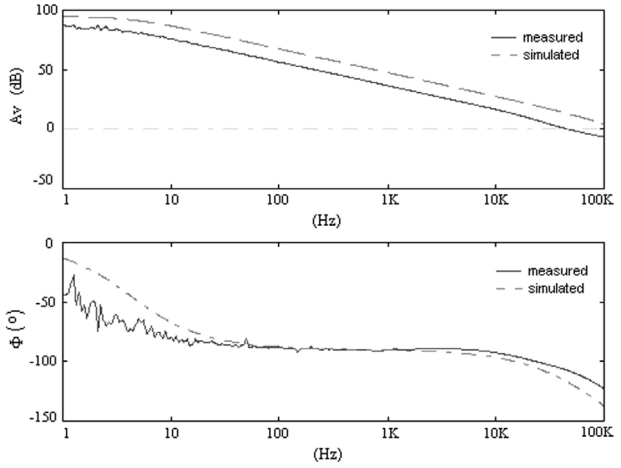

Figure 9. Simulated and experimental A_{DM} and Φ_M.

2.5V and V_{AGND}= 0V and summarized on Table 2. On-chip reference current is 100nA, for an overall stand-by power consumption of 13.4μW.

Figure 9 overlays simulated and experimental data of A_{DM} and phase-shift over a frequency span of 1Hz-100KHz, for R_L=10KΩ and C_L=12pF. Symmetry between input ports is confirmed by measuring practically identical characteristics of A_{DM} gain, after interchanging differential pairs.

Offset voltage has a mean value of 2.3mV and a standard-deviation (σ) of 1.1mV. Frequency characteristic of the amplifier rejection figures is displayed in Figure 10. CMRR, PSRR+ and PSRR- @1Hz are 98.8dB, 91.3dB and 78.2dB, respectively. As expected, the proposed amplifier features lower CMRR as compared to IA implementations using chopping techniques (140dB [4]) or current-feedback topologies (106dB [5]).

Measurements of input-referred noise spectral density give 5.2μV/√Hz @1Hz and 1.9μV/√Hz @10Hz, which corresponds to an equivalent input noise of 37.6μV, over 1Hz-200Hz bandwidth. Although the current-mode based IA in [5] presents a much lower equivalent noise (1.6μV), it demands larger power dissipation (50μW), however. Input-referred noise of the proposed IA can be further minimized by re-sizing differential-pair transistors, at expense of area.

Calculated and experimental data of the input-referred noise spectral density are superimposed in Figure 11. Measurements were collected by setting the amplifier as a voltage follower. A low-noise 60dB-gain external amplifier boosts the noise power before acquisition. Good agreement with (16) is attained at low frequencies, although no statistics for KF coefficients were available for calculation.

A voltage-follower configuration was used to obtain large-signal characteristics. As shown in Figure 12, good fitting occurs between calculated and measured low-frequency output swing as a function of load. For R_L=10KΩ, peak amplitude is 0.92V@100Hz and reduced to 0.85V@10KHz. Heavier load currents also

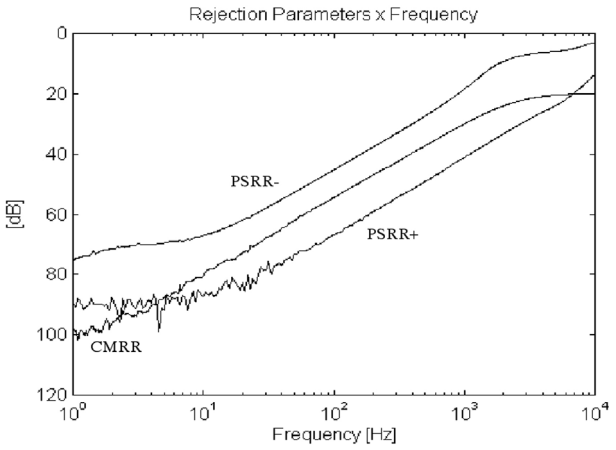

Figure 10. IA rejection parameters

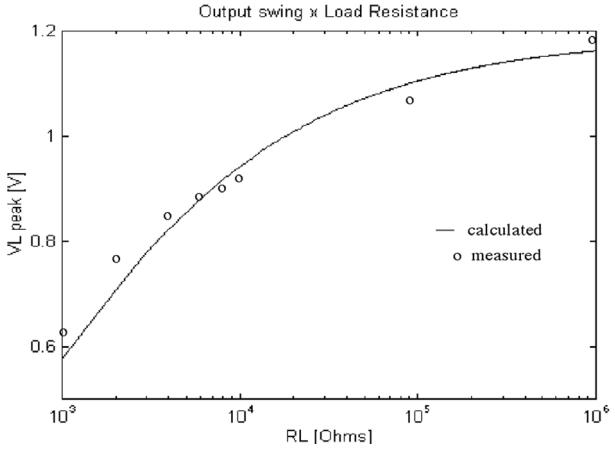

Figure 12. Output swing as function of R_L.

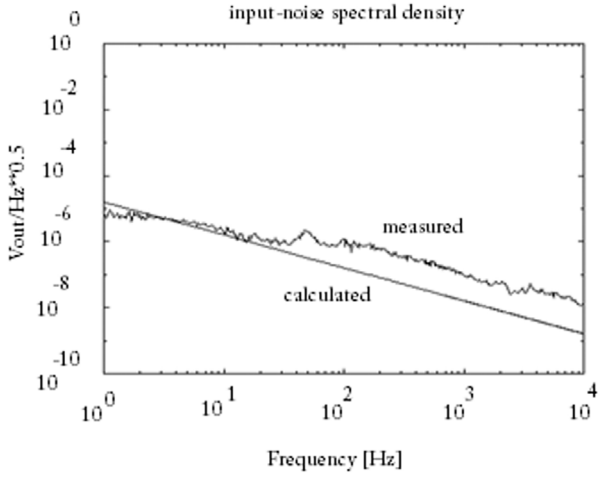

Figure 11. IA input-noise spectral density.

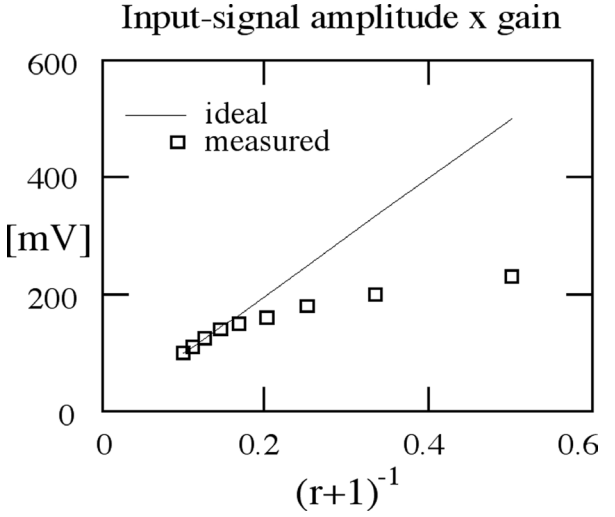

Figure 13. Signal amplitude as function of amplifier gain.

degrade linearity. For a 500mV-output, 100Hz-sinusoidal signal, THD decays from -66.3dB to -58.7dB for load resistances of 10KΩ and 1KΩ, respectively. Since nonlinearities associated with transconductance g_m are first-order canceled out in the differential stages, a major contributor to overall distortion is the push-pull circuit. As swing increases, transistors operating in saturation move towards the triode region. In addition, the mobility dependence on gate voltage and the body effect on M_{11} also degrade the linearity. A 40dB-gain was fixed by external resistors R_2=47KΩ and R_1=470Ω in the circuit of Figure 3. For a given output swing, the lowest resistive load (≅ R_2) is estimated from (23), whereas noise contribution limits its value to a maximum. A distortion measurement of an amplified 10KHz-sinusoidal signal exhibits a THD of –41dB, for 500mV-output amplitude. This figure improves to –64.5dB @100Hz.

Figure 13 shows the maximum amplitude of input signal @100Hz as function of the amplifier programmed gain, for a fixed THD of –44dB. At low gains of 5 and below, full output swing can no longer be attained since input pairs are driven out of their linear region by a high differential signal.

5. CONCLUSIONS

A simple topology for a CMOS instrumentation amplifier conceived for low-power, low-distortion electronics is introduced. It comprises a double-port G_m-stage and a low-distortion class-AB output stage to drive moderate capacitive and resistive loads. Low bias currents improve differential gain and rejection parameters, while still featuring a suitable bandwidth. Analytical expressions for CMRR and input-referred equivalent noise, in which their dependence on design parameters are described, are also presented.

The circuit was prototyped on a conventional n-well CMOS process and occupies an area of 0.1mm². For a rail-to-rail 5V-supply and I_{BIAS}= 100nA, stand-by consumption is 13.4μW. Open-loop measurements revealed a low-frequency A_{DM}=86dB, Φ_M=73° and GBW=47KHz for C_C=6.5pF, R_L=10KΩ and C_L=12pF. Offset voltage has a mean of 2.3mV and σ_{Vos}=1.1mV. Input common-mode range is [-1.60V, +1.22V]. For R_L=10KΩ, peak swing is 0.92V

@100Hz and 0.85V @10KHz. For a 500mV-output, THD@100Hz is -66.3dB for RL=10KΩ.

Experimental CMRR@1Hz varies from 98.8dB @V_{os}=0.7mV to 82.8dB@V_{os}=5.1mV. $PSRR^+$ and $PSRR^-$ values are within intervals [84.5dB, 91.3dB] and [71.8dB, 78.2dB], respectively. Good agreement between calculated and measured input-noise spectral density was attained. Noise measurements are 5.2μV/√Hz @1Hz and 1.9μV/√Hz @10Hz.

Owing to its compactness and low consumption, the proposed topology advantageously replaces bulky three-opamp instrumentation amplifiers. Input common-mode range can be further broadened by replacing diode-connected transistors with wide-swing current mirrors. Output driving can be increased by adopting larger (W/L) ratios in the push-pull stage without degrading bandwidth since its input capacitance composes the compensation capacitor. Although a 5V rail-to-rail supply was specified to accommodate high V_{TH} values, the present technique is compatible with lower voltages. The amplifier is suitable for many low-power control and low-frequency signal applications, such as battery-operated and remote systems.

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