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Oscillation Amplitude Analysis of MOS Hartley Oscillator Using a General Model

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ABSTRACT

New analytical equations for amplitude analysis of MOS Hartley oscillator are presented. Using exact large-signal circuit analysis, analytical equations for estimating the amplitude of Hartley oscillator are derived that considers all operation regions of transistor; including saturation, triode and cutoff. The analysis is based on a reasonable estimation for the output waveform. The estimated waveform should satisfy the nonlinear differential equations describing the circuit. Using this novel point, we can simply find the unknown parameters of the waveform, especially amplitude. The validity of the resulted equations is verified through simulations using TSMC 0.18 μm CMOS process. The amplitude calculated from this approach has a very good agreement with simulation for a large range of circuit parameters.

Index Terms: Oscillator, MOS Hartley oscillator, oscillation frequency, oscillation amplitude.

1. INTRODUCTION

LC oscillators, in the last two decades by the advent of monolithic inductors in MOS and bipolar technologies, are widely in use [7]. One of the LC oscillators is Hartley oscillator shown in Figure 1. This circuit is an important building block in variety of RF applications. Correct equations for frequency and amplitude of oscillation and phase noise are some designing challenges of LC oscillators as any other types of oscillators and VCOs. Variety of methods for finding transient or steady state behavior of these oscillators was presented [1], [5] and [7].

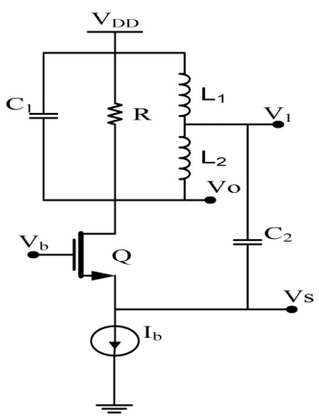


Figure 1. A typical MOS Hartley oscillator

The aim of this paper is to determine the steady state oscillation amplitude in MOS Hartley oscillator. Previous analyses [1], [6] assume that LC oscillators only meets saturation or saturation and cut-off regions during oscillation period and operation in triode region is ignored; however, the accuracy of their equations is limited only to this assumption. In this paper, we derived equations for amplitude of this oscillator without any restricting assumption. In our method by a reasonable assumption, we estimate the output voltage waveform as a parameterized sinusoidal waveform. Because of the inherent nonlinear behavior of MOS transistor [5], the differential equations describing the circuit are inherently nonlinear that should be satisfied by the estimated waveform. Using this point, equations for finding unknown parameters are derived. Although these equations are somewhat complicated but in comparison with simulation results, it will be shown that they are very accurate. In fact, the output voltage is not completely sinusoidal; but because of the filtering selectivity of the LC tank, this assumption is reasonable.

Section 2 describes our proposed analysis to derive equations for amplitude of oscillation. In section 3, a numerical example is presented for synthesizing a typical MOS Hartley oscillator and finally, we show the validity of our equations through simulations and compare them by some existing equations.

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2. THE PROPOSED METHOD

Hartley is a single transistor oscillator. In the beginning of oscillation, amplitude is very small and small signal condition for circuit is true and we can use linear model to achieve the condition needed for oscillation. To achieve oscillation, the circuit must satisfy Barkhausen's criteria: total phase shift in feedback loop must be 2π with a unity loop gain in oscillation frequency. To achieve 2π phase shift, the output (drain) signal is coupled by an inductive feedback to the source of transistor. Note that the circuit oscillates if the closed-loop transfer function goes to infinity at an imaginary value of S, $S=j\omega$. Consequently both the real and imaginary parts of denominator in transfer function must drop to zero at this frequency [8]. But after this behavior of circuit, the amplitude become larger and the circuit has large signal behavior. In designing of the oscillator, the designer mostly like to force the transistor to operate in class B or C in order to keep it off in most time of the oscillation period to decrease the phase noise that arises from the channel noise of the transistor. On the other hand, this research is dedicated to finding the equations for describing the circuit in all possible cases that gives a better insight to behavior modeling of these type oscillators.

A. General Procedure of the Proposed Method

Our method is a large signal analysis based on nonlinear differential equations that describe the circuit behavior. These equations can be simply obtained from circuit analysis methods. From this analysis, we can find analytical equations for output oscillation amplitude. This analysis involves all possible cases for operation region of MOS transistor. In general form, assuming that the drain current of transistor is $i_D(t)$ and writing *KCL* at nodes V_S, V_O and V_1, we get:

$$\begin{cases} \text{I}.C_1\dfrac{d^2Vo}{dt^2}+\dfrac{1}{R}\dfrac{dVo}{dt}+\dfrac{Vo-V_1}{l_2}+\dfrac{di_D(t)}{dt}=0 \\ \text{II}.\dfrac{Vo-V_1}{l_2}-\dfrac{V_1-V_{DD}}{l_1}-C_2\dfrac{d^2V_1}{dt^2}+C_2\dfrac{d^2Vs}{dt^2}=0 \\ \text{III}.C_2\dfrac{dV_1}{dt}-C_2\dfrac{dVs}{dt}+i_D(t)-I_b=0 \end{cases} \quad (1)$$

These equations describe the circuit behavior in a general case. As mentioned before, we can estimate V_O, V_S and V_1 as follows:

$$V_O(t)=V_{DD}+A\cos\omega t,\ V_S(t)=D+B\cos\omega t,\ V_1(t)=V_{DD}+B\cos\omega t \quad (2)$$

where ω is angular frequency and is equal to [1].

$$\omega=\frac{1}{\sqrt{C_1(l_1+l_2)}} \quad (3)$$

The procedure is to substituting equations of V_O, V_S and V_1 in differential equation of circuit (1) and calculating the unknown parameters *(A, B, D)*. Another assumption of this method is:

$$A=\frac{l_1+l_2}{l_1}B=\frac{1}{n}B \quad (4)$$

Note that validity of (2), (3), (4) are restricted to having high quality factor *(Q)* for the LC tank.

B. Analytical equations for the case that transistor meets only saturation region

Based on circuit parameter, we know that, transistor experiences different operation regions; here it has been supposed that the amplitude is small enough to keep the transistor only in saturation. We know that drain current of MOS transistor in saturation region can be expressed by square-law equation as follow:

$$I_D=\frac{K}{2}(V_{GS}-V_T)^2 \quad (5)$$

Now using this equation for i_D in (1) one will obtain the equations:

$$\begin{cases} \text{I}.C_1\dfrac{d^2Vo}{dt^2}+\dfrac{1}{R}\dfrac{dVo}{dt}+\dfrac{Vo-V_1}{l_2}-k\dfrac{dVs}{dt}(V_b-Vs-V_t)=0 \\ \text{II}.\dfrac{Vo-V_1}{l_2}-\dfrac{V_1-V_{DD}}{l_1}-C_2\dfrac{d^2V_1}{dt^2}+C_2\dfrac{d^2Vs}{dt^2}=0 \\ \text{III}.C_2\dfrac{dV_1}{dt}-C_2\dfrac{dVs}{dt}+\dfrac{k}{2}(V_b-Vs-V_t)^2-I_b=0 \end{cases} \quad (6)$$

Equation (6) describes the oscillator behavior in saturation region. As it can be seen, the equation (6) represents nonlinear differential equations describing the Hartley circuit. We know that the *DC* levels of V_O and V_1 are equal to V_{DD}. Also, because the transistor always operates in saturation region, the *DC* level of V_S can be simply computed from the following relation:

$$D=Vb-Vt-\sqrt{\frac{2I_b}{k}} \quad (7)$$

And we know that oscillation frequency can be expressed as equation (3). Using a bit mathematical calculations, equations (6) and (2) can be combined and reduced to (8).

$$\begin{cases} \text{I}.-C_1A\omega^2\cos\omega t-\dfrac{1}{R}A\omega\sin\omega t+\dfrac{A-B}{l_2}\cos\omega t+kB\omega\sin\omega t(V_b-V_t-D-B\cos\omega t)=0 \\ \text{II}.\dfrac{A-B}{l_2}\cos\omega t-\dfrac{B}{l_1}\cos\omega t-\dfrac{k}{2}(V_b-V_t-D-B\cos\omega t)^2+I_b=0 \end{cases} \quad (8)$$

First from (8.II), (7) A can be obtained in term of B as follows:

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$$A = \frac{B}{n} - l_2 k[-\sqrt{\frac{2I_b}{k}}B + \frac{B^2}{2}\cos\omega t] \quad (9)$$

In (9) the first term is equation (4) and other terms are negligible versus it. So by a good estimation we can say $A=B/n$, that confirms equation (4). Now substituting (9) in (8.I) and with simple mathematical calculations B can be written as:

$$\begin{aligned} &-C_1(\frac{1}{n} - l_2 k[-\sqrt{\frac{2I_b}{k}} + \frac{B}{2}\cos\omega t])\omega^2\cos\omega t - \frac{1}{R}(\frac{1}{n} - l_2 k[-\sqrt{\frac{2I_b}{k}} + \frac{B}{2}\cos\omega t])\omega\sin\omega t \\ &+\frac{(\frac{1}{n} - l_2 k[-\sqrt{\frac{2I_b}{k}} + \frac{B}{2}\cos\omega t]) - 1}{l_2}\cos\omega t + k\omega\sin\omega t(\sqrt{\frac{2I_b}{k}} - B\cos\omega t) = 0 \end{aligned} \quad (10)$$

Equation (10) holds for every time; for example when:

$$\begin{cases} \text{I.}\cos\ \omega t = 1\ ,\ \sin\ \omega t = 0 \\ \text{II.}\sin\ \omega t = 1\ ,\ \cos\ \omega t = 0 \end{cases} \quad (11)$$

Substituting $sin\ \omega t$ and $cos\ \omega t$ from (11) in (10) leaves beneficial equations of (12) from which B with some approximations can be calculated.

$$B = \frac{2k}{Rl_1[1 - C_1 l_2 \omega^2]} - \sqrt{\frac{2I_b}{k}} \quad (12)$$

Calculating B from (12) and knowing $A=B/n$, A will be calculated too. Therefore using equations (4) and (12), and using this point that in (12) the value of first term versus the value of second term is negligible. Therefore A approximately is

$$A \approx -\sqrt{\frac{2I_b}{n^2 k}} \quad (13)$$

Equation (13) represents oscillation amplitude at node V_O in terms of the circuit parameters. Note that the validity of this equation is restricted to the following two conditions:

- The transistors should not meet triode region that means: $A - V_{DD} < V_t - V_b$
- The transistors should not meet cutoff region that means: $-D - E \geq V_t - V_b$

C. Analytical equations for the case that transistor meets cutoff region too

In cases that the amplitude is large, the transistor may enter cutoff region too. Figure 2 shows a sample waveform of V_O when the transistor experiences both saturation and cutoff regions during oscillation period. This plot gives the evidence that the output voltage can be assumed as sinusoidal; therefore, we estimate output voltages as (2) again. But the DC level of V_S is not predictable as the former case and D should be calculated here using select the efficient points. The analysis is based on KCL at output nodes (1). Assuming the transistor in saturation region, with a bit mathematical calculations equation (1) will be reduced to (6) and assuming the transistor in cutoff region equation (1) leads to (14).

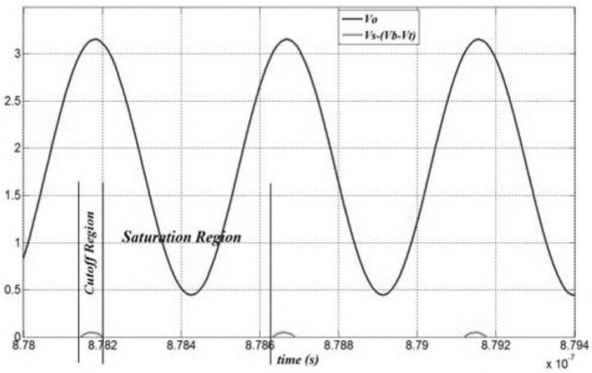


Figure 2. Output sample when transistor meets cutoff region during oscillation period.

$$\begin{cases} \text{I.}C_1\frac{d^2Vo}{dt^2} + \frac{1}{R}\frac{dVo}{dt} + \frac{Vo - V_1}{l_2} = 0 \\ \text{II.}\frac{Vo - V_1}{l_2} - \frac{V_1 - V_{DD}}{l_1} - C_2\frac{d^2V_1}{dt^2} + C_2\frac{d^2Vs}{dt^2} = 0 \\ \text{III.}C_2\frac{dV_1}{dt} - C_2\frac{dVs}{dt} - I_b = 0 \end{cases} \quad (14)$$

Substituting the estimated waveforms for V_O, V_S and V_1 in (14) for cutoff region equation (14), we have:

$$\begin{cases} \text{I.} - C_1 A\omega^2\cos\omega t - \frac{1}{R}A\omega\sin\omega t + \frac{A - B}{l_2}\cos\omega t = 0 \\ \text{II.}\frac{A - B}{l_2}\cos\omega t - \frac{B}{l_1}\cos\omega t + I_b = 0 \end{cases} \quad (15)$$

(15.II) can be rewritten as:

$$A = B + \frac{l_2 B}{l_1} - \frac{l_2 I_b}{\cos\ \omega t} \quad (16)$$

Using (16) and (15.I) we get:

$$B \approx \frac{Rl_1^2 I_b}{\omega\sin\omega t(l_1 + l_2)^2} \quad (17)$$

Now, using critical points will make the problem traceable. Assuming V_S as equation (2), the value of $cos\ \omega t$ for which the transistor is off region is equal to

$$\cos\omega t = \frac{V_b - V_t - D}{B} \quad (18)$$

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On the other hand, from Figure 2, we know if $\omega t=2n\pi$ then V_S meets its maximum value and the transistor will be exactly in cutoff region. Therefore, if $(V_b - V_t - D) / B < \cos \omega t < 1$ then the transistor will be exactly in cutoff region. One of these useful points occurs on average point between two limitations, when

$$\cos \omega t = \frac{B + V_b - V_t - D}{2B} = \cos \alpha \qquad (19)$$

And

$$\sqrt{1 - (\frac{B + V_b - V_t - D}{2B})^2} = \sin \alpha \qquad (20)$$

Substituting this value of *cos* ωt in (19) and value of *sin* ωt in (20) leads to following relation between B and D:

$$B \approx \frac{Rl_1^2 I_b}{\omega (l_1 + l_2)^2 \sqrt{1 - (\frac{B + V_b - V_t - D}{2B})^2}} \qquad (21)$$

Now, we know that transistor is in cutoff region and the time for this state is short therefore, Using Matlab we estimate the section radical of (21) with a line as

$$\sqrt{1-(\frac{B+V_b-V_t-D}{2B})^2} \approx -1.644(\frac{B+V_b-V_t-D}{2B})+1.882 \qquad (22)$$

when the transistor just remains in cutoff region. Substituting (22) in (21), the amplitude of source voltage, B, is calculated. Figure 2 shows that when $\omega t=(2n+1)\pi$, V_S reaches its minimum value, and in these points, the transistor is undoubtedly in saturation region. And we know that when transistor is in saturation region, D still consider by (7). Now with these two points and substituting the equation (22) in (8.III) and using (21), we get

$$B \approx \frac{0.9434\ Rl_1^2 I_b}{\omega (l_1 + l_2)^2} - 1.055 \sqrt{\frac{2I_b}{k}} \qquad (23)$$

Calculating A from (4):

$$A \approx \frac{0.9434\ Rl_1 I_b}{\omega (l_1 + l_2)} - 1.055 \sqrt{\frac{2I_b}{n^2 k}} \qquad (24)$$

Here, note that the validity of this equation is restricted to the following a condition too:

- The transistors should not meet triode region that means:

D. Analytical equations for the case that transistor meets triode region too

Most of the published methods for amplitude analysis in oscillators don't have accurate analyses for the case that transistor meets triode region during the oscillation period. Suppose that we choose V_{DD} and V_b values very close to each other in configuration of Figure 1. So, knowing that $A=B/n$ and choosing small values for n, we obtain the condition that oscillation amplitude at node V_S is small but oscillation amplitude at node V_O is so large. Figure 3 and Figure 4 show a sample waveform for this case. Here, the transistor will meet saturation and triode and cutoff regions during the oscillation period. In this method, with the same analysis, analytical equations for the case that the transistor meets triode region can be simply obtained. We know that drain current of MOS transistor in triode region can be expressed by this equation as follow:

$$i_D(t) = k[(V_{GS} - V_t)(V_{DS}) - \frac{(V_{DS})^2}{2}] \qquad (25)$$

The analysis proposed here is again based on the *KCL* equations at output and source nodes. These equations can be rewritten as:

$$\begin{cases} \text{I.} C_1 \frac{d^2Vo}{dt^2} + \frac{dVo}{dt}(\frac{1}{R} + kV_{od} - kVs) + \frac{Vo - V_1}{l_2} + k\frac{dVs}{dt}(2Vs - V_{od} - Vo) = 0 \\ \text{II.} \frac{Vo - V_1}{l_2} - \frac{V_1 - V_{DD}}{l_1} - C_2\frac{d^2V_1}{dt^2} + C_2\frac{d^2Vs}{dt^2} = 0 \\ \text{III.} C_2\frac{dV_1}{dt} - C_2\frac{dVs}{dt} + k[(V_b - V_t - Vs)(Vo - Vs) - \frac{(Vo-Vs)^2}{2}] - I_b = 0 \end{cases} \qquad (26)$$

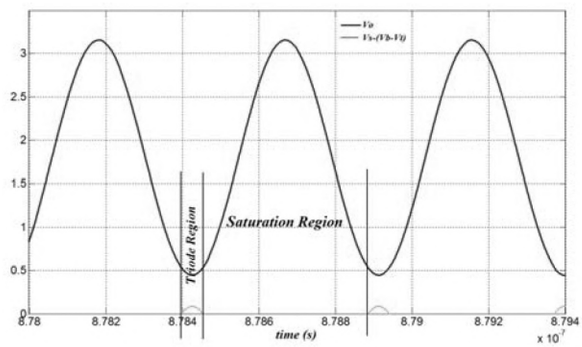


Figure 3. Output waveforms when transistor meet triode region during oscillation period.

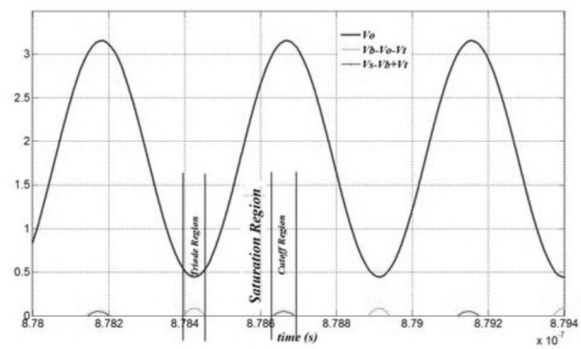


Figure 4. Sample output when the transistor meets all regions during oscillation period.

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Again, assuming the output voltages as sinusoidal waveforms makes the problem traceable. In this section, each transistor may meet the both triode and saturation regions during one period of oscillation. Now as the last cases, we use critical points for solving the problem. Choosing the points is based on knowledge about the times when transistor is exactly in triode or saturation region. For example, when $\omega t=2n\pi$, then V_O and V_S are maximum as shown in Figure 3 and the transistor is undoubtedly in saturation region. When $\omega t=(2n+1)\pi$, V_O and V_S have their minimum value and the transistor is exactly in triode region. On the other hand, by the assumption of sinusoidal waveforms for outputs, the boundary value of $\cos\ \omega t$ at which the transistor maybe enters the triode region is equal to:

$$\cos\ \omega t = \frac{V_b - V_t - V_{DD}}{A} \tag{27}$$

Therefore, if then the transistor will be in triode region. One of these useful points occurs when:

$$\cos\ \omega t = \frac{-A + V_b - V_t - V_{DD}}{2A} = \cos\theta \tag{28}$$

In this condition, transistor maybe is in all regions such as saturation and triode and cutoff regions. Again we consider D as equation (7). Therefore the equations in (26) for values of voltages in (2) are

$$\begin{cases} \text{I.} - C_1 A\omega^2 \cos\omega t - A\omega \sin\omega t\left(\frac{1}{R} + k\sqrt{\frac{2I_b}{k}}\right) + B\cos\omega t) + \frac{A-B}{l_2}\cos\omega t \\ - kB\omega \sin\omega t(2(Vb - Vt - \sqrt{\frac{2I_b}{k}}) + B\cos\omega t) - (V_b - V_t) - (V_{DD} + A\cos\omega t)) = 0 \\ \text{II.} \frac{A-B}{l_2}\cos\omega t - \frac{B}{l_1}\cos\omega t - k[(\sqrt{\frac{2I_b}{k}} + B\cos\omega t)((V_{DD} + A\cos\omega t) \\ - ((Vb - Vt - \sqrt{\frac{2I_b}{k}}) + B\cos\omega t))] + I_b = 0 \end{cases} \tag{29}$$

Again and using similar way, (29.II) can be rewritten as

$$A = \frac{B\cos\omega t[\frac{1}{l_2} + \frac{1}{l_1}] + k\sqrt{\frac{2I_b}{k}}V_{DD}B\cos\omega t - k\sqrt{\frac{2I_b}{k}}DB\cos\omega t - k\sqrt{\frac{2I_b}{k}}(B\cos\omega t)^2 - I_b}{[\frac{\cos\omega t}{l_2} - k\sqrt{\frac{2I_b}{k}}B(\cos\omega t)^2]} \tag{30}$$

First for use equation (30), we have to apply some approximation in it. And substituting equation (30) in (29.I), we have

$$B = \frac{[\frac{1}{Rn} + \sqrt{2kI_b}(2 - \frac{1}{n}) + k(V_{DD} - Vb + Vt)]}{\cos\ \omega t[\frac{1}{n} + k]} \tag{31}$$

Now using value of $\cos\omega t$ in (28) so the resulted equations for these assumptions are written as (32).

$$B = \frac{[\frac{1}{Rn} + \sqrt{2kI_b}(2 - \frac{1}{n}) + k(V_{DD} - Vb + Vt)]}{-\frac{1}{2n}[1 + nk]} + \frac{(V_b - V_t - V_{DD})}{2} \tag{32}$$

And then using B and (4) A can be derivate.

$$A = \frac{[\frac{1}{Rn} + \sqrt{2kI_b}(2 - \frac{1}{n}) + k(V_{DD} - Vb + Vt)]}{-\frac{1}{2}[1 + nk]} + \frac{(V_b - V_t - V_{DD})}{2n} \tag{33}$$

Equation (33) represents oscillation amplitude at node V_O in terms of the circuit parameters when the transistor meets all of operation regions. So this equation of oscillation amplitude is considered for Hartley oscillator in general state.

3. SIMULATION VERSUS ANALYTICAL RESULTS

New analytical equations for amplitude analysis of MOS Hartley oscillator were presented which are based on nonlinear differential equations of circuit. The analysis is general that involves MOS operation in all of the saturation, cutoff and triode regions. Above equations can be applied for synthesis of MOS Hartley oscillator in different ways. Suppose an oscillator with output voltage of 1.8V has to be designed with $\mu_n C_{ox}=275.6 \times 10^{-5}(A/V^2)$, $V_t=0.47(V)$ and $V_{DD}=1.8(V)$ where $L_1=6.5(nH)$, $L_2=5.5(nH)$, $R=6(k\Omega)$, $C_1=C_2=0.5(pf)$ and $I_b=200(\mu A)$. For this output voltage, the transistor operates in all off the saturation, cutoff and triode regions; furthermore, we know $n=0.542$ and then $B=0.542A$; therefore A can be calculated from (32) as follows:

$$A = \frac{[\frac{1}{6^4 \times 0.542} + \sqrt{2\times 2756\times 10^{-5}\times 0.2\times 10^{-3}}(2 - \frac{1}{0.542}) + 2756\times 10^{-5}(1.8 - 1 + 0.47)]}{-\frac{1}{2}[1 + 0.542\times 2756\times 10^{-5}]} + \frac{(1 - 0.47 - 1.8)}{2\times 0.542} \tag{34}$$

With this value for A, simulation shows *-1.171V* for output oscillation magnitude. As we can see, these equations have a good agreement with simulation and can be used for synthesis and hand analysis of MOS Hartley oscillator.

For validating our proposed equations and comparing them with competitive methods, some simulations and experiments are performed using Advanced Design System simulator (ADS). The TSMC 0.18µm CMOS process has been used in these simulations. Table.I gives the details of technology such as supply voltage, threshold voltage and other features of the transistor that is used in circuit.

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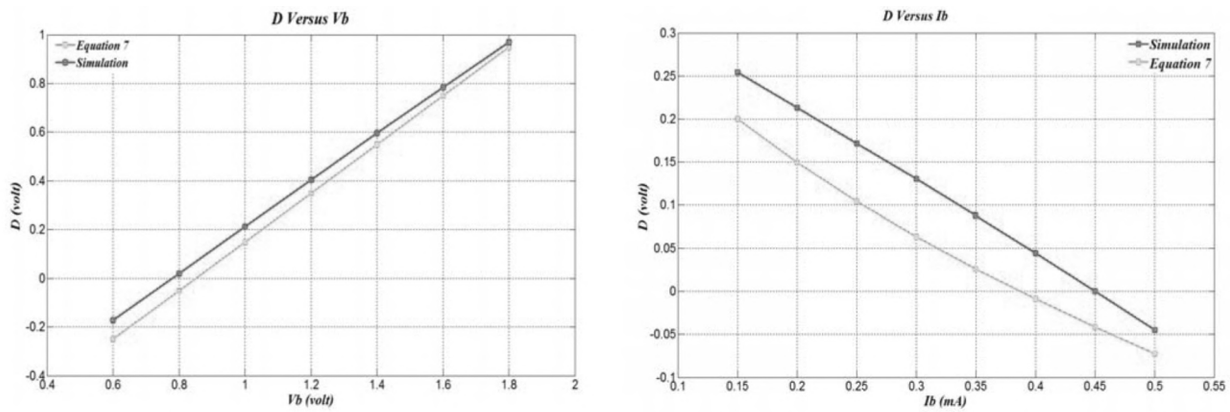
Table I. Details of Technology

	TSMC 0.18 µm
Supply Voltage	1.8 (V)
$\mu_n \cdot C_{ox}$	275.6e-6 (A/V^2)
Vtn (threshold NMOS)	0.47 (V)
Vtp (threshold PMOS)	-0.46 (V)
Transistor size (W/L)	10

First, a typical Hartley oscillator that was designed for the operation of transistor only in saturation region during oscillation period is presented. In each condition, one parameter of circuit is swept whereas other parameters are kept constant. The calculated amplitude by the proposed equation (13) is compared with the simulation results. Figure 5 shows the comparison between simulation and the results of *DC* level of source voltage *D*, from our analytical equations for the case that the transistor is only in saturation region during its oscillation period. In Figure (5.a) comparison is between 0.6(V) to 1.8(V) for V_b because the process is 0.18µm and the supply voltage can't become larger than 1.8(V) and the transistor need at least 0.6(V) for it will be on. As we can see in this figure, the results of equation (7) have a very good agreement with simulation especially for larger voltages. In Figure (5.b) simulation and comparison are between 0.15(mA) to 0.5(mA) for I_b. As shown in this figure, the equation (7) for larger current has more accurate results.

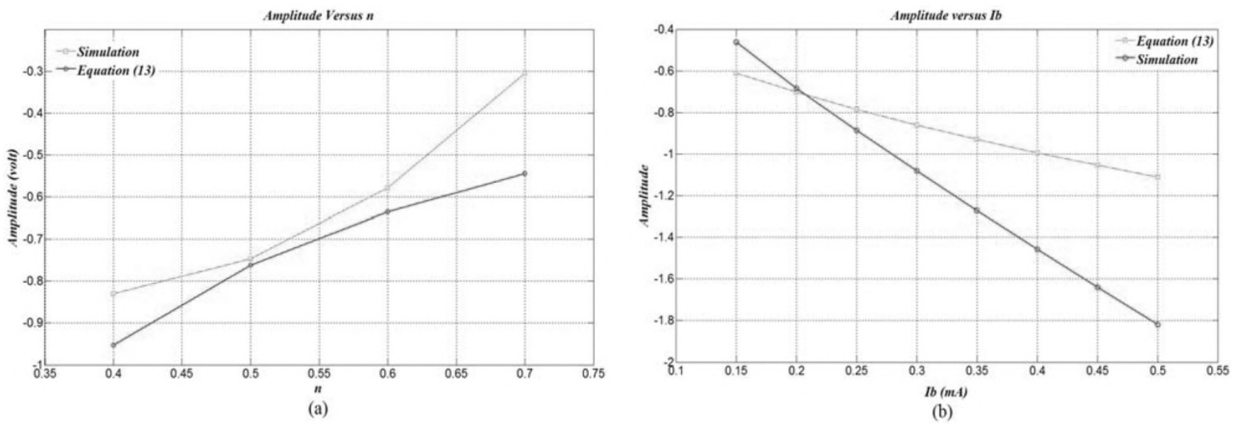
As the last step, the circuit is simulated under different conditions and parameters and comparisons between simulation results and amplitude obtained from the proposed method are illustrated in Figure 6, Figure 7 and Figure 8.

These simulations are repeated for the cases that the transistor changes the operation region during oscillation period. For example, Figure 6 shows the comparison between simulation and the results from our analytical equations for the case that the transistor is only in saturation region during its oscillation period. Using Figure 6, we can select the best value of *n* and hence l_1 and l_2 and also select best bias current I_b for better agreement with simulation. In this case, the transistor only is in saturation region. For example for *n=0.5* we have good correspondence with simulation. Figure 7 shows the comparison



(a) (b)

Figure 5. DC value of V_s as a function of (a) Bias voltage V_b (b) Bias current I_b.



(a) (b)

Figure 6. Comparison of simulation and analysis results when transistor meets only saturation region during oscillation period. (a) Amplitude versus n. (b) Amplitude versus I_b.

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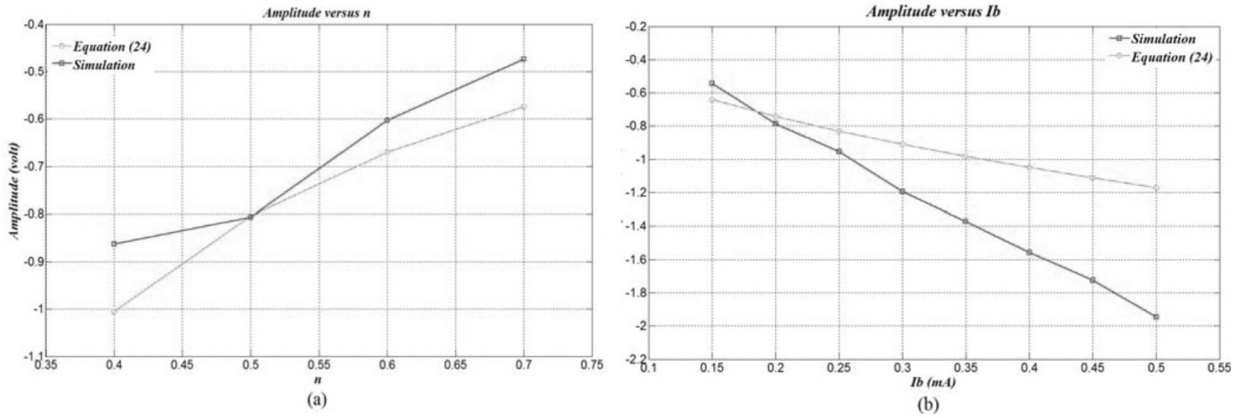


Figure 7. Comparison of simulation and analysis results when transistor changes its operation region between saturation and cutoff during oscillation period. (a) Amplitude versus n. (b) Amplitude versus I_b.

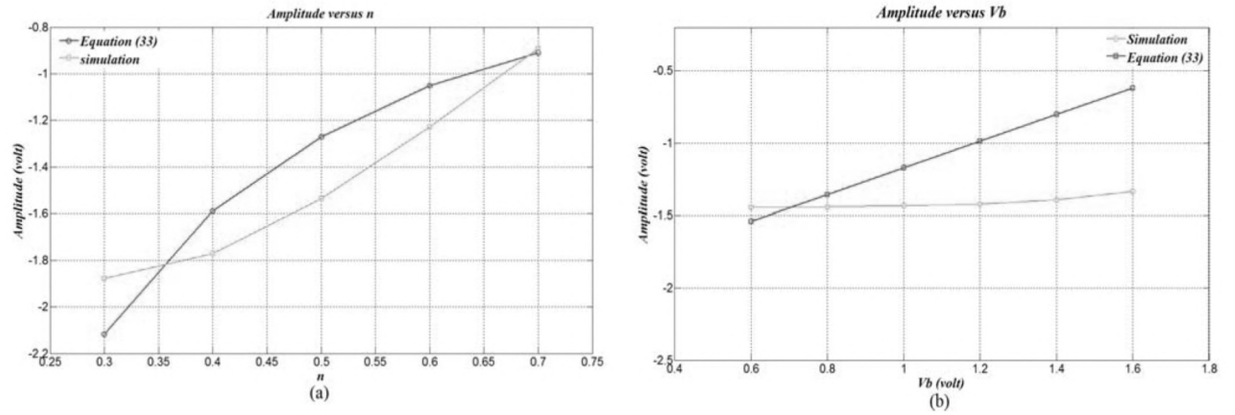


Figure 8. Comparison of simulation and analysis results when transistor changes its operation region between saturation, triode and cutoff during the oscillation period. (a) Amplitude versus n. (b) Amplitude versus V_b.

between simulation and the results from our analytical equations for the case that the transistor changes its operation region between saturation and cutoff regions during a period of oscillation. Using Figure 7, also we can select the best value of *n* and we can select best bias current I_b. In comparison with Figure 6 in this case, the transistor is in saturation and cutoff regions. Again, as shown in Figure 7, for *n=0.5* we have better correspondence with simulation. Therefore we can select the value of *n* close to the 0.5. These two figures give a good insight about *n* and current bias I_b to design a Hartley oscillator in large and small signal analysis.

At last, Figure 8 shows the comparison between simulations and results from our analysis for the case that the transistor operation region changes between saturation, triode and cutoff during oscillation period. It can be performed by choosing large values for n, I_b and V_b to increase oscillation amplitude at nodes V_O and V_S. In comparison with Figure 6 and Figure 7, in this case, the transistor is in all three regions. These figures give an accurate insight about oscillation amplitude in Hartley oscillator and about changing it as a function of circuit parameters in all states of transistor. In our simulations, it was not possible to compare our method and other proposed methods, because they have not exact equations for the case that the transistor meets triode region during oscillation period and there are not any analytical method for analysis amplitude oscillation in Hartley oscillator.

4. CONCLUSION

The Hartley oscillator has been analyzed in a general form in which the operating region of MOS transistor may be the saturation, cutoff and triode regions whereas previous analyses are limited only to transistor operating in saturation and cutoff regions. An analytical method to derive exact analytical equations for the amplitude of Hartley oscillators has presented. The output signal is assumed a sinusoidal waveform where the unknowns are amplitude and dc level. Applying the large signal analysis, the equations derived in this paper represent amplitude accurately.

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Nonlinear behavior of an oscillator can be explained easily with the presented equations. Also, the equations are provided for all operation regions of transistors but the effect of channel length modulation and more parasitic element are challenging points that limits the analysis. These equations will be of significant to be used in guiding LC oscillator design. As it can be seen, the results from our proposed equations have good agreement with simulation results and they can be used for design and analysis of RF MOS Hartley oscillator and an example illustrating this application was presented.

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