A High-Efficiency CMOS Rectifier for RF Using Bulk Biasing Control Circuit

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***Abstract*— In MOSFET-transistor based rectifier circuits, leakage currents occur through both source-bulk and drain-bulk connections of their transistors causing some power dissipation decreasing their efficiency. Such a scenario is more worrying in ultra-low power circuits as those used in energy harvesting. As a solution, in this work it is proposed a control circuit of transistor bulk biasing that switches the bulk bias in an efficient way assuring adequate inversion of the source-bulk and drain-bulk junctions. The rectifier based on the proposed bulk biasing control circuit shows to be a high-efficiency one capable of reducing the leakage currents. To obtain experimental results, the circuit was fabricated in a 130 nm CMOS process and tested on a micromanipulator. The results were compared with other works where it is observed that the efficiency of our proposal reaches up to 72.5% or 5% higher that the best previous one.**

***Index Terms*— CMOS rectifier; bulk biasing; power conversion efficiency.**

I. INTRODUCTION

Ultra-low power CMOS rectifiers are applied to RFID [1], energy harvesting systems, biomedical instrumentation [2][3], or any electronic device that energy consumption is critical. In general, researching of CMOS rectifier topologies aims to reduce voltage drop of the constituent transistors and to improve the power conversion efficiency (PCE) [4-7]

Some topologies of rectifier are based on: (I) V_t cancellation techniques [1][7]; (II) circuits with active-diode using operational amplifiers [6][10]; (III) bridgeless AC-DC converters [6]; (IV) conventional AC-DC rectifier using transistors instead of diodes [9][10].

In rectifier topologies based on V_t cancellation technique, it is aimed to decrease the voltage drop through the rectifier to obtain larger output voltage levels across the load [1][7]. However, these techniques reduce the PCE of the rectifier, since the involved leakage currents are increased due to the transistors operate near the linear region when they are in cut-off state. Rectifiers with active-diode based on operational amplifiers [4][8] increase the energy consumption since the operational amplifiers needs to be powered with some external power supply, which is not feasible for energy harvesting, for example. Bridgeless AC-DC converters [6] use inductors that show to increase energy consumption decreasing PCE.

In the conventional CMOS rectifier, for instance the diode bridge full-wave one [9], the voltage levels applied to the source and drain terminals of the CMOS transistors are clearly not continuous and, consequently, a positive potential difference appear across the drain-bulk junction and across source-bulk junction causing leakage current through the respective bulk due to the appearance of parasitic diodes.

In order to reduce or eliminate such leakage currents, it is shown some half-wave rectifiers in [11] and [12] that uses a scheme of switching the bulk terminals of the diode-connected transistors in order to reduce the threshold voltage and the leakage current. In [11], as the bulk terminals are connected directly to terminals of the alternating power supply, the bulk biasing voltage is not constant allowing conduction through the drain-bulk or source-bulk junctions decreasing the achieved PCE. In [12] the bulk biasing is carried out by an external power supply provided by a microprobe that is unviable where such a power supply is not possible in practice. In [13], four additional transistors are used to bias the bulk of the bridged p-type transistors of a conventional full-wave rectifier to eliminate leakage currents (for the n-type transistors, there is no bulk biasing). However, those additional transistors degrade the efficiency of the rectifier because they generate even more leakage currents. In [14] the bulk biasing technique is applied in a charge-pump based DC-DC converter that requires an external clock generator for bulk biasing making it unfeasible for energy harvesting.

As an alternative to overcome these drawbacks, in this work it is introduced a high efficiency low-power full-wave CMOS bridge rectifier using a proposed bulk biasing control circuit (BBCC) that avoids the appearance of parasitic diodes and consequently leakage currents. The proposed BBCC is composed of only four additional transistors arranged in a simple and innovative way and the BBCC-based rectifier shows to achieve a high PCE. The BBCC does not use neither operational amplifier nor V_t cancellation techniques and, unlike the schemes of [11-14] its additional transistors provide a continuous bulk voltage for self-biasing the n-type and p-type transistors of the bridge, avoiding appearance of parasitic diodes in the drain-bulk and source- bulk junctions. Plus, the proposed circuit does not depend on any external power supply for bulk biasing, operating exclusively with the input alternate voltage.

An integrated BBCC-based rectifier circuit was fabricated with a 130 nm CMOS process with its components fully integrated. Experimental results were obtained using a test bench containing a RF generator, a micromanipulator with microprobes and an oscilloscope. Additionally, post-layout

simulations were performed in Virtuoso/Cadence software and its results were compared with the experimental ones. Finally, an experimental comparative study with other circuits was carried out to demonstrate the efficiency of our proposition.

II. Conventional Rectifier

The proposed BBCC-based rectifier circuit is based on a conventional full-wave CMOS rectifier, shown in Fig. 1, which consists of two p-type transistors, T_{P0} and T_{P1}, and two n-type transistors, T_{N0} e T_{N1}. In this circuit, when $V_A > 0$ and $V_C < 0$, T_{P0} and T_{N1} are conducting (ON) while T_{P1} and T_{N0} are cut-off (OFF), interconnecting the load R_L to V_{in} through T_{N1} and T_{P0}. Similarly, when $V_A < 0$ and $V_C > 0$, T_{N1} and T_{P0} are OFF while T_{P1} and T_{N0} are ON, and R_L is interconnected to V_{in} through T_{P1} and T_{N0}. As in all situations the higher potential is interconnected to the load, the voltage across R_L in relation to ground is always positive [1].

It is important to observe that the bulk biasing of the transistors in ON state should be in such a way that the *pn* junctions between source-bulk and drain-bulk of the transistors must be reversed. This biasing prevents leakage current, and transistor body-effect take places.

In order that the threshold voltage has not large variations, the bulk (B) is connected to the source (S) terminal, (V_{SB}=0), as shown in Fig. 1. On the other hand, when $V_{SB} = 0$, the drain-bulk voltage $V_{DB} > 0$ and parasite diode and leakage current appear. Therefore, in a rectifier circuit it is important to ensure that the both source-bulk and drain-bulk junctions are always reverse preventing leakage current and unneeded power dissipation. For example, when the drain voltage (V_D) of T_{P0} in Fig. 1, is equal to V_A and its bulk voltage V_B is equal to V_{out}, V_D is greater than V_B and leakage current appears as can be seen in the simulation results shown in Fig. 2 (red circle at p-type conduction). Similarly, for T_{N0}, V_D is less than V_B and leakage current appears as can be seen in Fig. 2 (black circle at n-type conduction). Then, leakage currents exist in drain-bulk junctions for all transistors of the rectifier shown in Fig. 1.

To compute the drain current i_d of T_{P0}, for example, when V_B is equal to V_{out}, $V_{out} = V_p - V_d - V_r/2$; where V_p is the peak value of the input voltage V_{in}; V_d is the voltage drop across the transistor; V_r is the ripple voltage depending

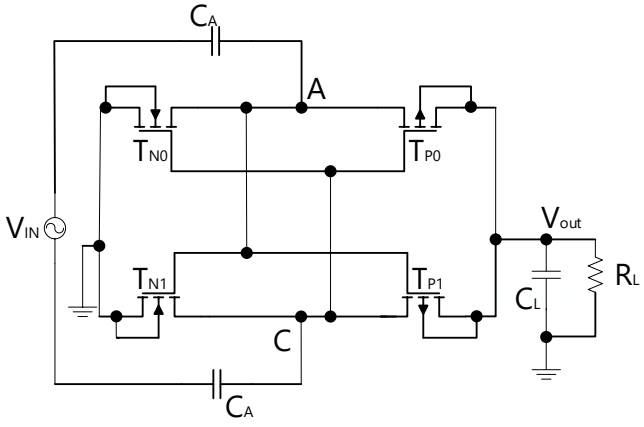

Fig. 1. Conventional Full-Wave CMOS rectifier.

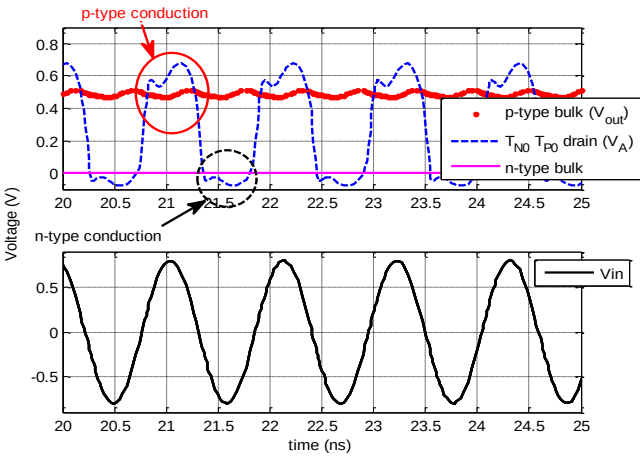

Fig. 2. Conduction of the drain-bulk junctions of the conventional Full-Wave CMOS rectifier.

on the capacitor C_L.

Then, $V_{DB} > 0$, because $V_D = V_A$ and $V_B < V_A$. Therefore, i_d can be expressed as (1) the sum of the current in the triode region and the current in the drain-bulk junction according to [15][16]:

$$i_d = \mu_p C_{ox} \frac{W_p}{L_p}\left[(v_{GS} - V_t)(v_{DS}) - \frac{1}{2}(v_{DS})^2\right] + I_S\left(e^{v_{DB}/nV_T} - 1\right), \quad (1)$$

where W_p/L_p represents the aspect ratio of the p-type transistor; $\mu_p C_{ox}$ the transconductance parameter; V_t the threshold voltage; I_S the saturation current of the drain-bulk junction diode; n the ideality factor; V_T the thermal voltage.

In Fig. 1, when $V_A > 0$ and $V_C < 0$, T_{P0} and T_{N1} are ON while T_{P1} and T_{N0} are cut-off, thus the circuit current I_C can be computed based on (1) considering $v_{DS} = V_{out} - V_A$ and $v_{GS} = V_C - V_A$. Then, replacing v_{DS} and v_{GS} in (1) and let $I_K = I_S\left(e^{V_{DB}/nV_T} - 1\right)$ be the leakage current, it is obtained:

$$I_C = \mu_p C_{ox} \frac{W_p}{L_p} \ldots \left[(V_C - V_A - V_t)(V_{out} - V_A) - \frac{1}{2}(V_{out} - V_A)^2\right] + I_K \quad (2)$$

and V_{out} in (2), according to [15][16], can be expressed as:

$$V_{out} = (V_p - V_d)\left(1 - \frac{1}{4fC_L(R_L + r_{DS})}\right), \quad (3)$$

because $V_r = (V_p - V_d)/2fRC_L$, where $R = R_L + r_{DS}$, load and T_{N1} transistor resistance. Thus replacing V_r in V_{out} it is obtained (3). r_{DS} is given by, according to [15][16]:

$$r_{DS} = \frac{v_{DS}}{i_D} = \frac{v_{DS}}{\mu_n C_{ox} \frac{W_n}{L_n}\left[(v_{GS} - V_t)(v_{DS}) - \frac{1}{2}(v_{DS})^2\right]}, \quad (4)$$

where W_n/L_n represents the aspect ratio of the n-type transistor. Considering $v_{DS} = -V_C$ and $v_{GS} = V_A - V_C$, and replacing v_{DS} and v_{GS} in (4), r_{DS} can be rewritten as follows:

$$r_{DS} = \frac{-2L_n V_C}{\mu_n C_{ox} W_n \left[-2(V_A - V_C - V_t)V_C - {V_C}^2\right] + 2L_n}. \quad (5)$$

Thus replacing (5) in (3),

$$V_{out} = (V_p - V_d)\left(1 - \frac{1}{4fR_L C_L} + \frac{B + 2L_n}{-8L_n V_C fC_L}\right), \quad (6)$$

where: $B = \mu_n C_{ox} W_n \left[-2(V_A - V_C - V_t)V_C - {V_C}^2\right]$. Therefore, the circuit current I_C in (2) can be given by, replacing (6) in (2):

$$I_C = \mu_p C_{ox} \frac{W_p}{L_p}\Big[(V_C - V_A - V_t)\ldots$$
$$\ldots\left((V_p - V_d)\left(1 - \frac{1}{4fR_L C_L} + \frac{B + 2L_n}{-8L_n V_C fC_L}\right) - V_A\right)\ldots$$
$$\ldots - \frac{1}{2}\left((V_p - V_d)\left(1 - \frac{1}{4fR_L C_L} + \frac{B + 2L_n}{-8L_n V_C fC_L}\right) - V_A\right)^2\Big] + I_K$$

or

$$I_C = I_C^0 + I_K \quad (7)$$

In the circuit shown in Fig. 1, the PCE can be written using:

$$PCE = \frac{P_L}{P_{in}} = \frac{V_{out}^2 / R_L}{V_{in}(I_C^0 + I_K)} \cdot 100 \quad (8)$$

where P_L is the output power consumed by R_L and P_{in} is the input power delivered by the source. Other leakage currents are not considered because they are negligible.

Take in consideration (8), the greater, I_K the lesser PCE. In the next section a proposed solution to decrease I_K is introduced.

III. Proposed Rectifier

To reduce the current through the convectional CMOS full-wave rectifier transistor's drain-bulk junctions and increase the PCE, a bulk biasing control circuit (BBCC) is introduced and shown in Fig. 3. The BBCC is based on techniques of bulk biasing, which is a well-known one, but never applied in CMOS full-wave rectifier to the best of our knowledge.

The BBCC, as shown in Fig. 3, operates as follows. In the positive half of the cycle of V_{in} (point A is positive with respect to point C), when $V_A > 0$ and $V_C < 0$, T_{N1} and T_{P0} are conducting and T_{N0} and T_{P1} are cut-off (OFF), interconnecting V_{in} to R_L through T_{N1} and T_{P0}. Under these conditions, T_{P2} and T_{P3}, are conducting ($v_{GS} < V_t$) connecting V_A to the bulk of T_{P0} and T_{P1} (see the red line at Fig. 4(a)) and connecting the voltage source's negative voltage, V_C, to the bulk terminals of T_{N0} and T_{N1} (see the purple line at Fig. 4(a)). T_{N2} and T_{N3} (see the gray line at Fig. 4(a)) are cut-off ($v_{GS} < V_t$). As the BBCC's transistors were designed with ultra-low threshold voltage 100 mV, their conduction state and voltage drop occur at low voltage level and, the most important, the BBCC switching ensure that both source-bulk and drain-bulk junctions are always reverse preventing leakage current and unneeded power dissipation.

In a similar way, in the negative half of the cycle of V_{in} (point A is negative with respect to point C), when $V_A < 0$ and $V_C > 0$, T_{P0}, T_{N1}, are cut-off while T_{P1}, T_{N0}, are conducting, and R_L is interconnected to V_{in} through T_{P1} and T_{N0}. Under these conditions, T_{N2} and T_{N3}, are conducting connecting V_C to the bulk of T_{P0} and T_{P1} (see the red line at Fig. 4(b)) and connecting V_A to the bulk of T_{N0} and T_{N1} (see the purple line at Fig. 4(b)). T_{P2} and T_{P3}, (see the gray line at Fig. 4(b)) are cut-off ($v_{GS} > V_t$).

In a general way, the BBCC maintain the drain-bulk junctions of T_{N0}, T_{N1}, T_{P0} and T_{P1} reversed biased throughout the positive and negative cycle of V_{in}, taking V_{DB} close to zero reducing the junction leakage currents of the transistors and the channel effects related to bulk biasing, because the drain and bulk potential are about the same when T_{N0}, T_{N1}, T_{P0} and T_{P1}. To achieve this, the BBCC switches the bulk of the n-type transistors to the lowest potential (either V_A or V_C) and switches the bulk of the p-type transistors to the highest potential (either V_A or V_C) accordingly to the voltage polarity of V_{in} (positive or negative). Additionally, as the transistor currents decrease, the on-resistance of them does not increase contributing to better the efficiency.

A way to prove that the reduction of leakage currents decreases the power dissipation in T_{N0}, T_{N1}, T_{P0} and T_{P1} and increases the rectifier PCE is shown in Fig. 5, which shows the simulation results of the dissipated power by T_{P0}, for example, in the conventional rectifier (line —◆—) and in

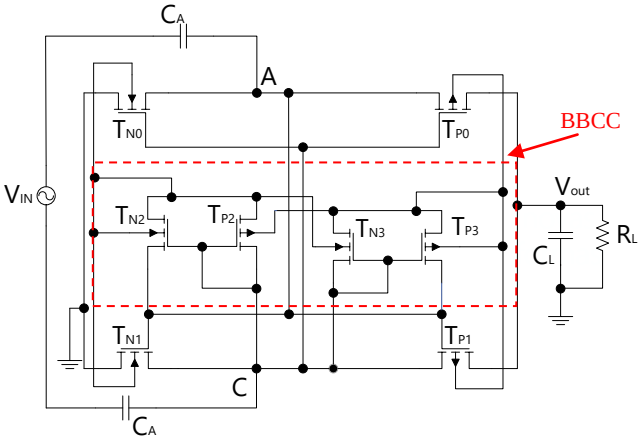

Fig. 3. BBCC-based Rectifier.

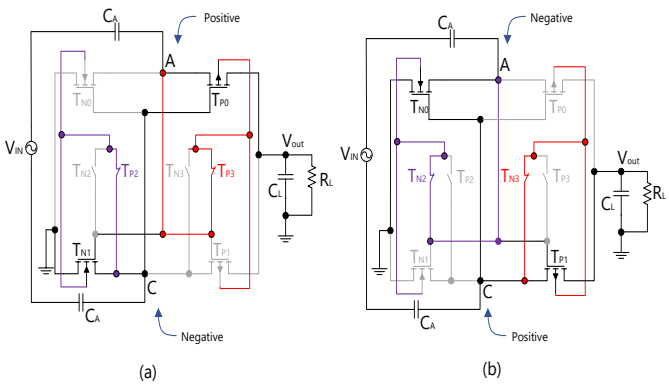

Fig. 4. V_{in} cycles: (a) Positive cycle (b) Negative cycle.

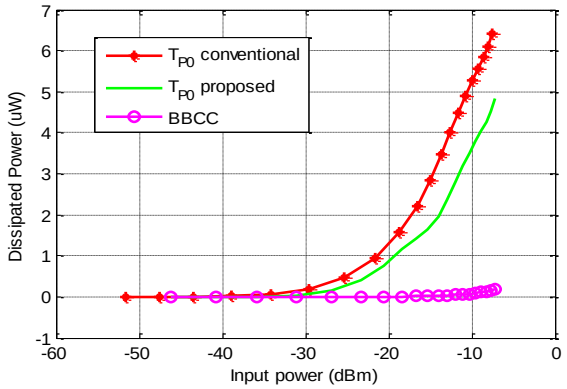

Fig. 5. Output DC voltage and PCE as a function of R_L.

the BBCC-based rectifier (line ——). For a range of input power, the dissipated power of BBCC-based rectifier's T_{P0} is always lower than that dissipated by T_{P0} in the conventional rectifier. The same result happens for T_{N0}, T_{P1} and T_{N1}. Fig. 5 also shows the dissipated power of the entire BBCC block (line —o—) that is very small, almost negligible, because either T_{N2} and T_{P2} or T_{N3} and T_{P3} are never shorted on the same time.

It is important to highlight that during the periods, called here dead zone as shown in Fig. 6, that the transistor switching occurs ($V_{in} \approx 0$), that is, the periods from T_{N2} stops conducting to T_{P2} begins conducting and vice-versa (or similarly from T_{N3} stops conducting to T_{P3} begins conducting and vice-versa), T_{N2} and T_{P2} (or T_{N3} and T_{P3}) do not conduct (no short-circuited) simultaneously avoiding short-circuiting and consequently power dissipation peaks.

Fig. 7 shows the bulk biasing voltage through several V_{in} cycles that, as expected, the n-type transistors' bulk voltage is negative and the p-type transistors' bulk voltage is positive demonstrating that their bulk junctions are reversed. An explanation for this is that, considering T_{P0} for example and when $V_A > 0$ and $V_C < 0$, $V_B = V_A - V_Q$, where V_Q is the voltage drop across the respective conducting transistors in the BBCC. It is possible to see in Fig. 7 that the blue curve crosses up the red one (at top) and down the purple one (at bottom), but there is no conduction in these situations as the concerned potential differences do not overcoming the *pn* barrier potential. As $V_Q \ll V_A$ then $V_B \approx V_A$ and thus $V_{DB} \approx 0$, because $V_B \approx V_D = V_A$. Since $V_{DB} \approx 0$, the term I_K of (7) is approximately zero. For $V_A < 0$ and $V_C > 0$, I_C is similar.

Consequently, (7) can be rewritten as:

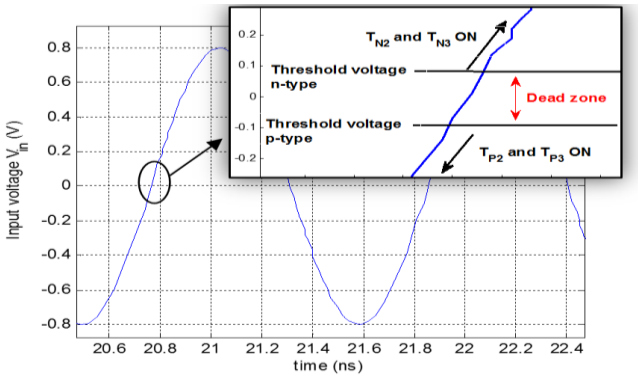

Fig. 6. Dead zone of the BBCC block transistors.

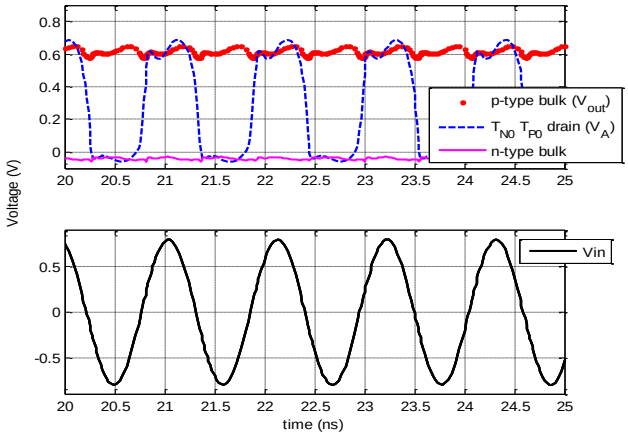

Fig. 7. Bulk biasing voltage through several V_{in} cycles to n-type and p-type transistors.

$$I_C \cong I_C^0 \tag{9}$$

In this way, PCE for the proposed BBCC-based rectifier is given by $PCE = \frac{V_{out}^2 / R_L}{V_{in} I_C^0} \cdot 100$ that prove to be higher than conventional rectifier given by (8).

IV. Results and Discussion

Simulation results of the proposed BBCC-based rectifier were obtained by modeling and simulation analysis using Virtuoso/CADENCE with 130 nm CMOS process. An integrated circuit was fabricated and experimental results were also obtained. The integrated circuit parameters were: L = 180 nm for all transistors; W = 10 µm for T_{N0} and T_{N1}, W = 18 µm for T_{P0} and T_{P1}, W = 600 nm for T_{N2}, T_{N3}, T_{P3} and T_{P2}; C_A = 10 pF and C_L = 1 pF. The test frequency was 915 MHz since it is an unlicensed frequency for ISM commonly used in other works.

Fig. 8 shows a comparative chart with the achieved PCE of the conventional rectifier and the BBCC-based rectifier for different input power for R_L = 2 kΩ, in which is possible to observe the greater PCE of BBCC-based rectifier. Also, as shown in Fig. 8, the rectified DC output voltage is slightly greater as well.

In order to achieve the value of R_L that achieve the highest PCE (efficiency), Fig. 9 shows the values of PCE for different values of R_L and the best R_L = 2 kΩ.

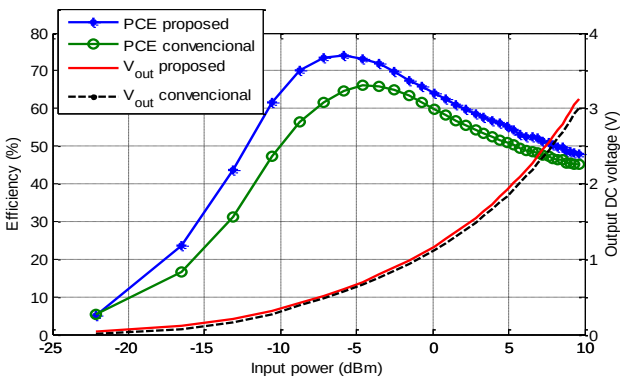

Fig. 8. Comparative results with the achieved PCE of the conventional rectifier and the BBCC-based rectifier for different input power for R_L = 2 kΩ.

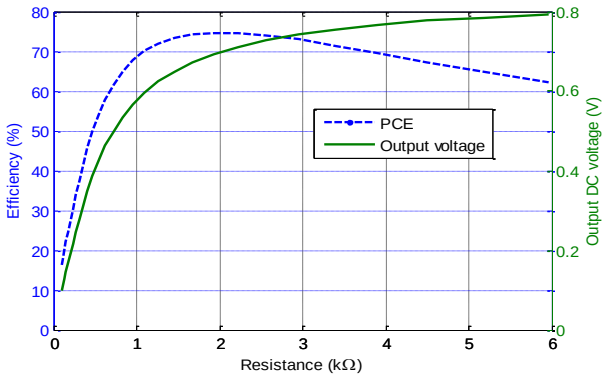

Fig. 9. Output DC voltage and PCE as a function of R_L.

In order to achieve the value of R_L that achieve the highest PCE (efficiency), Fig. 8 shows the values of PCE for different values of R_L and the best R_L = 2 kΩ.

Experimental results were obtained using a test bench containing a microprobe manipulator, an RF signal generator and an oscilloscope. The entire test bench is suspended in an aluminum cage fully grounded.

Fig. 10 shows a photomicrograph of the fabricated rectifier.

Fig. 11 shows the comparison between the simulation and experimental results of the output DC voltage and PCE as a function of input power. The best result is 72.5% for -7 dBm.

As shown in Fig. 11, the simulation and experimental results of the proposed rectifier are very close, mainly after -10 dBm of input power, demonstrating that the circuit has a good efficiency for energy harvesting applications. There is a small difference between the simulation and experimental results for values below -10 dBm due to imperfections of the manufacturing process increasing the threshold voltage and delaying the conduction of the transistors. For values below -15 dBm, the input power is insufficient for biasing the transistors and the circuit is operational.

Some novelties have been proposed in this work, as for example: (1) no change on topology in the rectifier bridge, only new interconnections are made from the bulk of the rectifier bridge transistors to BBCC; (2) the BBCC-based rectifier does not use any external power supply for its operation, depending exclusively on the voltage input power supply V_{in}; (3) the BBCC provides a constant voltage for all bulk of the rectifier bridge transistors regardless of the polarity of V_{in}; and, as its main goal, (4) the BBCC decreases drastically the leakage currents through bulk-drain and

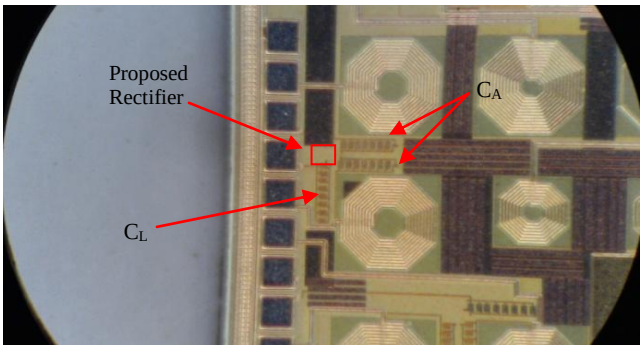

Fig. 10. Photomicrograph of the fabricated rectifier.

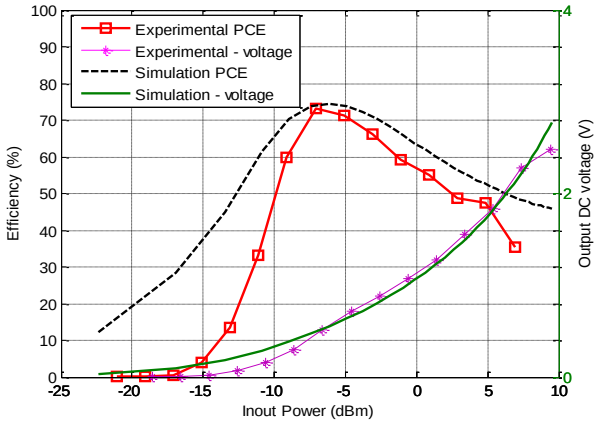

Fig. 11. Simulation and experimental results of output DC voltages and PCE as a function of input power.

bulk-source junctions of the rectifier bridge transistors and increase its PCE. The performance summary and comparison with previous work are shown in Table 1. It is important to observe that the rectifier topologies of [9] and [18] work from -12 dBm and -11 dBm of input power, respectively, that are lesser than the proposed BBCC-based rectifier, but their load must be greater than 10 kΩ and 68 kΩ, respectively. In [9], a 100-mV output voltage has been obtained at a cost of a poor PCE of 5%. For its turn, the proposed circuit in [11] works from input power greater than -6dBm and load value lesser than that achieved in [9] and [18], but its obtained PCE is just 11%, that is, 61.5% lesser the proposed BBCC-based rectifier.

In [1] an output voltage of 1.5 V was obtained, but voltage boost circuit is needed. [17] and [18] did not specify (*) the output voltage. We conclude that, even needing input power greater than -7 dBm, the proposed BBCC-based rectifier achieves the best PCE, 72.5%, even using a few more transistors, but considering a 2 kΩ-load.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK.

Ref.	Technology (nm)	Input Power (dBm)	Frequency (Hz)	Load (kΩ)	PCE (%)	V_{out} (mV)
[1]	300	-6	950 M	3.7	11.0	1500
[9]	180	-12	953 M	10	67.5	600
[17]	350	-6	953 M	14.2	36.6	*
[18]	90	-11	13.56 M	68	45.0	*
This work	130	-7	915 M	2	72.5	500

V. CONCLUSION

A bulk biasing control circuit, called BBCC, for high-efficiency CMOS bridge rectifier was proposed and shown to be very effective to decrease drastically the leakage currents through bulk-drain and bulk-source junctions of the transistors that form the bridge rectifier and, consequently, increase the efficiency of the rectifier. The proposed BBCC switches efficiently the source-bulk and drain-bulk junctions of the bridge rectifier transistors to maintain them in reverse biased. According to the experimental results achieved, the overall power efficiency obtained is 72.5% for 915 MHz at 2 kΩ load. The proposed BBCC-based rectifier

shows to be more efficient than other rectifiers found in recent scientific literature.

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