A Simulation Methodology for Wirebonds Interconnects of Radiofrequency Integrated Circuits

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ABSTRACT

This work presents a methodology for the simulation of bonding wires under the circumstance when signals with RF frequencies are employed and thus, the impedances of the parasitic resistances, capacitances and inductances of these interconnections are no longer negligible. A s-parameters extraction strategy for each of the wirebonds will be shown with the help of Agilent's EM simulator ADS resulting in a netlist in spectre which will be used in the test-bench of the designed IC to emulate the behavior of the bondwires and thus making possible a proper dimensioning and tuning of the RF chip to ensure a better performance of the encapsulated RF IC. Finally the design example of a power amplifier is proposed and some aspects of the interaction of this block with the wirebonds are studied.

Index Terms: RF IC Design, 3D EM Simulation, wirebonds.

I. INTRODUCTION

The Integrated Circuit (IC) technology development is resulting on constant reductions of the physical dimensions of the devices and the increasing of the frequency and area used in each chip. This brings a very big challenge regarding to the interconnects of the chip, especially for the wirebonds which may, due to its physical dimensions, have impedances with magnitude high enough to compromise the performance of the Radiofrequency (RF) IC [1]. Nevertheless, the bonding wire interconnection is still very commonly employed for RF ICs [2] and therefore it is necessary to implement a proper design methodology which will take into account, the influence of the electrical characteristics of the packaging and interconnections.

Some package houses provide the model for the wirebonds interconnects, but it is not unusual that the IC application requires a package type that was not yet modelled or it is going to be built for prototype purposes on a local research lab. Hence, in this case, no model is available.

The present work provides a strategy to simulate the interconnects by using 3D Electromagnetic (3D-EM) simulators, and as a result, predict with good accuracy the impact of the interconnects on the performance of RF IC blocks such as Low Noise Amplifiers (LNAs) and Power Amplifiers (PAs). Additionally, a practical example presents the analysis of the impact of the input impedance of the PA when the effect of the wirebond is not taken into account.

The main constraints for the proper modelling of the electrical behavior of the bonding wire are the geometry of this interconnect, the electrical characteristics of its raw material (commonly gold, aluminum or copper) and the geometry and electrical characteristics of surrounding wirebonds and package structures which accounts for coupling capacitances and mutual inductances.

A very common way to extract the s-parameters matrix of the wire bondings (from which the impedances may be derived) is by means of 3-Dimensional ElectroMagnetic (3-D EM) simulations. For this work Agilent's ADS (Advanced Design System) tool will be employed to make the 3-D EM simulations.

Nevertheless, it is necessary to simulate the package structures while in the presence of the wirebonds due to capacitance coupling and mutual inductance involved. Even though it is possible to

custom design the whole package structure on ADS, there are some of these package structures that are predesigned and tested. The QFN (Quad-Flat No leads) package is very commonly used for RF IC and it is possible to find ADS design kits for this package on AMKOR's website [3]. For this reason, the examples of this work will be designed for a QFN-68 package. Developments for other packages will be considered in the future.

The geometry of the wirebonds is modelled as a polygon with design co straints defined by [4]. This model also comprises a series of analytical expressions for the extraction of important electrical and geometrical characteristics such as inductances, DC resistances and wire lengths.

Once the simulations are finished, an s-parameters file (.s2p) is generated and it is possible to convert this to a netlist (spice, hspice, spectre and others) which will be the model for the wirebond component employed on the simulated test bench. This will make possible for the RF IC designer to make a proper dimensioning and tuning of the circuit while taking in consideration the electrical behavior of the bonding wires and package structures.

II. LAYOUT PREPARATION

The design flow of low frequency ICs commonly starts by the specification of the product, definition of the blocks of the system, and then the front-end development (schematic for analog circuits and RTL for digital). For RF circuits, it is necessary to take some back-end strategies before the start of the front-end development. This happens due to the influence of the interconnects on the overall encapsulated RF IC behavior which needs to be taken into account while developing the schematics of the RF circuits.

This is why it is important for mixed-signal ICs with RF front-ends to have the definition for pads and interconnections beforehand in such a way that the choice of the package and the distribution of wirebonds might be done before the start of the front-end development. If that strategy is not taken into account the RF design will experience an unnecessary rework which may take an important time and compromise the schedule for the tapeout of the chip.

Fig. 1 shows an example of a padring which is one of the main tasks while developing the correct planning of the system requirements. It is the basis for the alignment, geometric configuration and distribution of wirebonds throughout the package structure.

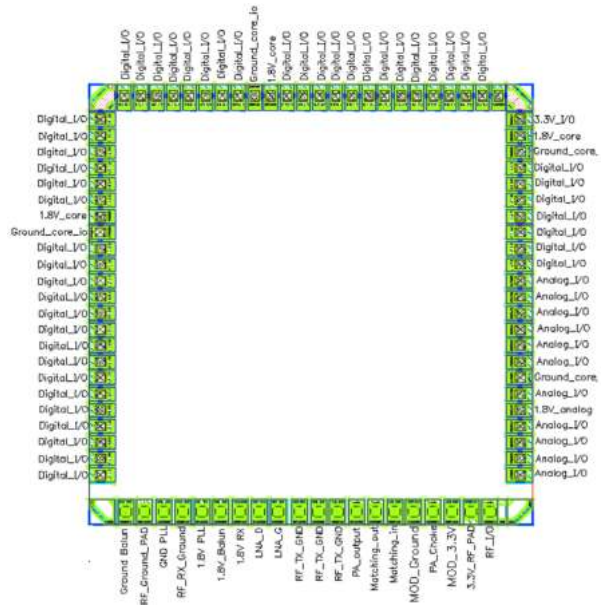

Figure 1. Example of the layout of a padring

Then, the padring layout is exported to a gdsii format which ADS is able to read and import.

III. LOADING THE PACKAGE DESIGN KIT AND DESIGNING THE WIREBOND DIAGRAM

It is very important to have a pre-defined design of the package to be used. The choice for the package is possible after the padring is done. As an example, it will be used the AMKORs design kit for the QFN-68 package for ADS. Once the package design kit is loaded, it is necessary to make the library shared and thus possible to add new layouts. This ensures that the layout of the chip with the package and interconnections be created attached to the technology of the design kit, which includes the substrate (Fig. 2) where the information about each layers electrical and physical characteristics can be found.

Within the new layout, an instance of the QFN-68 package is included. Then it is necessary to make the placement of the imported gdsii of the padring (typically on the center of the package).

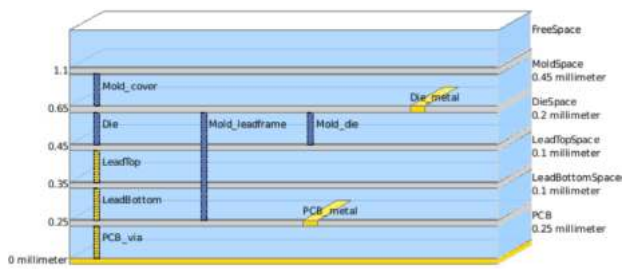

Figure 2. Substrate of the QFN-68 package

Then it is possible to instance the JEDEC wirebond cells connecting each pad to its respective lead. The resulting design containing the padring (or the whole chip layout), the package and each of the wirebonds is known as the wirebond diagram (Fig. 3).

Once the wirebonding diagram is ready, a 3D EM simulation is set. The frequency plan for this simulation may include disjoint intervals of frequencies.

IV. LOADING THE PACKAGE DESIGN KIT AND DESIGNING THE WIREBOND DIAGRAM

The 3D EM simulation is made without the padring because there are so many vias in each pad that the simulation time and memory needed would be impracticable. Nevertheless, the padring is still very important for the alignment of wirebonds and for the choice of the package.

Once the wirebonding diagram is ready, a 3D EM simulation is set. The frequency plan for this simulation may include disjoint intervals of frequencies. Thanks to this feature

of the tool, it is possible to simulate only the range of frequencies of interest, reducing the simulation time.

It is important to mention that the DC frequency must be included on the frequency plan otherwise, the circuit may show an awkward behavior for DC such as the presence of an impedance with negative real part. This might happen because of a linear extrapolation of the s parameters at the last frequency range simulated. Actually the s-parameters of the wirebonds typically changes at a non-linear rate so the linear extrapolation from high frequencies to DC will very commonly yield imprecise and inadequate results. For the example shown on this work it is simulated the frequencies ranges from 0 to 500 kHz and from 2GHz to 5GHz.

Once the substrate (Fig. 2) is prepared, it is necessary to probe the pad and lead terminals with ports (arrows on Fig. 3). These ports will inject current density through the ports with many different frequencies and from the reflecting waves it will determine the s-parameters. The engine used was Momentum (MOM). Other techniques such as FDTD (Finite Difference Time Domain) and FEM (Finite Element Methods) are also possible, but the MOM technique was accurate and fast enough for the application considered on this paper.

Finally, the result of the simulation is an s-parameters matrix as a function of frequency (Fig. 4). It is written on a 2 ports s-parameters touchstone file (.s2p). There is a discontinuity on the derivative with respect to frequency in each s-parameters graphic due to the disjoint frequency intervals. The resistance (loss) and quality factor may be obtained [5] from ADS function definitions (1) to (5).

$$Zwb = stoz(s) \quad (1)$$

$$Zwb1p = Zwb(1,1)\text{-}2 * Zwb(1,2)Zwb(2,2) \quad (2)$$

$$Leff = imag(Zw1p)/(2 * pi * freq) \quad (3)$$

$$Reff = real(Zwb1p) \quad (4)$$

$$Q = imag(Zw1p)/real(Zwb1p) \quad (5)$$

First, the resulting 2-port s-parameters from the 3D-EM simulation is converted to a 2-port z-parameters, by means of the stoz() ads function (1). Then, expression (2) converts the data to a one-port z-parameter which is the impedance of the wirebond. Finally, expressions (3), (4) and (5) are respectively responsible to find the inductance, resistance and quality factor of the wirebond.

The simulation at Cadence's Virtuoso is made by means of an n-port component, from which the .s2p file may be used directly, or through a netlist (spice, hspice,

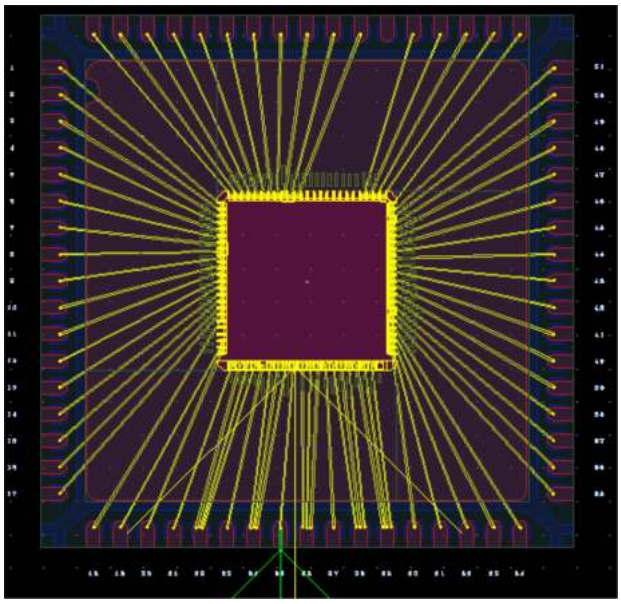

Figure 3. Wirebond diagram of the chip

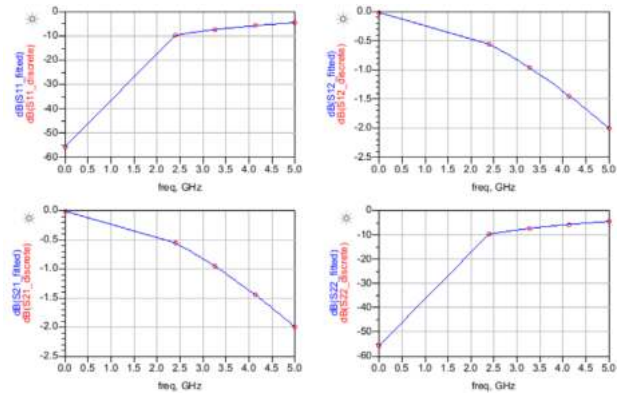

Figure 4. S-parameters matrix (main result for the 3D-EM simulation)

spectre and other) file obtained from the .s2p file by means of a non-linear broadband conversion [6]. In any case, the model of the wirebond will be taken in consideration for the tuning of the RF circuits during the design phase.

V. DESIGN EXAMPLE

One of the most sensitive blocks to the wirebonds electrical behavior is the Power Amplifier (PA). This happens because the wirebonds impedance represents a source degeneration (Fig. 7) for the amplifier and this represents a degradation of the power gain which is one of the most important design parameters of this block.

The PA of the example is a sub block of the transmitter system which is part of a real design of a mixed-signal CMOS RFID chip compliant with the ISO 18000-4 standard for the 2.4GHZ ISM band [7]. Its input is connected to the output of the Amplitude Shift Keying (ASK) modulator through a tapped capacitor input matching network (Fig. 5).

The parameters considered for the wirebonds were:

- Material: Gold
- Diameter: 12.5μm
- Package: QFN-68
- Model for the geometry: JEDEC [4]

After the 3D EM simulation and extraction of the s parameters of the bonding wire interconnections, the model of the wirebond for the ground terminal of this transmitter was obtained and instanced on the testbench of the transmitter. Some important parameters at 2.4GHz are:

- Inductance: 2.45nH
- Effective Series Resistance: 715mΩ
- Quality Factor: 52.7
- Wirebond length: 2.7mm

This result is approximately in accordance to the thumb rule of 1nH of inductance for each millimeter of length of the wirebond. Nevertheless it is more precise and more reliable because the result was obtained from a 3D EM simulation. It would be very tempting, due to the high quality factor of the wirebond inductor, to change the on-chip inductor L_1 to a wirebond inductor.

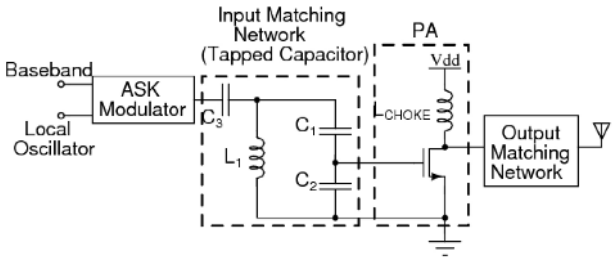

Figure 5. Example of an ASK transmitter architecture

Unfortunately, the resulting network still has a wirebond on the source of the PA transistor. The result is a series RLC network with a low impedance at the resonance. This disables the main feature of the tapped capacitor matching network which is a high input impedance and a low impedance output. For this reason it is necessary to implement L_1 as an on-chip device.

The inductance of on-chip inductors such as L_1 in Fig. 7 and wirebonds have the same order of magnitude (some nanohenries at 2.4GHz). Therefore, it is expected that the input impedance of the PA be considerably changed when a wirebond is added to the source terminal of the circuit.

As a result, if the effects of the wirebonds are not taken in consideration, the matching of the input of the Power Amplifier is compromised (fig. 6). The return loss differences around 6dB and the resonance frequency is shifted 32MHz ahead. This may result on a considerably big degradation of the PA performance.

The return loss ($S_{11,dB}$) is obtained by adding a port to the input terminal of the matching network and setting the simulation to a sweep within the frequency of interest.

Nevertheless, one of the main design specifications of the Power Amplifier is the output power and its drain efficiency. The insertion of wirebonds on the output and ground pad has a greater impact on these features of the PA.

The output matching network of a PA has to be carefully designed in order to ensure that the drain of the transistor sees an impedance as close to the optimum impedance as possible. Since the device has limited current and voltage swings, it is necessary to use a different strategy than the common conjugate

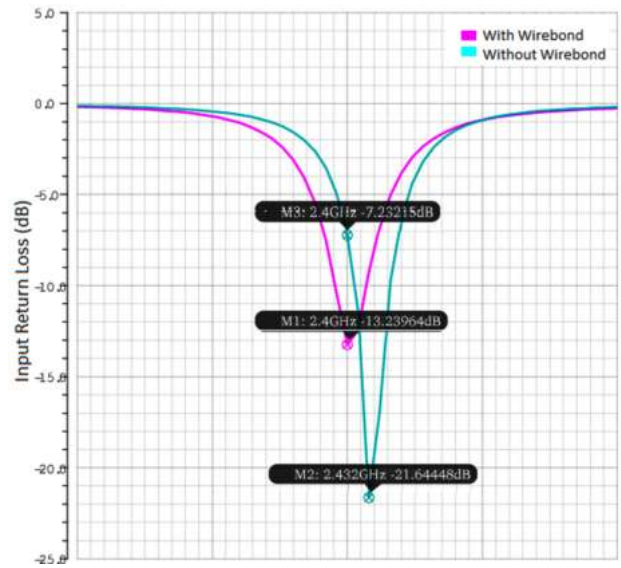

Figure 6. Comparation of the return loss at the input of the PA with and without wirebonds at the source terminal

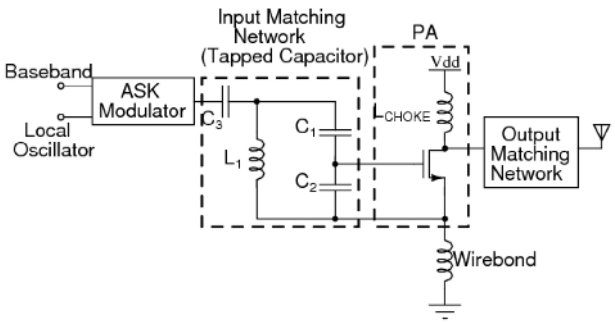

Figure 7. Example of an ASK transmitter architecture with wirebond

match. One of the most commonly used techniques is the load-pull measurement [8]. It consists of a plot on a smith chart of constant power contour by means of an adequate sweep over the impedance seen by the transistor of the PA.

Fig. 8 shows the load-pull contour of a PA designed without taking in consideration the effects of the package interconnects. The main results of this analysis are the normalized (50 ohms) optimum impedance (as a function of the reference impedance) and the maximum output power achieved when the optimum impedance is connected to the output of the PA.

In order to evaluate the impact of the insertion of the wirebonds on the ground pad of the PA, the optimum impedance was connected to the output of the PA and after a transient simulation, the average power delivered to the load and the power efficiency were evaluated. Then, the wirebond models, resulting from the 3D-EM simulation presented for the input matching considerations was connected to from the source of the PA transistor to the ground and the simulations were run again. Table contains the resulting data and is used to compare the results.

The main design specifications of the PA were therefore seriously compromised by the packaging interconnections since the changing on the optimum impedance resulted in a drastic change on the output power and efficiency. Hence, it is remarkable the importance of the precautions regarding to wirebonds and packaging structures influence towards the design.

Fig. 9 shows the result of the load-pull analysis if the interconnect parasitics were taken into consideration before the design of the PA in this example. The same devices and bias were used, except that now the load-pull analysis is done with the wirebond connected to the source of the transistor.

The resulting maximum output power at the optimum load impedance is around 5dB lesser than that observed before considering the package interconnects effects. This happens because the wirebond works as a source degeneration of the PA, which yields a lesser gain (but higher linearity) for this circuit.

Table I. Comparison between two PAs with same structure except for the wirebond interconnect.

Configuration	Output Power (dBm)	Efficiency	Optimum Impedance (Ω)
With wirebond	18.93	32.30	13.5+j8
Without wirebond	23.95	12.64	26.6+j1.88

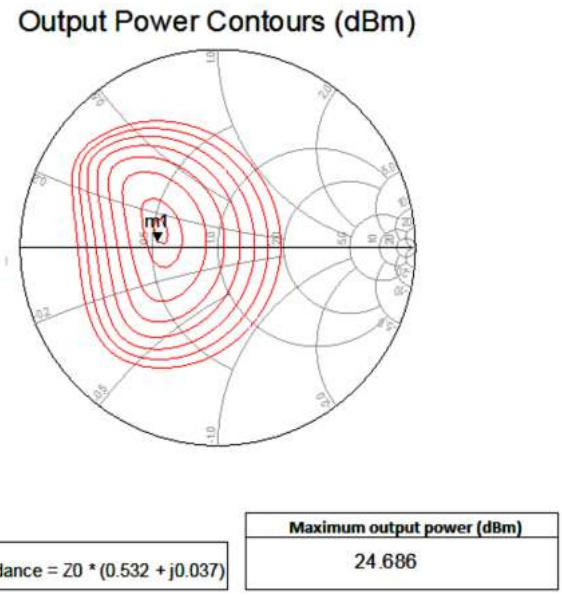

Figure 8. Load-pull of a PA that was designed without taking into account the effects of the wirebonds.

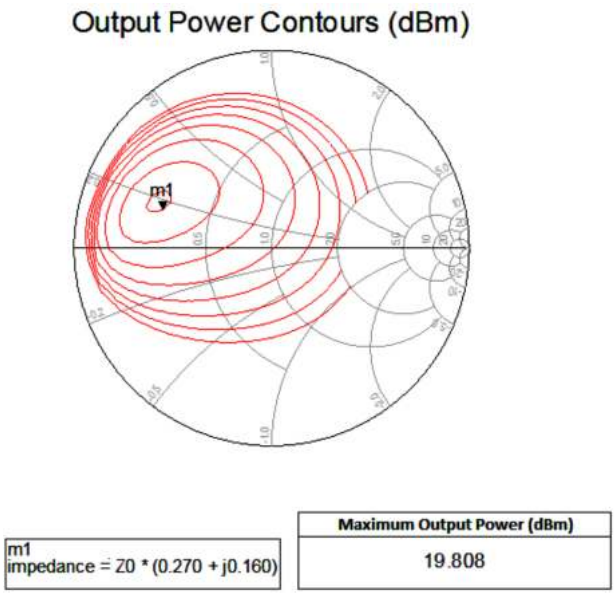

Figure 9. Load-pull of a PA that was designed without taking into account the effects of the wirebonds.

VI. WIREBOND COUPLING

The high integration level of modern IC implementations is increasing the density of interconnections of a package. This situation makes it necessary to choose carefully the position of each of the wirebonds because adjacent interconnects may experience some interference from one wirebond to another due to electromagnetic induction.

Fig. 10 shows the result of the EM simulation over the chosen package. The colors indicate the level of current density over the stimulated pad. Intense current is depicted by colors close to red while a low current is represented by tones close to blue.

The coupling effect may be simulated with the methodology proposed on the present work. It is necessary, for this end, to assign 2N ports for N wirebonds. The cross-terms (S_{31}, S_{13}, S_{14} and so on) are the responsible for the accounting of coupling between the wirebonds.

As an example, two adjacent wirebonds of the QFN-68 package were chosen and one of then was stimulated with a 0dBm 2.4GHz signal. Then, it was observed a -50dBm signal at the adjacent wirebond.

It is reasonable to avoid having wirebonds carrying small signals such as the input of a Low Noise Amplifier (LNA) close to interconnects responsible for high power RF signals, as it is seen on the output of PAs.

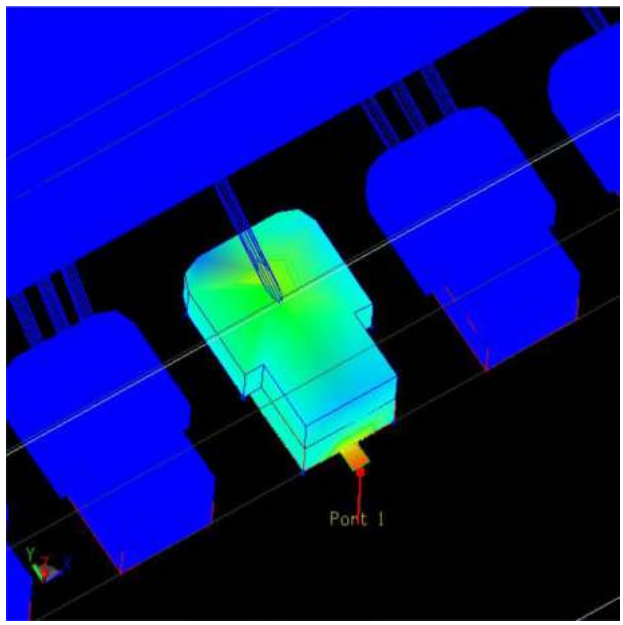

Figure 10. Coupling of adjacent leads of a package

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