

Effect of Substrate Bias and Temperature Variation in the Capacitive Coupling of SOI UTBB MOSFETs

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Abstract— In this work, the electrical features related to the capacitive coupling and temperature influence of the Ultra-Thin Body and Buried Oxide SOI MOSFET (UTBB) transistors are explored through numerical simulations calibrated to experimental data. The impact of the substrate bias is observed for a set of values ranging from -3 V to 2 V for a temperature range between 100 K and 400 K. Also, structures with n- and p-type ground planes (GP-P and GP-N) and without GP have been evaluated. This approach analyzes the capacitive coupling through the body factor and shows that the negative biasing for all GP types significantly improves the structure coupling and that the device with P-type ground plane has the lowest value of body factor for all the evaluated conditions. The dependence of the body factor on the temperature has shown to be negligible for longer devices. However, for devices shorter than 50 nm, the position of the maximum electrons concentration inside the silicon layer may affect the capacitive coupling.

Keywords- Substrate Bias, UTBB, Capacitive coupling, Body Factor, mobility

I. INTRODUCTION

The continuous demand for increasing the integration density of the integrated circuits has led to the exponential reduction on the MOSFETs dimensions since the middle of the 60's [1]. However, along the last decades, the reduction in the devices dimensions has been inefficient due to the occurrence of unwanted effects such as large parasitic currents and capacitances. These phenomena are related to short channel effects (SCEs) [2,3,4], which tend to appear at extremely reduced dimensions. So that, it has been necessary to develop novel technologies such as the SOI-MOSFET that consists in a MOSFET structure with the active silicon channel layer isolated from the wafer substrate by a buried oxide layer (BOX) [2].

This structure presents a large reduction in SCEs with respect to the conventional (or bulk) MOSFET technology as well as inherently reduced parasitic effects due to channel insulation. However, for ultra-submicrometer devices even devices fabricated in conventional SOI technology exhibit strong SCEs [4]. For that reason, some improvements have been proposed. Initially, it was proposed the reduction of the silicon layer in order to enhance the capacitive coupling of the structure (UltraThin Body transistor - UTB). However, for small devices, the thin silicon above a thick buried oxide can bring some drawbacks such as the self-heating, once the BOX layer present low thermal coefficient and harms the heat removal of the silicon channel [5,6,7].

In the sequence, as an evolution of the UTB devices, it was proposed a transistor in which both the silicon and the buried oxide layer were reduced. This device has been called UTBB (UltraThin Body and Buried Oxide) SOI MOSFET and its

schematic is shown in Figure 1. Due to the small thickness of the BOX layer (10-20 nm) [8,9,10,11], it can be used as a second gate for the transistor, improving the capacitive coupling of the structure. Both top and bottom gates are independent, such that the potential applied to the substrate (V_{BS}) can be adjusted to improve the devices characteristics [12]. Usually, a negative potential applied to the substrate reduces the leakage whereas a positive bias makes the device faster, since the threshold voltage can be modulated by the variation of V_{BS} . In order to enhance the effect of the V_{BS} application as well as to allow the access of the substrate of individual transistors, a highly doped thin silicon layer is created below the BOX layer, which is called ground plane (GP) [12, 13]. This layer can present N- or P-type doping concentration as also shown in Figure 1.

However, the variation of V_{BS} changes the capacitive coupling of the structure, affecting the subthreshold swing as well as the current capability of the devices. For that reason, this work will verify the behavior of the UTBB-SOI-MOSFET capacitive coupling when its substrate is biased from -3 V up to 2 V for structures with N- and P-type GPs and without GP. This analysis has been performed for a channel length range from 20 nm to 500 nm.

Another important point to be considered is the devices temperature of operation that is directly related to the carriers' mobility and concentration and could affect the body factor. Thus, the analysis was extended considering the structures and bias mentioned above for temperatures varying from 100 K to 400 K.

II. DEVICES AND SIMULATIONS CHARACTERISTICS

The analysis of the substrate biasing on capacitive coupling in UTBB SOI-MOSFET transistor was carried out through 2D numerical simulations performed in Sentaurus Device TCAD [14]. This software was chosen because of its well-known robustness and its simulation feature, which

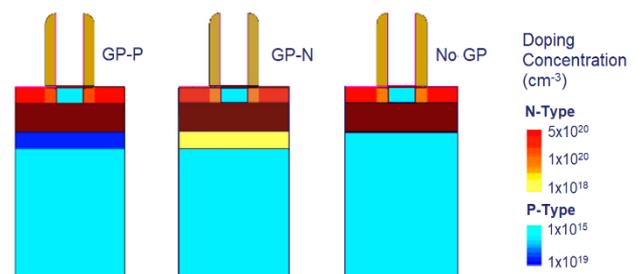


Figure 1. Three SOI UTBB transistor with $L=20\text{nm}$; $t_{si}=10\text{nm}$, $t_{box}=20\text{nm}$ and P- and N-type Ground Planes (GP-P and GP-N, respectively) and no GP.

consists in a grid of points that allows the construction and simulation of any structure.

Along the simulations, the devices were defined with silicon channel thickness (t_{si}) of 10 nm, top gate oxide thickness (t_{ox}) of 1.7 nm, buried oxide thickness (t_{box}) of 20 nm, drain and source lengths (L_{fd}) of 30 nm, channel length ranging from 20 nm to 500 nm, source and drain arsenic doping concentration of $5 \times 10^{20} \text{ cm}^{-3}$ and channel and substrate boron doping concentration of $1 \times 10^{15} \text{ cm}^{-3}$. The ground plane presents thickness (t_{gp}) of 10 nm with doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$ and $1 \times 10^{18} \text{ cm}^{-3}$ for the P- and N-type GP, respectively. All the devices' characteristics were chosen based on the UTBB structure described in [10,11,15], proposed by STMicroelectronics.

The simulation performed in Sentaurus account for models considering the effects of the mobility degradation through vertical and longitudinal electrical fields as well as temperature variation, bandgap narrowing, carriers' generation and recombination and quantum confinement. For temperatures of 100 and 200 K, incomplete ionization of carriers was also accounted. The overall analysis was performed for V_{GS} ranging from -0.5 V to 1.2 V, V_{BS} ranging from -3 V to 2 V, $V_{DS} = 50 \text{ mV}$ and temperatures ranging from 100 K to 400 K.

In order to validate the simulations for different gate and drain biases (V_{GS} and V_{DS} , respectively), drain current (I_{DS}) as a function of V_{GS} are validated to the experimental data from [11] as shown in Fig. 2. On the other hand, in order to validate the devices' behavior against the temperature, the drain current and the thermal resistance of the UTBB devices were validated to the data from [15] similarly as done in [16]. The comparison between simulated and experimental data are shown in Table 1.

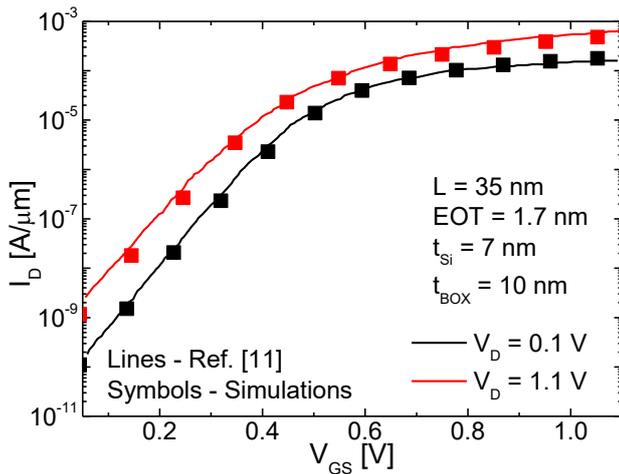


Figure 2 Normalized drain current as a function of gate voltage for simulated and experimental data of [11] biased at different V_{DS} .

Table I. Comparison between simulated data and the measured one from [15].

Parameter	t_{box}	Data Comparison		
		Simulation	Experimental	% Error
Drain Current [mA/μm]	10 nm	0.55	0.55	0
($V_{GS} = V_{TH} + 0.8 \text{ V}$ and $V_{DS} = 1 \text{ V}$)	25 nm	0.80	0.80	0
Thermal Resistance [μm Km/W]	10 nm	69	70	1.42
	25 nm	80	84	4.34

III. CAPACITIVE COUPLING ANALYSIS

The first step of the analysis consisted in the simulation of the drain current (I_{DS}) curves as a function of the gate voltage for the devices with and without ground plane biased at $V_{DS} = 50 \text{ mV}$ and $V_{BS} = 0 \text{ V}$ for different channel lengths (L). In Fig. 3 (A), one can see the simulated I_{DS} curves normalized by (W/L) as a function of V_{GS} . It is possible to see that a reduction in L promotes an I_{DS} reduction due to the increase in the series resistance.

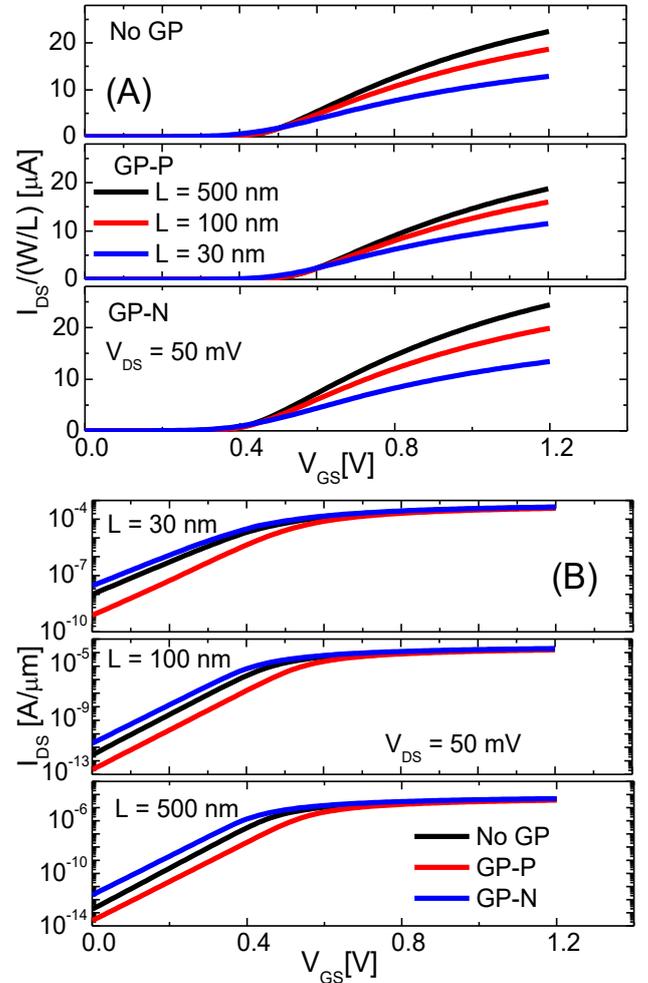


Figure 3 Normalized drain current as a function of gate voltage for three settings of ground plane and $V_{BS} = 0 \text{ V}$ in linear (A) logarithmic (B) scales.

In Fig 3 (B), I_{DS} is presented in logarithm scale as a function of V_{GS} where it is possible to observe the degradation of the subthreshold of the devices for $L \leq 50 \text{ nm}$ due to the SCEs, as well as a lowering of V_{TH} due to the occurrence of SCEs. Considering the same L and a fixed bias, a larger current is observed for the N-type ground plane device mainly due to the smaller V_{TH} .

In order to evaluate the capacitive coupling of the structure, the subthreshold swing (SS) of the devices was obtained for different substrate biases. This parameter represents the variation of V_{GS} needed to shift I_{DS} in one order of magnitude. SS can be directly extracted from $I_{DS} \times V_{GS}$ curves by the inverse of the derivative of logarithm of I_{DS} as a function of V_{GS} . The curves of the subthreshold swing are exhibited in Figure 4 as a function of the channel length for different substrate bias. It is possible to see a nearly exponential trend of SS as the channel length decreases, which can be associated to the intensification of the short channel

effects that cause the control loss of part of the depletion charges by the gate [17,18], thus varying the capacitive coupling.

By the ground plane point of view, the p-type ground plane presents slightly smaller values, which could be related to the capacitive coupling of the structure. In this figure, it is also possible to observe that as more negative is the substrate biasing, lower is the subthreshold slope. The negative V_{BS} tends to lead the interface between silicon and buried oxide to the accumulation. In this case, the current flows closer to the gate dielectric interface and the top gate presents a better control over the channel charge.

To better understand the behavior of I_{DS} and subthreshold swing with respect to the capacitances of silicon and gate oxide, SS can be written according to expression (1), which associates the subthreshold slope to the body factor ($n = 1 + \alpha$).

$$SS = \frac{kT}{q} \ln(10)(1 + \alpha) \quad (1)$$

where T is the temperature. The body factor is used to measure variation in the threshold voltage due to substrate biasing and it can also be associated to the variation of the surface potentials and, consequently, the variation of the capacitive coupling on device and as smaller its value, the higher is the quality factor. The body factor in an SOI fully depleted device is given by expression (2) [2].

$$n = (1 + \alpha) = 1 + \frac{C_{Si}C_{OX2}}{C_{OX1}(C_{Si} + C_{OX2})} \quad (2)$$

The body factor in a fully depleted device is approximately given by the ratio between the series association between the silicon and buried oxide capacitances (C_{Si} and C_{OX2} , respectively) by the gate oxide capacitance (C_{OX1}). For very thin silicon layers, such as in the case of the UTBB, the point of the silicon layer in which the centroid of charge is located, i.e. the point where there is the highest concentration of electrons, becomes important. So that, expression (2) must be rewritten in terms of the position of the centroid of charge (X_{bar}), as shown in (3) [19].

$$n = 1 + \frac{t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{Si}}(X_{bar})}{t_{box} + \frac{\epsilon_{ox}}{\epsilon_{Si}}(t_{Si} - X_{bar})} \quad (3)$$

where ϵ_{ox} and ϵ_{Si} are the permittivities of the oxide and silicon respectively.

In Figure 5, the body factor for devices with no GP is presented as a function of the V_{BS} . For the extraction of the body factor, the subthreshold slope (SS) was obtained through the minimum point of the inverse of the derivative of the logarithm of I_{DS} as a function of V_{GS} and, then, n was calculated through expression (1). The smaller the channel length, higher is the body factor presented. Due to the occurrence of short channel effects, the depletion charge controlled by the gate is reduced. Although not explicitly demonstrated in the equations (2) and (3), the reduction on the depletion charge results in an alteration of the silicon capacitance of eq. (2), which increases the body factor.

As one can also see in the figure, for all the channel lengths evaluated, a lower body factor, i.e., better capacitive coupling, is noticed for negative substrate biasing. This effect can be explained through expression (3). As the substrate bias is reduced, the electrons inside the silicon layer are pushed to

the upper part of the channel, closer to the interface with the gate oxide. In this case, the centroid of charge is closer to the top interface, resulting in a small value for X_{bar} , which induces a smaller α . As the substrate bias is increased, part of the electrons is pushed down to the back interface, moving the centroid deeper inside the silicon layer and increasing X_{bar} , which results in an increment of the body factor.

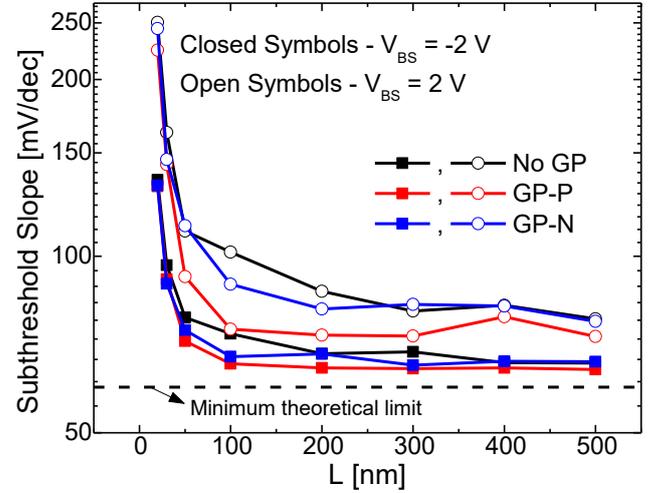


Figure 4. Subthreshold slope as a function of the channel length for devices with N- and P-type GPs and without GP for V_{BS} of -2 V and 2 V.

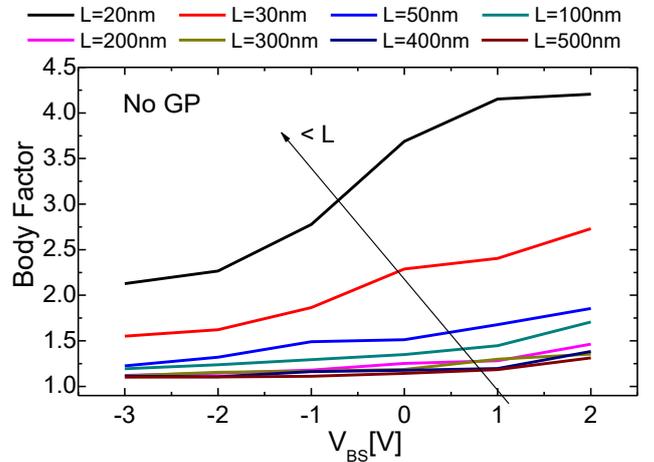


Figure 5. Body factor as a function of substrate bias for devices with channel length ranging from 20 nm to 500 nm.

Figure 6 presents the body factor as a function of the channel length for devices with N- and P-type ground planes and without ground plane biased at $V_{BS} = -2$ V, 0 V and 2 V. It is possible to perceive that, contrarily to the strong variation in the body factor promoted by the substrate biasing, the ground plane does not make a large difference in the capacitive coupling.

In order to better observe the impact of the GP in the body factor of the devices, Figure 7 presents the body factor as a function of the substrate biasing for different ground planes and channel lengths. In this figure, it is possible to see that for more negative biasing, the effect of ground plane implantation is reduced, i.e. all the devices configurations (P-type, N-type or no GP) present similar body factor. However, for positive substrate bias, the P-type ground plane promotes a reduction in n . The different body factor are related to the different flatband voltages of the second interface of the

devices, i.e. closer to the buried oxide. For N-type GP, for example, the flatband occurs at lower gate voltages, which indicates that, at a similar biasing condition, such device present a stronger depletion at the second interface.

Anyway, the P-type ground plane presented better values of body factor for all channel lengths as well as, the smaller the channel length, higher the short channel effects and, the greater the short channel effects, more efficient is the negative biasing for reducing them.

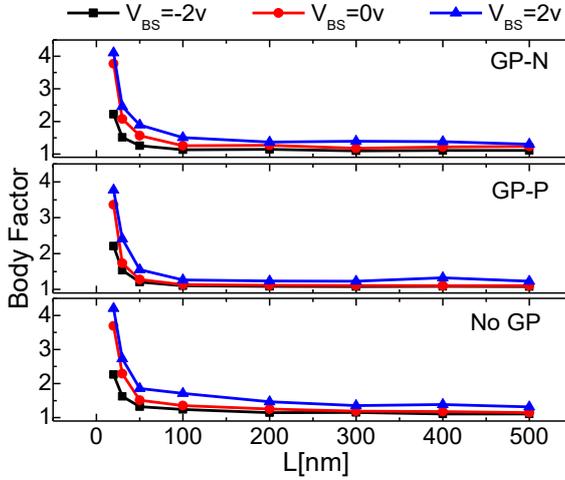


Figure 6. Body factor as a function of channel length ranging from 20nm to 500nm for three settings of ground plane and V_{BS} ranging from -3 V to 2 V.

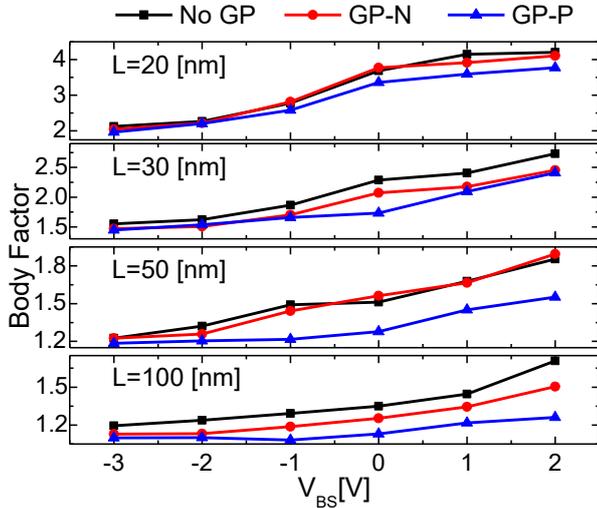


Figure 7. Body factor as a function of V_{BS} biasing ranging from -3 V to 2 V for channel length ranging from 20nm to 100nm for all ground planes.

IV. TEMPERATURE VARIATION ANALYSIS

In this approach, the analysis was performed through the simulation of the drain current curves as a function of the gate voltage for the devices with and without ground plane biased at $V_{DS} = 50$ mV and for different channel lengths and V_{BS} with the temperature ranging from 100 K to 400 K.

The curves of the threshold voltage as a function of the temperature for different ground plane configurations and V_{BS} varying from -2 V to 2 V are presented in Figure 8 for (A) $L = 30$ nm and (B) $L = 100$ nm. It is possible to notice that for $V_{BS} = 0$ and 2 V, the threshold voltage increases with the reduction of the temperature for both channel lengths. However, a reduction in the dV_{TH}/dT ratio is observed as V_{BS}

is changed from 2 to 0 V for devices of different L , as detailed in Table II. This behavior could be expected since the Fermi potential (Φ_F) rises for lower T , owing to the intrinsic carrier concentration (n_i) reduction, as shown by (4) and (5)

$$\phi_F = \frac{kT}{q} \ln\left(\frac{NA}{n_i}\right) \quad (4)$$

$$n_i = 3.9 \times 10^{16} \times T^{\frac{3}{2}} \times e^{-\frac{E_g}{2kT}} \quad (5)$$

where E_g is the energy bandgap and kT/q is the thermal voltage, being k the Boltzmann constant and q the elemental charge.

For $V_{BS} = -2$ V, devices of both of channel lengths present V_{TH} nearly constant with T , as shown in Figure 8 as well as in Table II. This behavior can be related to the potential in the third interface (Φ_{sub}), i.e., between the buried oxide and substrate.

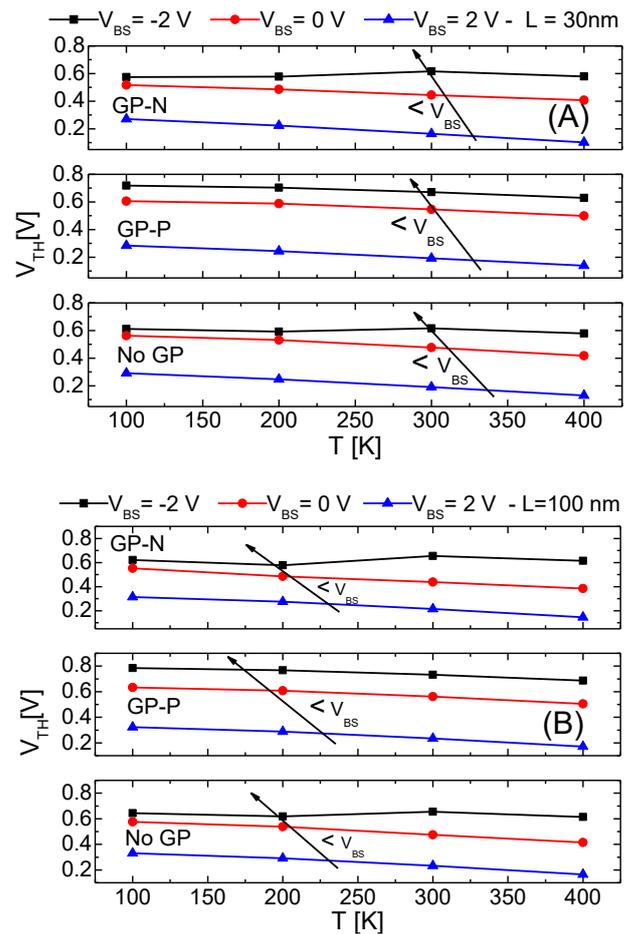


Figure 8 Threshold voltage as a function of temperature ranging from 100 K to 400 K for devices with three settings of ground plane, (A) $L = 30$ nm and (B) $L = 100$ nm.

Table II. Variation of the threshold voltage with the temperature between 100 and 400 K for devices of different L biased at different V_{BS} .

Channel Length (nm)	V_{BS} (V)	dV_{TH}/dT (mV/K)		
		GP-N	GP-P	No GP
30	-2	0.05	-0.30	-0.08
	0	-0.37	-0.36	-0.49
	2	-0.57	-0.49	-0.54
100	-2	-0.06	-0.33	-0.05
	0	-0.55	-0.43	-0.55
	2	-0.56	-0.51	-0.56

The gate voltage in a fully depleted SOI influences the surface potentials close to the gate and buried oxides, i.e., first the second interfaces, respectively, and is given by expression (6) [2],

$$V_{GS} = \phi_{MS1} - \frac{Q_{OX1}}{C_{OX1}} + \phi_{S1} \left(1 + \frac{C_{S1}}{C_{OX1}}\right) - \frac{C_{S1}}{C_{OX1}} \phi_{S2} - \frac{Q_{depl}}{2C_{OX1}} - \frac{Q_{inv}}{C_{OX1}} \quad (6)$$

where Q_{OX1} is the gate oxide charge, Q_{depl} is the depletion charge, Φ_{MS1} is metal gate to silicon work function, Φ_{S1} and Φ_{S2} are the surface potentials in the first and second interfaces and Q_{inv} is the inversion charge in the first interface. To obtain the threshold voltage of the device, Φ_{S1} is considered as twice the Fermi potential, Q_{inv} is assumed to be zero and Φ_{S2} depends on the applied V_{BS} .

As UTBB devices present smaller silicon and buried oxides thicknesses than conventional FD SOI transistors, the potential at the third interface should be accounted for correct determination of Φ_{S2} , which can be calculated through the solution of the following expressions [20-22]

$$V_{BS} = \phi_{MS2} - \frac{Q_{OX2}}{C_{OX2}} + \phi_{S2} \left(1 + \frac{C_{S1}}{C_{OX2}}\right) - \frac{C_{S1}}{C_{OX2}} \phi_{S1} - \frac{Q_{depl}}{2C_{OX2}} - \frac{Q_2}{C_{OX2}} - \phi_{sub} \quad (7)$$

$$\phi_{sub} = \left[\frac{-\sqrt{2qN_{Asub}\epsilon_{Si}}}{2C_{OX2}} + \sqrt{\left(\frac{2qN_{Asub}\epsilon_{Si}}{4C_{OX2}^2} - V_{FB3}\right) + (\phi_{S2} - V_{BS})} \right]^2 \quad (8)$$

where Q_2 is the inversion or accumulation charge in the second interface, N_{Asub} is the doping concentration of the ground plane and V_{FB3} is the flatband voltage between the buried oxide and the substrate [21].

As shown in [20], the potential at the third interface alters the slope of the $V_{TH} \times V_{BS}$ curve. There is a V_{BS} range in which the third interface is depleted, where the dependence of V_{TH} on V_{BS} becomes negligible, i.e. a plateau is observed in the curve of V_{TH} as function of V_{BS} . This range is in the order of 0.5 V for room temperature and increases for T reduction. Thus, for temperatures lower than 300 K, the devices with GP-N and No GP can be biased in this region, which explains the reduction of dV_{TH}/dT observed at some conditions.

In Figure 9, where the body factor is presented as a function of the temperature, we can see a constant or slight reduction of the body factor for low T. When the temperature decreases, the depletion region increases, but as in FD SOI transistor the entire silicon layer is depleted, it does not present any variation in the depletion region. So, the only variation is in the potential inside the silicon layer, which leads to a variation of the maximum electron concentration position (X_{bar}) that is correlated to the body factor by the (3) equation and the quantum confinement effects.

The behavior of X_{bar} variation depends on the biasing condition silicon layer in the GP region. When the silicon in this region is either inverted or accumulated, the potential inside the active layer presents almost no variation and the body factor remains nearly constant along the whole temperature range. When the silicon in the GP region is depleted, it represents an additional capacitance, which is placed in series to the buried oxide capacitance. As the body

factor is given by the ratio between the capacitances below and above the current path, the depletion of the silicon in the GP region can be responsible for a reduction in the body factor. Usually, as the temperature decreases, a larger depletion depth is observed. This phenomenon can lead to a slightly smaller n at lower temperatures.

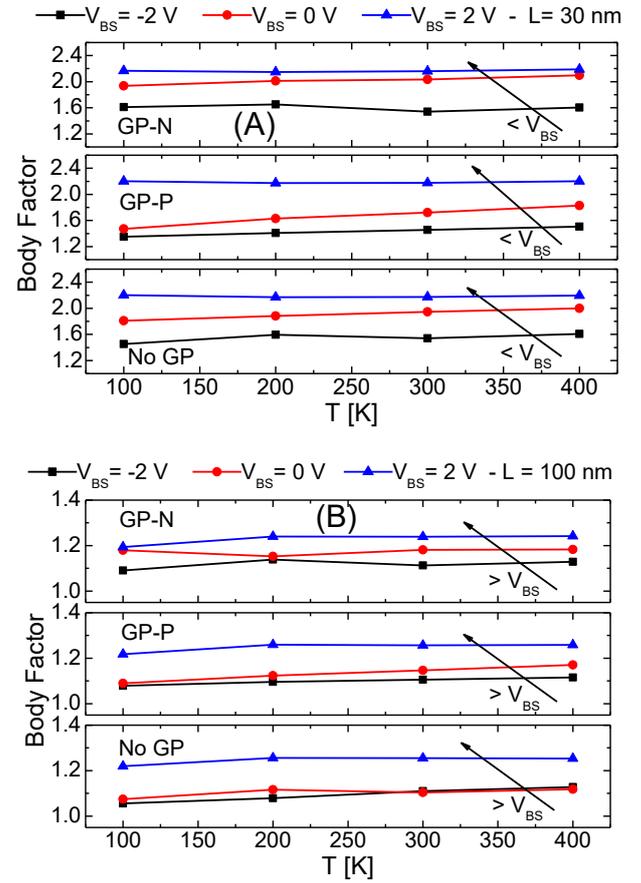


Figure 9. Body Factor as a function of temperature for devices with different GP configurations for (A) $L = 30$ nm and (B) $L = 100$ nm.

The different body factors observed for the different V_{BS} are related to the different flatband voltages of the second interface as previously explained. However, it can also be understood through the X_{bar} position. For negative V_{BS} , the second interface is closer to the flatband, which moves X_{bar} closer to the first interface, reducing n. The opposite occurs for V_{BS} , when the centroid of charge is closer to the second interface, increasing n.

Figure 10 presents an analysis of the body factor as a function of the channel length for three values of substrate bias ($V_{BS} = -2, 0$ and 2 V) as well as the three settings of ground plane and temperatures ranging from 100 K to 400 K. In this analysis, one can see an exponential increase in the body factor for channel lengths below 100 nm related to the increase in SCEs as previously shown. From the point of view of the temperature, it is possible to note that the body factor presents practically no dependence with T for devices longer than 50 nm. For shorter transistors, different trends can be observed depending on ground plane and biasing conditions, which is related to the already mentioned dependence of X_{bar} with the temperature variation.

For the GP-P transistor with $V_{BS} = 0$ and -2 V, the reduction of the temperature clearly reduces the body factor, which can be related to the increase in the depletion layer at the third interface observed for lower temperatures. For $V_{BS} = 2$ V, an accumulation layer is formed in the third interface and the body factor dependence on T becomes negligible. For the GP-N and No GP configurations no significant alteration of body factor is observed as a function of the temperature, similarly as obtained in Fig. 9.

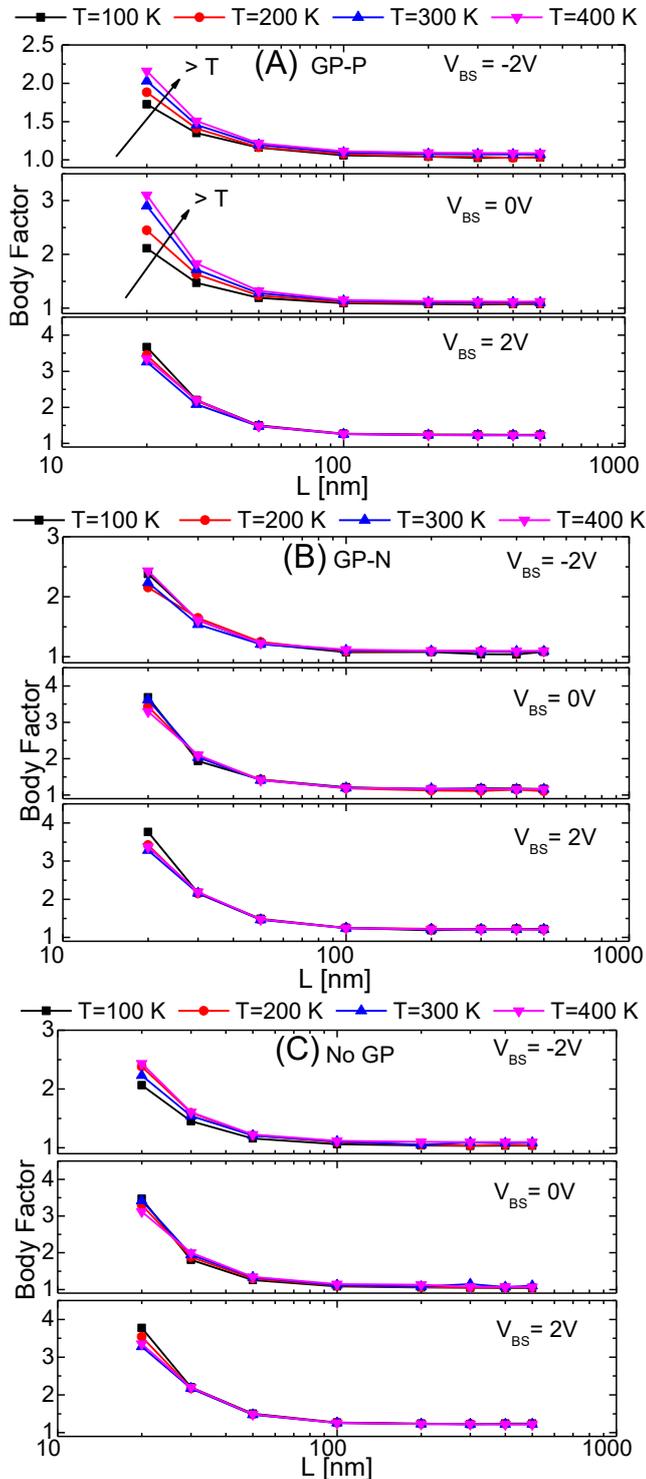


Figure 10. Body Factor as a function of L for T ranging from 100 K to 400 K for (A) GP-P, (B) GP-N and (C) NO GP ground plane configurations.

V. CONCLUSIONS

This paper has presented an analysis through 2D numerical simulations of the electrical features on UTBBs SOI MOSFETs related to capacitive coupling and temperature variation when its substrate is biased and when a ground plane layer is implanted in its body. The structures simulated were chosen to demonstrate the capacitive coupling response to situations where short channel effects are presented in low, medium, and critical intensities as well as the biasing, ground plane settings and temperature variation were chosen in order to fully evaluate the electrostatic responses of the transistors.

From the point of view of obtaining a better body factor, the configuration with a ground plane layer with p-type dopants presented a better efficiency for all the channel lengths, although the dependence of the body factor with GP is not very large. On the other hand, the variation presented in the capacitive coupling due to substrate biasing was shown to be noticeable. The body factor has shown to increase for positive substrate biases and keeps nearly constant for negative substrate biases. In the temperature approach we can see that in some cases the temperature variation is no longer noticeable. However, for some bias conditions, one can notice some body factor variations related to the shift of the position of the point of maximum electron density, which affects the capacitive coupling of the devices.

ACKNOWLEDGMENT

This work was supported by National Council for Scientific and Technological Development (CNPq) grant #303938/2020-0. Everton Matheus da Silva thanks Centro Universitário FEI and CNPq for the sponsorship.

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