The impact of spacer oxide material on the underlapped SOI-nFinFET working as charged based radiation sensor

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Abstract — In this work, the influence of the underlap region on the electrical behavior of a SOI-nFinFET transistor has been studied by numerical simulation with the purpose of radiation sensing. The analysis has been performed by evaluating the impact of spacer length, width and spacer oxide material of the underlap region on the On-state current and by studying its sensitivity. The impact of the underlap region on the drain current and, consequently, on the devices' sensitivity was explained by the analysis of series resistance, the fringing field and electron density. Considering the main impact of radiation in these devices, the study of sensitivity has been also performed taking into consideration the variation of oxide trapped charges density. When applying the transistor to a harsh environment, the underlapped FinFET showed to be a quite respectable radiation sensor, since the results performed with very good sensitivities when using long and narrow spacer oxide with low permittivity oxide. With thicker spacer oxide in the underlap region, the charge concentration makes the spreading field high enough to overcome the series resistance effect, which results in a less sensible device. Since underlapped FinFETs have high sensitivity in the On-state current, reaching 200% for SiO₂ spacer oxide material and V_{DS}=1V, these devices show to be promising to work as charged based radiation sensor. Two different proposals for radiation sensing are presented.

Index Terms — Spacer oxide material, permittivity, charge trapping, underlapped FinFET.

I. INTRODUCTION

Due to the growing society's needs to obtain powerful and quick devices, technologies made in silicon on insulator (SOI) wafers and multiple gates transistors have stood out, for instance, as FinFETs (*Fin Field Effect Transistor*) [1]. This transistor appears in the Moore's law as an alternative for technological nodes below 32 nm due to its strong gates coupling and high control of channel charges. Considering this technology, countless benefits are related like lower power consumption [2], higher processing speeds, better drain induced barrier lowering (DIBL), lower subthreshold slope (SS) and lower short channel effects (SCE) [3]. Besides that, FinFETs also present a higher drain current (I_D) when compared with a planar one, which occupies the same silicon area [4].

The MOSFET technology has been the subject of a wide range of research, including its resilience to the radiation effects, which point out that the electrical behavior of bulk-FinFETs are more damaging than SOI-FinFETs [5]. One of the MOSFET technology application is the use of it in radiation environment, for instance, applying this technology as a radiotherapy dosimeter [6] or gamma and x-rays sensors [7] in conventional MOSFETs. In addition, as reported in [8–

10], the FinFET with fin width (W_{FIN}) equal to 20 nm shows a high immunity to accumulated effects caused by proton total ionization dose (TID), even considering the charges accumulated in the gate oxide and in the buried oxide, due to the high coupling between the gates. Furthermore, there are studies that also evaluate the negative bias temperature instability (NBTI) in FinFETs applied to radiation environment [11].

Additionally, transistors with an underlap region (spacer oxide material) in a gate-to-drain region and/or in a source-to-gate one have also shown benefits. The transistors with this structure are called underlapped transistor due to the lack of part of the gate length (L_G) over the channel length (L_{CH}) and it can be manufactured for single or multiple gates devices, and in both MOS and SOI technologies [12,13]. The underlapped SOI-FinFETs, for example, present good characteristics for analog applications, such as improvement in the intrinsic voltage gain dc (A_{VO}) and low cutoff frequency (f_T) [13]. It is also pointed out better drain induced barrier lowering (DIBL), less saturation current degradation due to better control of charges in the channel surface [3,14], high speed performance and also smaller short channel effects [15]. Due to its physical characteristic, is observed a reduction in leakage current caused by gate-source/drain underlap, however its structure also promotes an increase in the series resistance (R_{SD}) [2,14], which linearly growth with the underlap length increasing. Besides, this structure presents higher capacitances between gate (G) and source/drain (S/D) and an intrinsic R_{SD}, which have to be taken into account in new applications.

Considering that the conventional MOSFET and SOI single gate technologies have been studied as radiation sensor and that underlapped FinFET presents several advantages compared with the single gate planar one, this work aims to study the underlapped SOI-nFinFET behavior in order to qualify and optimize the device structure for radiation sensing applications.

II. DEVICES CHARACTERISTICS

The studied underlapped SOI-nFinFETs have been simulated at TCAD Sentaurus [16] considering the 3D structure. The simulations have been calibrated with experimental behavior of the self-aligned SOI-FinFET at room temperature (300 K) before and after being exposed to proton radiation. The self-aligned SOI-FinFET has been fabricated at Imec, which presents the following characteristics: channel length (L_{CH} = 400 nm), fin width (W_{FIN} = 20 nm) and fin height (H_{FIN} = 65 nm), effective gate oxide thickness (EOT = 2 nm) and buried oxide (t_{BOX} = 145 nm).

After proton radiation, the experimental measurements of self-aligned devices have been performed after stabilization (few months and again after 2 years) and it was demonstrated that the narrow devices have also high immunity to permanent radiation effects (Total Ionization Dose - TID).

The overlapped FinFET device has the same structure to the original SOI FinFET, except for the underlap regions on both sides (gate to source and gate to drain), by inserting the oxide spacer and reducing the gate length (L_G). Knowing that L_{CH} has been kept constant, the gate length can be summarized by equation 1.

$$L_G = L_{CH} - 2 L_{SP} \quad (1)$$

where the L_{SP} is the underlap length.

Fig. 1 shows the schematic structure of the self-aligned SOI nFinFET (A) and overlapped SOI FinFET (B). The effective gate oxide thickness ($EOT = 2$ nm) and gate oxide permittivity ($\kappa = 3.9$) are kept constant for both structures, and the spacer oxide length, width and permittivity are changed. The gate length (L_G) is reduced over the L_{CH} , varying the spacer underlap length (L_{SP}) from 0 nm (self-aligned structure, Fig. 1-A) to 50 nm, leaving the spacer oxide exposed as can be observed in Fig. 1 (B).

Throughout this work, besides the different spacer underlap length (L_{SP}), the impact of the underlap oxide material permittivity (κ) and its thickness (W_{SP}) has been also evaluated, which will have the following values: $\kappa = 1$ (absence of oxide material), 3.9 (SiO_2), 9 (Al_2O_3) and 25 (HfO_2) [17] and $W_{SP} = 2$ nm, 5 nm, 10 nm, 20 nm, 40 nm.

The source/drain doping concentration was 10^{20} cm^{-3} (As) and the channel region was 10^{15} cm^{-3} (B). The analysis were performed for gate voltage (V_{GS}) sweep from 0 to 2 V and drain voltages (V_{DS}) of 50 mV and 1 V.

Fig. 1 - Schematic structure of the A) Self-Aligned SOI-FinFET; B) overlapped SOI-FinFET

III. RESULTS AND DISCUSSIONS

Fig. 2 presents the simulated drain current (I_D) behavior as a function of gate bias (V_{GS}) varying the spacer oxide permittivity (κ) and the spacer underlap length (L_{SP}) for self-aligned ($L_{SP}=0$ nm) and overlapped FinFETs with $W_{SP} = 2$ nm, $V_{DS} = 50$ mV (A) and $V_{DS} = 1$ V (B). In the inset of Fig. 2A a good agreement between the experimental and simulated drain current of self-aligned FinFET is presented.

As can be noticed, the L_{SP} increasing results in a strong I_D degradation due to the R_{SD} increasing [14], caused by lower electric field (fringing field) in the underlap region. The I_D reduction is dampened when high κ dielectric is used in the

spacer oxide (underlap region), because it results in a higher intensity of fringing field from the G to the S/D regions and, consequently, a higher current density (smaller R_{SD}) that in turn, causes On-state current (I_{ON}) improvement. Although the I_D variation, the threshold voltage (V_t) remains constant, with value of approximately 0.465 V.

Fig. 2 – Self-aligned FinFET and overlapped FinFETs $I_D \times V_{GS}$, varying κ and L_{SP} for $W_{SP}=2$ nm, (A) $V_{DS}=50$ mV (B) $V_{DS}= 1$ V.

Fig. 3 shows the transconductance (g_m) as a function of the gate voltage for the overlapped FinFET and self-aligned FinFET for low drain bias ($V_{DS}=50$ mV) (A) and high drain voltage ($V_{DS}=1$ V) (B).

Fig. 3 – Self-aligned FinFET and overlapped FinFETs transconductance, varying κ , L_{SP} for $W_{SP}=2$ nm, (A) $V_{DS}=50$ mV (B) $V_{DS}= 1$ V.

As already shown in Fig. 2, the series resistance increasing affects the device current (lower I_D). Knowing that g_m is derivative of I_D , g_m also decreases as longer is the L_{SP} and increases as higher is κ , which means in a current control variation for the same gate voltage bias. In Fig. 3, for both drain bias (50 mV and 1V), the g_m increases with higher κ values due to the better electric field distribution, that improves (reduces) the series resistance, resulting in a drive current improvement. In Fig. 3 (B) an anomaly characterized by two peaks in the transconductance appears. In order to better understand the two g_m peaks, the electron density for a device with $L_{SP} = 10\text{nm}$ in different V_{GS} conditions, is shown in Fig. 4.

In Fig. 4 (A) the electron density has been extracted for gate overdrive voltage (V_{GT}) of 200 mV ($V_{GT} = V_{GS} - V_T$). For this V_{GT} value, it is possible to notice in Fig. 3B that the transconductance is still increasing (it does not reach the first peak). In this situation, it is possible to observe in Fig. 4A that the values of electron density are relatively low when compared with Fig. 4B and Fig. 4C. Besides that, focusing on the underlap region, an even lower electron density is observed when compared with the channel region. Increasing V_{GS} to a value that g_m is near to the first peak ($V_{GS} = 1\text{ V}$), Fig. 4 (B) shows that the inversion charge under the gate is high, but the electron density reduces at least 3 times in the underlap region, showing that there is an inversion layer below the gate, but below the spacer oxide, the Si is only weakly inverted. Thanks to the high electron energy caused by a high drain bias ($V_{DS} = 1\text{ V}$) and, consequently, a strong lateral electric field between S/D, the electrons overcome the R_{SD} in the spacer region, causing the first peak, as previously mentioned.

Finally, at high V_{GS} (1.32 V), Fig. 4 (C) shows the complete inversion of the device channel (L_{CH} and L_{SP}), the V_{GS} increasing resulted in a second inversion in the underlap region and, consequently, the second g_m peak in the plot.

Fig. 4 – Underlapped FinFET cross-section: Electron density with 10nm spacer oxide and $V_{DS} = 1\text{V}$ for (A) $V_{GS} = 670\text{mV}$, (B) 1V and (C) 1.32V.

Considering the strong I_D degradation with L_{SP} increase, the device sensitivity (S_κ) has been calculated by equation 2, considering high and low drain bias (triode/saturation), with $W_{SP} = 2\text{ nm}$ and $V_{GS} = 1.5\text{ V}$, where $I_{D(\kappa=x)}$ is the drive current with different permittivity. It is also considered the underlapped FinFET without any material in the spacer region ($\kappa = 1$) as the reference by calculating S_κ . Fig. 5 shows that for low drain bias (open symbols) the higher the L_{SP} and permittivity, the higher the sensitivity. Although usually the R_{SD} is an undesirable effect, when the device is used as a sensor, the high I_D degradation gives to the transistor a high sensing capacity. However, for high drain bias ($V_{DS}=1\text{V}$) the underlap length plays a role until $L_{SP} = 30\text{ nm}$. For longer underlap, no significant sensitivity variation was obtained due to the higher influence of series resistance for high V_{DS} .

$$S_\kappa(\%) = \frac{|I_{D(\kappa=x)} - I_{D(\kappa=1)}|}{I_{D(\kappa=1)}} \times 100 \quad (2)$$

Fig. 5 – Underlapped FinFET Sensitivity varying κ and L_{SP} for $W_{SP}=2\text{nm}$, $V_{DS} = 50\text{mV}$ and 1V.

Considering the structure with $L_{SP}=50\text{nm}$, an evaluation of the influence of the spacer oxide thickness (W_{SP}) and permittivity (κ) on drain current level has been also performed. Fig. 6 shows I_D increment by increasing the W_{SP} and κ . As the underlap oxide width grows, the electric field lines distribution improves (higher fringing field intensity) in the underlap region, which promotes a better channel inversion and, therefore, the drive current increasing. It stands out when a higher κ is used, making the fringing field better distributed in the spacer region.

Fig. 6 – Self-aligned FinFET and underlapped FinFETs $I_D V_{GS}$ varying W_{SP} for (A) $\kappa = 3.9$ (B) $\kappa = 25$.

To take a step further, after all characteristics presented in this work, mainly the good sensitivity of the studied device and also the reported SOI-FinFETs hardness to TID effects exposure [9], the underlapped FinFET with longer underlap region ($L_{SP} = 50$ nm) has been considered to evaluate its charges sensing ability. For that, fixed charges density (Q_{OX}) with 10^{11} , 5×10^{11} and 10^{12} cm^{-2} carrier concentration have been considered in the underlap region and compared with the pre-irradiated transistor ($Q_{OX} = 0$ cm^{-2}). Fig. 7 presents the $I_D V_{GS}$ for different W_{SP} (2 and 40 nm). In Fig. 7 (A), despite the low On-state current caused by the high series resistance, when the oxide charges are considered, the potential increasing in the underlap region causes a better inversion layer, which counteracts the R_{SD} effect, resulting in an I_{ON} enhancement. In Fig. 7 (B), the W_{SP} increasing makes the I_D variation with charges to be smaller. This fact is explained by two factors: as larger is W_{SP} , the fringing field lines become better distributed into the spacer region, improving I_D ; and, when it was considered the fixed charges in the spacer oxide, the surface potential becomes high enough to strong invert most of the channel region, overcoming the R_{SD} impact for both $V_{DS} = 50$ mV and 1V.

The sensitivity with the charge accumulation variation (S_{OX}) is calculated by equation 3, that represents the device after ($Q_{OX} = x$ cm^{-2}) and before ($Q_{OX} = 0$ cm^{-2}) proton irradiation, where x is the different charge density.

$$S_{OX}(\%) = \frac{|I_{D(Q_{OX}=x)} - I_{D(Q_{OX}=0)}|}{I_{D(Q_{OX}=0)}} \times 100 \quad (3)$$

Fig. 7 – Underlapped FinFETs $I_D V_{GS}$, varying Q_{OX} for (A) $W_{SP} = 2$ nm (B) $W_{SP} = 40$ nm

Fig. 8 shows that the higher the charge concentration, the better is the sensitivity found. However, when the comparison is between the obtained results for pre and post irradiation, as W_{SP} has been increasing, the sensitivity decreased very sharp, reaching small values of current variation (4% for $\kappa = 25$, $W_{SP} = 40$ nm). In this case, the structure of $W_{SP} = 2$ nm and $\kappa = 25$ stood out for its excellent performance when applied the fixed charges, reaching 92% rate of I_D increasing.

Fig. 8 – Underlapped FinFETs Sensitivity, varying Q_{OX} and W_{SP} for $\kappa = 25$ and $L_{SP} = 50$ nm

Analyzing the sensitivity in Fig. 9 for structures with $W_{SP} = 2 \text{ nm}$ and 20 nm and varying the permittivity, it has noticed that transistors with smaller W_{SP} tend to be the best radiation sensing structure, as already mentioned in Fig. 8. However, there was also a considerable sensitivity increase when using low κ permittivity, reaching values of 130% I_D improvement if compared to the same pre-irradiated device. It is also possible to notice that the impact of W_{SP} is to much higher than the κ influence on transistor sensitivity.

Fig. 9 –Underlapped FinFETs Sensitivity, varying Q_{OX} , k and W_{SP} for $L_{SP}=50\text{nm}$.

Knowing that $W_{SP} = 2 \text{ nm}$ had the best charge sensitivity, considering Q_{OX} , it has been analyzed the L_{SP} variation for $\kappa = 3.9$ and $\kappa = 25$, as shown in Fig. 10. The results show that there is an exponential growth of the sensitivity by increasing the spacer region length, mainly considering high charge density ($Q_{OX}=5 \times 10^{11}$ and 1×10^{12}). With values that reaches 138% ($\kappa = 25$) and 190% ($\kappa = 3.9$) of I_D variation for $W_{SP} = 2 \text{ nm}$ and $V_{DS} = 1 \text{ V}$.

Fig. 10 –Underlapped FinFETs Sensitivity, varying L_{SP} and Q_{OX} for $L_{SP}=50\text{nm}$, $\kappa=25$ and $\kappa=3.9$.

Considering only the drain current (I_D) variation for the same device pre and post irradiation, that means only one device for sensing, the device with narrow underlap oxide region ($W_{SP}=2\text{nm}$) and low permittivity (for example $\kappa=3.9$) had been chosen being the best transistor for irradiation sensing purpose.

However, when a slightly more complex circuit for sensing radiation through trapped charges is considered, comparator circuits that use the device without material in the spacer region as a reference, and another device structure with $L_{SP}=50\text{nm}$, $W_{SP}=2\text{nm}$ and $\kappa=25$ also performed a very good sensitivity ($S=161\%$ for $V_{DS}=0.5\text{V}$) as shown in Fig. 11.

Fig. 11 shows the comparison between the post irradiated transistor ($Q_{OX}=1 \times 10^{12}$) with $\kappa=3.9$ and $\kappa=25$ and the devices without oxide material ($\kappa=1$) in the spacer region.

Knowing that devices without oxide material ($\kappa=1$) in the spacer region does not trap charges, for example, the current does not change after radiation, and comparing with devices with different spacer oxide permittivity, the results for $V_{DS}=50\text{mV}$ presents an 161% of I_D improvement for the underlapped FinFET with the highest permittivity ($\kappa=25$), whereas for $\kappa=3.9$ the general sensitivity reached 147%.

Fig. 11 –Underlapped FinFET I_D variation, for $Q_{OX}=1 \times 10^{12}$, $L_{SP}=50\text{nm}$, $\kappa=25$ and $\kappa=3.9$ comparing with $\kappa=1$

Conventional MOSFETs are extremely affected by radiation and it brings a large uncertainty in this kind of application. The studied device applied for radiation sense purpose has a huge advantage if compared with the conventional MOSFET [6] due to its accuracy on the trapped charges measurements associate to the high immunity of SOI technology.

Thereby, from the presented analysis, it is possible to propose the use of the underlapped FinFETs as radiation sensor in two different ways: the first one, it must be used a simple device with long underlap length ($L_{SP}=50\text{nm}$), small spacer width ($W_{SP}=2\text{nm}$) and low permittivity (for example SiO_2 - $\kappa=3.9$) in the spacer oxide. This structure presented a very good sensitivity when comparing the I_{ON} before and after radiation. In the second way, it must be used two different devices structures, where one would be the underlapped FinFET without spacer oxide ($\kappa=1$) and another one, the transistor with the highest sensitivity if compared its response with the first device ($\kappa=1$). In this case, the transistor that presents the best sensitivity when compared with the reference device would be the underlapped FinFET with the same $L_{SP} = 50\text{nm}$ and $W_{SP} = 2 \text{ nm}$, however with $\kappa=25$.

CONCLUSIONS

Underlapped SOI-FinFET has been evaluated by changing its structure width and length of the spacer region, as well as the spacer oxide permittivity aiming to use the behavior of series resistance and the On-state current degradation to choose the best device for a sensing purpose.

From the characteristics of the spacer oxide and the behavior of the devices before and after proton irradiation (trapped charges), it has been observed that the underlapped FinFET with 50nm of underlap length and 2nm of underlap thickness showed to have the best characteristics for application as radiation sensors. However, the choice of the spacer oxide type depends on the type of the sensor that it will be applied. If only one transistor is considered, comparing its drain current before and after radiation, then the oxide with the lowest permittivity ($\kappa = 3.9$) showed the best sensing capacity (highest sensitivity), while if the sensing strategy uses comparator circuits that have as a reference signal the underlapped FinFET without material in the spacer region, so the best choice is the device with high permittivity spacer oxide ($\kappa=25$).

Independent on the sensor choice, the present study confirms the outstanding underlapped FinFET behavior for radiation sensing purpose, bringing up a vast field of researches for many kinds of application for the society's needs.

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