A 59 pA/V and 62 nW Differential OTA with 0.35% THD for Biomedical Applications

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Abstract— This paper presents a novel differential pA/V Operational Transconductance Amplifier (OTA) topology. The circuit is suitable for the implementation of fully integrated operational transconductance amplifier-capacitance (OTA-C) filters with small feature size capacitors, suited for electrophysiological signal acquisition and conditioning. Unlike typical OTA-Cs, the proposed topology consists of transconductance reduction technique based on unbalanced output branches that allow current subtraction thus enabling transconductances in the order of pA/V. The technique is demonstrated through the design of a 59 pA/V transconductor, which is very suited for designing large time-constant filters. This OTA-C achieved a worst-case 0.35% THD with just 61.7nW average power consumption, which allows its applicability to biomedical implants. Simulations were carried out with STMicroelectronics 0.13 μm HCMOS9 node using Cadence's IC design tools. We employed the OTA in a design of a fourth-order bandpass filter with a narrow bandwidth of 13.5–21.8 Hz. Similar results to the ideal transfer function, turn the proposed OTA ideal for biosensing-based applications.

Index Terms— Analog design; OTA; G_m reduction; OTA-C.

I. INTRODUCTION

The conditioning of electrophysiological signals, such as for the electrocardiogram (ECG), electroencephalogram (EEG), and other bio-signals require high-selective filters to eliminate intrinsic noise proceeding from signal acquisition by biomedical implants [1] or bio-sensing. Those filters like the illustrated in Fig. 1 are also obligatory for new biomedical trends in analog-front ends (AFE), such as retinal or vision prosthesis [2, 3], neurostimulators [4, 5], and seizure or neural anomalies detection systems [6, 7]. All these bio-signals have an inherent baseline (wander and DC) and a high-frequency noise, which is common to both implants (invasive) and wearable (non-invasive).

An important issue in the implementation of such large time-constant filters is the requirement of big capacitances, in the order of dozens to hundreds of pF. These capacitance magnitudes cannot be accommodated within integrated silicon die, which is often limited to a few square millimeters of area. The most widely used approaches for avoiding large capacitances when implementing integrated filters with ultra-large time-constant are either pseudo-resistors [8–11] or transconductance-C blocks [12–14]. The former approach proposed in [8–10] considerably suffers from its sensitivity to bias conditions, and hence, low linearity and high harmonic distortion. In [11], it is proposed a solution for these

Fig. 1: Typical ECG acquisition in biomedical applications.

drawbacks by designing a new biasing circuit. Nevertheless, the pseudo-resistor is the same topology as previously mentioned versions, besides, the extra circuit significantly increases the circuit's complexity, and area in order to provide a good matching targeting reduced process sensitivity. On the other hand, OTA-C can mitigate the demand for the area by significantly reducing the size of the required capacitance. There is a wide list of techniques in the literature, that makes it possible to achieve transconductances in the range of pA/V. Some examples include, bulk-driven inputs [15, 16], drain-driven input [14], current division [17], floating gate structures [17], current steering [18], low-ratio current-mirroring [19], adaptive biasing [20], and G_m cancellation [21]. Most of the above-cited methods are based on a MOS transconductance (gate transconductance, g_m , or bulk transconductance, g_{mb}) to convert the input voltage into a current signal [22].

The main contribution of this work is to introduce a new technique suited for the implementation of circuits with very large time constants. The principle underlying the transconductance reduction consists of creating slightly different copies of input currents from a differential pair and subtracting them at the output node, so as almost to cancel each other out. Two challenges arise in realizing this method: a) precisely setting the two currents under subtraction, and b) overcoming the severe gain reduction due to low output current. A feasible solution to both problems is proposed by Arnaud et al. [19], who introduced enhanced current mirrors implemented with series-parallel associations of transistors [23]. The adoption of trapezoidal transistors in a current mirror has proven to both reduce mirroring ratio error and increasing voltage gain, because of a higher output resistance [23]. Those features are particularly welcome for technologies below 130nm, that exhibit low voltage gains due to the effects of halo implants [24]. The proposed technique is demonstrated in a pA/V transconductor with small capacitors size, which also exhibits low total harmonic distortion (THD), low power consumption, and moderated CMRR. These features

Fig. 2: Proposed differential transconductor topology. (a) Block diagram of the proposed technique. The grey OTA block represents the following circuits in (b): ① tail current source, ② active source-degeneration transistors, ③ the PMOS differential input pair, and ④ two identical transistor associations (current mirrors' inputs). This input section is shared by the output branches identified as ⑤ and ⑥, which comprise the current-mirror factors, k_1 and k_2 and output conductances g_{o1} and g_{o2} depicted in (a).

allow implementing a range of essential blocks for front-end circuitry, such as high time constant filters. The paper is organized into five sections. Section II gives a description and analysis of the proposed technique. Section III presents typical and Monte-Carlo simulations in order to validate the new transconductor. In Section IV, we present an application of our circuit in a fully integrated fourth-order bandpass filter which is applied in the filtering of a raw data stream electrocardiogram (ECG) signal.

II. CIRCUIT TOPOLOGY AND ANALYSIS

A. Transconductance reduction through current subtraction

The proposed concept for the current subtraction technique is depicted in Fig. 2 (a). The main goal is to reduce the transconductance G_m , which is the ratio between the small-signal output current i_o and the small-signal input voltage, $v_i = (V_{inP} - V_{inN})$. Unlike [21] in which transistors are performing in strong inversion and the current subtraction is done in the input differential pair, in this work the reduction is achieved by subtracting two slightly different output currents ($i_o = i_{o1} - i_{o2}$), copied from a common input differential pair through unbalanced current-mirrors. This current subtraction task is precisely controlled by adopting advanced current mirrors [19, 23], which comprises the use of series-parallel transistor associations in place of individual devices and a careful definition of the number of their constituent elements. The resulting transconductance can be estimated, according to (1).

$$G_m = \frac{i_o}{v_i} = g_{m1} - g_{m2} = \frac{g_{m1} - g_{m2}}{g_{m1}} g_{m1} = \alpha g_{m1}. \quad (1)$$

Where $g_{m1} = (i_{o1} / v_i)$ and $g_{m2} = (i_{o2} / v_i)$ are slightly different due to the imbalance between i_{o1} and i_{o2} , the transcon-

ductance attenuation can be represented by a factor α with respect to g_{m1} . Due to the topological differences between associations (see Appendix for more details) adopted in the implementation of current mirrors' output branches (M_{R9} - M_{T2} and M_{R10} - M_{T1}), the overall output conductance is hence dominated by g_{o1} . Consequently, the voltage gain (A_v) of the proposed OTA can be estimated as shown in (2), which is also attenuated by α . From (1) and (2), we can conclude that there is a tradeoff between transconductance and voltage gain.

$$A_v = \frac{g_{m1} - g_{m2}}{g_{o1} + g_{o2}} \approx \alpha \frac{g_{m1}}{g_{o1}}. \quad (2)$$

B. Proposed OTA

The block diagram in Fig. 2 (a) illustrates the concept of transconductance reduction, and Fig. 2 (b) details each part of the circuit. Parts indicated as ①, ② and ③ make up the input stage of the circuit, and ④ is the input of current-mirrors that copy small-signal effect from input pair into the output node. Each current mirror has two different outputs which are part of output branches identified as ⑤ and ⑥. While each transistor is depicted as a single entity in this schematic, they are actually implemented as rectangular or trapezoidal associations of transistors [25–27]. The basic constructive difference between a rectangular and trapezoidal association is that the second always has the transistor connected to the drain terminal wider than the transistor connected to the source terminal, which makes its output conductance smaller than the one from a rectangular association with similar size and biasing condition [26]. For the sake of simplicity, we use M_{Ri} and M_{Ti} to identify rectangular and trapezoidal associations, respectively. According to [26], the adoption of series-parallel associations usually

Fig. 3: Monte-Carlo analysis for mismatch and process. In this evaluation, we verify the impact of alpha value, as also the individual size of transistors on the transconductances g_{m1} and g_{m2} . The difference between the green and cyan curves is the area occupied by the transistors, i.e., $W/L = 0.5\mu\text{m}/0.94\mu\text{m}$ and $W/L = 1.15\mu\text{m}/2.15\mu\text{m}$, respectively. Still in this analysis, note that the cyan curve has smaller variability than the green one, which the fact is due to the bigger area used in individual transistors sizes. Besides, the same aspect ratio was used for building the configurations related to the orange, and purple curves, differing the number of transistors into the trapezoidal branch as can be observed in the right diagram. The black curve corresponds to the transconductance of G_{m1} which only has the rectangular branch.

improves transistor matching, output conductance, and immunity against process variations (particularly to threshold voltages). It also increases the common-mode rejection ratio (CMRR), while it is reported to improve transconductance linearity [20, 28, 29]. The two types of series-parallel associations employed in this work (rectangular and trapezoidal) are detailed in Appendix - Transistors Associations. The appendix also includes the necessary information to understand the details of transistors sizing and layout, given in Table I.

The circuit operation can be understood as follows: the input stage consists of a PMOS differential pair (M_{R5-6}), a tail current source (M_{R1} and M_{R2}), an active source-degeneration (M_{R3} and M_{R4}), and the input devices (M_{R7} and M_{R8}) of the two above-mentioned current mirrors, which constitute a passive load for the differential pair. In order to force the degeneration-transistors (M_{R3} and M_{R4}) to operate in the linear region, their aspect ratios (S_{R3} , S_{R4}) must be kept at least four times smaller than those from the input differential pair (M_{R5} and M_{R6}) [20]. Thus, two different attenuated copies (i_{o1} and i_{o2}) are generated at M_{R9}/M_{T2} from i_{inP} , and at M_{R10}/M_{T1} from i_{inN} , respectively. The current attenuation in each current mirror can be identified by the current factors $k_1 = i_{o1}/i_{in}$ and $k_2 = i_{o2}/i_{in}$.

In (3a) and (3b) current-factors k_i are defined in terms of aspect ratios ($S_i = W_i/L_i$), where W_i and L_i are the equivalent channel width and length of transistor M_i .

$$k_1 = \frac{S_{R9}}{S_{R7}} = \frac{S_{R10}}{S_{R8}}, \quad (3a) \quad k_2 = \frac{S_{T1}}{S_{R7}} = \frac{S_{T2}}{S_{R8}}, \quad (3b)$$

The output current signal can be computed as

$$i_o = 2(i_{o1} - i_{o2}) = 2\left(1 - \frac{k_2}{k_1}\right)i_{o1} = 2\alpha i_{o1}, \quad (4)$$

where the i_{o1} and i_{o2} are the output currents of ⑤ and ⑥, respectively. Details of values for parameters such as aspect

ratios (S_i) and how they are calculated are provided in Table I and the Appendix.

From (1) to (4), the reader can conclude that both the gain and the transconductance can be adjusted by choosing the geometric parameters of the transistors used in the current mirrors.

The setting of parameters can be understood with the help of Fig. 3, which shows the effect of increasing the number of transistors in the drain terminal of the trapezoidal associations (M_{T3} and M_{T4}) on their g_m , and consequently on alpha. As the rectangular transistor has a fixed area, the modulation of the overall transconductance as a function of alpha is changed by adding more transistors in the drain terminal of the trapezoidal association. It can be seen that each new self-cascode association included into M_D , represented by the highlighted devices in cyan, orange and purple, moves the average value of g_m , represented by dot-dashed normal curves with corresponding colors, towards that of the rectangular association M_{R11} and M_{R12} (solid black line).

Still, in Fig. 3, one can observe the effect of increasing the active area (W.L) of individual devices that make up trapezoidal association, on the leftmost normal curve. As predicted by Pelgrom's law [30], the mismatch is nearly halved when increasing four times the active area of unitary transistors. Those relations between individual device areas, number of devices composing M_D , and differences between transconductances have paramount importance for the proposed technique. They define the limit for the overall g_m reduction trades off with silicon area.

For our design case, whose transistor sizes are shown in Table I, the minimum reduction given by $\alpha=0.032$, is limited by M_T and M_R tolerances (assuming 3σ). The limit is represented by the black and the purple bell curves in Fig. 3. By further accreting devices into M_T , curves will increasingly overlap, thus raising the number of fabricated transconductors with overall negative g_m .

Table I.: Transistors sizes

Transistor	Type	(N_{PD}/N_{SD})	(N_{PS}/N_{SS})	(N_P/N_S)	(W_u/L_u)	$(W/L)_{eq}$
$M_{R1,R2,R15,R24,R25}$	PMOS	-	-	32/2	1.15/2.15	8.558
$M_{R3,R4}$	PMOS	-	-	2/1	4/10	0.8
$M_{R5,R6,R26,R27}$	PMOS	-	-	8/1	4/10	3.2
$M_{R12,R13,R14}$	PMOS	-	-	4/16	1.15/2.15	0.134
$M_{R16,R17,R18,R19}$	PMOS	-	-	4/16	1.15/2.15	0.134
$M_{R33,R34,R35}$	PMOS	-	-	4/16	1.15/2.15	0.134
$M_{T4,T5,T6,T10,T11,T12}$	PMOS	8/4	4/16	-	1.15/2.15	0.118
$M_{T4,T5,T6,T10,T11,T12}$	PMOS	16/4	4/16	-	1.15/2.15	0.125
$M_{T4,T5,T6,T10,T11,T12}$	PMOS	32/4	4/16	-	1.15/2.15	0.129
$M_{R9,R10,R11}$	NMOS	-	-	4/16	4/4	0.25
$M_{R7,R8,R28,R29}$	NMOS	-	-	32/2	4/4	16
$M_{R20,R21,R22,R23}$	NMOS	-	-	4/16	4/4	0.25
$M_{R30,R31,R32}$	NMOS	-	-	4/16	4/4	0.25
$M_{T1,T2,T3,T7,T8,T9}$	NMOS	8/4	4/16	-	4/4	0.222
$M_{T1,T2,T3,T7,T8,T9}$	NMOS	16/4	4/16	-	4/4	0.235
$M_{T1,T2,T3,T7,T8,T9}$	NMOS	32/4	4/16	-	4/4	0.242

Trapezoidal associations consist of a series association of two blocks: M_D is an array of N_{PD} parallel connections of N_{SD} minimum-sized series associated PMOS, and M_S is a similar arrangement made of N_{PS} associations of N_{SS} series-connected NMOS. The gate terminal of the trapezoidal device is connected to all individual gates, the main drain goes to drains of uppermost PMOS devices in M_D , and the source is connected to all sources of bottom-most NMOS in M_S . For more details about trapezoidal transistors, see Fig. 10 in the Appendix.

As well as the other transconductance reduction techniques [15, 16, 19, 28], our proposed current-subtraction technique is limited by the sensitivity to process variability, more specifically to transistor mismatch, but it is important to mention that in our proposed technique it is possible to know the limits, as opposed to pseudo-resistor-based schemes. As the main goal is to achieve a very small transconductance from unbalanced current mirrors, an excessive transconductance mismatch can cause not only a frequency deviation but can result in a transconductance phase inversion (a positive transconductance turns negative as the positive and negative). In the worst case, i.e., a phase inversion would turn negative feedback into a positive one, which could cause instability, making a filter design infeasible. For example, a bandpass filter would not only have a different center frequency but could have more attenuation than the design. Hence, the transistors should be increased in size as much as possible, by respecting the increase of the parasitic capacitance and the technology constraints.

In our technique, the input circuit of Fig. 2 (a) (grey highlighted OTA) and the bias circuit, define the basic transconductance of the new topology. By supposing a perfectly matching between the transistors, M_{R3-4} , M_{R5-6} , and neglecting the body and channel length modulation effects, the output currents (i_{nN} and i_{nP}) of the transconductor shown in gray (see Fig. 2) are given by

$$i_{nN(P)} = \frac{\sqrt{2} \beta_{R5} I_{bias}}{\Phi} v_i \sqrt{1 - \frac{\beta_{R5} v_i^2}{\Phi^2 I_{bias}}}, \quad (5)$$

where β_i is M_i technological transconductance parameter [15] given by

$$\beta = \mu \cdot C_{ox}, \quad (6)$$

where μ , C_{ox} are the average mobility of the carriers in the channel, and the oxide capacitance per unit area of the transistor's gate, respectively. The parameter Φ is related to the transconductance ratio by the transistors in the input differential pair and the active degenerative source transistors, which is given by

$$\Phi = 1 + \frac{\beta_{R5}}{4 \beta_{R3}}. \quad (7)$$

According to [20, 28], the square root terms are usually made smaller than unity which takes an increase in linearity and input dynamic range. On the other hand, this increased linearity reflects in smaller equivalent transconductances, keeping the bandwidth and noise features similar to a simple input differential pair. The minimum input voltage necessary for the linearization scheme to work well is given by

$$|v_i| > \sqrt{\frac{4 I_{bias}}{\beta_{R5}}} \frac{\Phi}{\sqrt{1 - 2\Phi + 2\Phi^2}}, \quad (8a)$$

$$i_{nN(P)} = \left(\frac{v_i \sqrt{\beta_{R5} (4\Phi - 2) + \sqrt{(8\Phi - 2) I_{bias} - \beta_{R5} v_i^2}}}{4\Phi - 1} \right)^2. \quad (8b)$$

From the analysis of 8a, when the input voltage has a value upper or lower to the rightmost expression of (8a), one of those degeneration transistors, M_{R3-4} enters in strong inversion and the other not, hence, the output current can be approximate by (8b). We can conclude that the input differential pair biasing and transistor's channel inversion level defines the minimum supply voltage, nominal transconductance, and area, such as proposed by [20, 28].

Fig. 4: Bias circuit and OTA for offset voltage reduction.

Input offset voltage and flicker noise are limited by the active area of input devices (M_{R5} and M_{R6}). Considering a fixed biasing current, if the aspect ratio of input pair transistors is increased, the inversion level decreases, thus leading linearity to decrease [29]. For a very low inversion level, the transistor length and resulting area tend to be very large. If we consider an integrated filter design, large transistors exhibit less mismatch but also increase the parasitic load capacitance, which could be in the same range of magnitude of filter capacitors (the filter cutoff frequencies should not be defined by parasitic capacitance unless it is part of the design itself). This leads to the conclusion that an OTA project should minimize mismatch, without significantly increasing the parasitic capacitance, as this may change the pole frequencies of the designed OTA-C filter.

The other important parameter is the common-mode rejection ratio (CMRR) which is defined by non-idealities of the OTA current sources. In our circuit, a high CMRR is achieved by using cascode current sources, which, on the other hand, reduces input voltage swing and increases the minimum supply voltage. In our circuit, the nominal transconductance is limited by the linearity constraints of the differential input pair, such as [19]. The output transconductance is a function of the mirroring ratio (parallel-series and parallel-trapezoidal), such as [19] and our proposed technique, i.e. current subtraction from the unbalanced current mirrors.

C. Biasing circuit

In our proposed topology, besides the highlighted gray OTA (see Fig. 2 (a)), the transconductance also is defined by the biasing current shown in Fig. 4.

Fig. 4 (b) illustrates the circuit which provides all biasing voltages (V_{bp1} , V_{bp2} and V_{bn1}) and controls the DC offset at the transconductor output (V_O). The offset control strategy relies on using the bias circuit as a common-mode feedforward block (CMFFB) to the transconductor (Fig. 2 (b)). The concept is illustrated in Fig. 4 (a). The bias circuit consists of two bootstrapped cascode current mirrors ⑧ driven by a current reference (I_{bias}) ⑦, and a common-mode feedback circuit (CMFBC) which is almost a replica of the transconductor, except for the diode connections in M_{R32} and M_{T9} ,

not present at M_{R11} and M_{T3} .

The voltage drop V_{bp1} , caused by flowing I_{bias} through M_{R15} , allows for all of biasing currents in the transconductor to be set through this reference. A feedback loop is established by using V_{bp2} to control output cascode transistors (M_{R33} and M_{T10}) and by applying the output voltage (V_{bn1}) back into the gates of M_{R20-21} . Notice that currents and voltage drops in the output cascode current sources of ⑨ (M_{R31-34} and M_{T8-11}) are jointly defined by I_{bias} and the common-mode input voltage.

III. SIMULATION RESULTS

The circuit performance was evaluated through typical and 500 runs of process and mismatch Monte-Carlo (MC) post-layout simulations. Our design used the 130 nm HCMOS9 node process by STMicroelectronics using Cadence Virtuoso®. In Table I, the implementation of each transistor is detailed in terms of the device number of each association, and the corresponding equivalent transistors aspect ratio. Main performance metrics for OTAs are adopted to evaluate the proposed circuit: transconductance (g_m), voltage gain (A_v), dynamic power consumption (P), total harmonic distortion (THD), common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR).

Results for typical cases are shown in Fig. 5 and summarized in Table II. As can be seen in these results, the adoption of the proposed current subtraction method led to a transconductance reduction of approximately 37 times concerning an OTA using self-cascode current mirrors, i.e. $g_m \approx g_{m1}/37$. As suggested by Fig. (3), transconductance could be further decreased by reducing the standard deviation of currents, at the cost of more silicon area. Moreover, (g_m) reduction came at the cost of increasing the THD, while other features remained nearly unchanged. Still in Table II, it is possible to observe that the bandwidth obtained by the new topology allows the implementation of fully integrated filters by using small capacitors without committing a lot of silicon area, which is very hard to achieve with classical topologies.

Still evaluating the simulation results also it is possible to observe that the unavoidable drawbacks of the proposed OTA are relatively poor voltage gain and PSRR. The decreased gain is due to the drastic reduction of output current. As

Table II.: Summarized results of proposed OTA

Parameters	G_{m1}	G_m , $\alpha=0.112$	G_m , $\alpha=0.06$	G_m , $\alpha=0.032$
g_m [pA/V]	-2192	-240.8	-121.7	-59.22
i_o [pA]	-0.374	-0.726	-0.720	-0.710
A_v [dB]	54.3	29.4	23.4	17.2
P [nW]	60.89	61.68	61.73	61.75
BW [Hz]	1.508	1.195	0.9244	0.6316
GBW [Hz]	115.3	12.75	6.402	2.885
IRN [nV/ $\sqrt{\text{Hz}}$]	2.3	339	1350	5690
THD [%]	0.03	0.08	0.18	0.35
CMRR [dB]	107.7	79.5	74.3	69.5
PSRR [dB]	57.7	32.7	26.7	20.5

$V_{DD}=1.2$ V, $I_{bias}=10$ nA, i_o computed for $V_{in-DC}=600$ mV. Using the integrator configuration, the OTA was analyzed with respect of voltage gain (A_v), bandwidth (BW), common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR). The total harmonic distortion (THD) was computed with the proposed OTA in unitary buffer configuration and used other OTA as a load with a capacitor of 0.8 pF, besides, an input-signal with the follow characteristics $V_{in}=100$ mV_{pp} and 100 mHz.

we have shown, the output current results from a subtraction between two nearly equal currents, whose difference is set by the number of parallel elements (N_{SD}) in the trapezoidal transistor associations, since the rectangular associations are kept fixed (see Appendix for more details). The higher the number of parallel transistors (N_{SD}) in the drain of trapezoidal association, the smaller is the difference between the unbalanced mirrors, i.e. α achieves lower values. As an advantage over pseudo-resistors that suffer from high variation with the manufacturing process, our technique allows designers to adopt different trapezoidal and rectangular configurations in the output stages in order to control both gain and transconductance according to the application requirements. In order to estimate the area of the proposed OTA by using the minimum value of alpha, i.e., the lowest value of transconductance allowed by the new topology in the technology used, its layout is shown in Fig. 6.

As our proposed technique aims to reduce the transconductance g_m , by subtracting two slightly different output currents ($i_o=i_{o1}-i_{o2}$), copied from a common input differential pair through unbalanced current-mirrors, hence this scheme should guarantee that one branch always has output conductance higher than the other in order to reduce the overall transconductance. Hence the mismatch between the output mirrors should be kept controlled since our technique relies on its unbalanced currents. Consequently, if one branch becomes more conductive than the other, the transconductance signal can invert which represents a sum of currents and an increase of g_m . Simulations were executed 500 times by evaluating mismatch and process variation. The main tested parameters are transconductance and voltage gain. From Monte-Carlo (MC) analysis, the extreme cases are presented in Fig. 7.

According to the Fig. 7 the proposed topology achieved

Fig. 5: Simulation results for the typical cases of standard symmetrical topology (G_{m1}), and proposed OTA (G_m). (a) Transconductances, (b) zoomed-in view of transconductances, (c) output currents, (d) zoomed-in view of the output currents, (e) voltage gain, (f) CMRR, and (g) input-referred noise. Note the linearity of 150 mV in the transconductance feature. Note that the good symmetry observed in transconductance and output currents is due to the high CMRR achieved by the new OTA topology.

$\sigma/\mu=8\%-31.17\%$ and $\sigma/\mu=2.27\%-37.46\%$ for transconductance and voltage gain, respectively. Moreover, these results illustrate the limits of the proposed technique by using this 0.13 μm CMOS process. The evaluated parameters are strongly dependent on the technology employed in the transistors manufacture and the layout techniques used in the circuit since the CV relies on the mismatch and process variation features. These results represent the best and worst cases in terms of coefficient of variation (CV).

In Table III most common OTA performance figures obtained with our technique are compared with other g_m reduction topologies found in the literature. Post-layout simulation results evince that the technique proposed in this work provided a balanced performance regarding power consumption, silicon area, transconductance reduction, and THD. Moreover, the high CMRR, low frequency, and modest gain

Fig. 6: Layout of the proposed OTA for $\alpha=0.032$. The area occupied by the circuit corresponded to 400 μm x 188 μm .

Fig. 7: Evaluation of the proposed circuit by mismatch, process, and temperature variation. By 500 runs of Monte-Carlo analysis for (a) transconductance of G_m , $\alpha = 0.112$, (b) voltage gain of G_m , $\alpha=0.112$, (c) transconductance of G_m , $\alpha=0.032$, (d) voltage gain of G_m , $\alpha=0.032$, (e) transconductance in function of process, and (f) transconductance in function of temperature.

achieved through our design allow the implementation of filters with high-time constants, which are very suited to bio-sensing integrated circuits.

IV. BIO-SENSING APPLICATION

Designing filters with large time constants for biomedical applications involve several constraints like area, linearity, and power. The area is the biggest issue since integrated capacitors and resistors require a large area themselves [36]. Usually, an initial estimate is made to define frequencies and maximum allowed capacitors' size. In order to compensate for the eventual filter corner frequency deviation due to process variability, some kind of calibration is needed. The adopted frequency tuning scheme defines what kind of OTA capacitors are chosen. For bias current calibration, the capacitors have a fixed value while the OTA transconductance is variable. For capacitance calibration, digitally trimmed capacitors [37] or varactors can be used instead.

In order to demonstrate the application of the proposed topology, an integrated fourth-order OTA-C bandpass filter (BPF) [38] shown in Fig. 8 (b) was designed and simulated. The BPF uses three OTAs allowing for to set quality factor (Q) and central frequency (f_c). This filter is intended to be building-block of an analog front end (AFE) for identifying QRS complexes from a noisy ECG signal, the system is illustrated in Fig. 8 (a). In this way, the cutoff frequencies were defined in order to remove low noise (baseline wander and DC) and 50-60Hz artifacts, while preserving the features of R-waves whose central frequency content is in 17 Hz [39].

By isolating R-waves, heart rate variability (HRV) can be more reliably measured with the help of simple spike detectors [40]. Furthermore, it is worth mentioning that this type of filter can be applied to other biomedical signals such as

electroencephalogram (EEG: 0.1-70 Hz), electromyography (EMG: 10-500 Hz), Electroneurogram (ENG: 0.2-5 kHz), intracardiac electrograms (IEGM: 0.7-70 Hz), by simply adjusting capacitances.

Each section of the fourth-order OTA-C filter shown in Fig. 8 (b) uses three of the proposed transconductor and two small capacitors of 0.3 and 0.5 pF, for C_1 and C_2 respectively. According to the Monte-Carlo simulations, by taking into account the integrated filter design constraints, we adopted an OTA design with $\alpha=0.112$ due to good area, mismatch and power consumption trade-offs. Moreover, filters applied to ECG signals non require very small frequency corners, consequently higher alpha values can be used. The aspect ratio of unit-size transistors (S_u), voltage supply (V_{DD}) are the same as shown in Table I, with exception to the bias current, $I_{bias} = 16$ nA that was employed to set f_c . The fourth-order transfer function is obtained by cascading by a couple of second-order stages whose transfer function is shown in (9).

$$H(s) = \frac{B s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} = \frac{\frac{g_{m2}}{C_2} s}{s^2 + \frac{g_{m3}}{C_2} s + \frac{g_{m1} g_{m2}}{C_1 C_2}}, \quad (9a)$$

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}, \quad (9b)$$

$$BW = \frac{\omega_0}{Q} = \frac{g_{m3}}{C_2}, \quad (9c)$$

$$Q = \sqrt{\frac{g_{m1} g_{m2} C_2}{C_1 C_2 g_{m3}}}, \quad (9d)$$

$$H(s) = \frac{-76.051410753669s}{s^2 + 91.903317709769s + 10830.52163291}, \quad (9e)$$

where $\omega_0=104.07$ rad/s, $BW=91.9$ Hz and $Q=1.14$.

The feasibility of the proposed OTA on the implementation of fully integrated filters can be observed in Fig. 8, where the simulated transfer function ($H(s)$) is compared to the ideal one. It is possible to notice that simulated $H(s)$ deviates from the ideal above 100 Hz. That stems from significant parasitic capacitances associated with transistors' gate-width inside the associations. This non-ideality rises a relevant concern regarding the design of integrated filters with large time constants. Designers must trade-off between avoiding increasing parasitic capacitances and implementing too-small transistors, that suffers prohibitive mismatch and sensitivity to process variations. Both constraints need to be balanced when defining the magnitude response and pole frequencies. It is important to mention that this deviation would be even larger if the circuit was implemented with single devices rather than associations.

The time-domain response shown in Fig. 9 confirms that main ECG features are preserved after filtering. Another important feature is the low power consumption (494.4 nW), which enables the circuit to wearable or implantable bio-

Fig. 8: (a) Bandpass filter into a system-on-chip applied to the detection of QRS complexes. Comparison between 4th order transfer function $H(s)$, and 4th order OTA-C bandpass filter, (b) Magnitude responses. The narrow poles-frequency of the integrated filter was achieved by using three equal OTAs with $\alpha=0.112$ that allow adjustments in its quality-factor and central frequency. It is possible to observe a magnitude deviation around 100 Hz caused by unavoidable parasitic capacitance inserted by the increase of gate-width of transistors in associations in order to increase the OTA robustness against the mismatch and process variation.

Fig. 9: The transient simulations present the filtering of a stream of ECG data that was applied to the filters; it can be observed that the proposed filter obtained similar results to a fourth-order transfer function filter $H(s)$ 4th BPF and OTA-C BPF in the goal of QRS filtering.

sensing systems.

V. CONCLUSION

We have devised and presented a new technique for transconductance reduction. The concept is proved through post-layout simulation runs of an OTA which achieved as low as 59 pA/V. Thanks to its low transconductance, the circuit allowed the implementation of a fourth-order OTA-C band-pass filter with cutoff frequencies of 13.5–21.8 Hz using capacitors of just 0.3 pF and 0.5 pF. With a power consumption of 494.4 nW, the functionality is demonstrated by streaming raw ECG data. A small distortion (0.35% THD) can be observed on the output when compared with

the same filter built with ideal blocks due to parasitic capacitances. This kind of distortion has a tradeoff with silicon area since parasitics become non-negligible in comparison to designed capacitances. The resulting set of specifications of the presented G_m -C topology is attractive for ultra-low-power biomedical implants.

APPENDIX - TRANSISTORS ASSOCIATIONS

This appendix presents the different types of transistor associations, as well as how to compute their equivalent aspect ratios.

Association of transistors is often used for two main reasons, to solve the intrinsic offset that can be caused by transistor mismatch and process deviation [26] and the low gain achieved by amplifiers [23, 24]. The size of transistors is commonly increased to overcome these problems in technologies older than 130 nm, which results in better tolerance to mismatch and process variation, although increasing the parasitic capacitances. In the newest technologies, which already have higher parasitic capacitances, lower Early-voltages (V_A), this solution can be prohibitive, besides the limited available silicon area. Additionally, the enlargement of the transistor's gate does not improve the gain of amplifiers in the most recent technologies. Hence, the found solution is the association of transistors indifferent configurations [24].

Figures 10 (a), and (b) show the different types of transistor associations, i.e., rectangular and trapezoidal. The primary difference between these associations is that the trapezoidal has the drain transistor wider than the source transistor. Both associations consist of combinations of transistors in series and parallel inside. A rectangular association can be computed with (A-1).

$$S_R = \left(\frac{N_P}{N_S} \right) \cdot S_u. \quad (\text{A-1})$$

Table III.: Comparison with Simulated (S) and Measured (M) Integrator designs

Parameters	This Work (S)	[14] (S)	[31] (M)	[32] (M)	[33] (M)	[8] (S)	[34] (M)	[35] (S)
Supply [V]	1.2	3.3	3.2	0.25	0.3	3.3	1.5	1.5
Process [nm]	130	130	350	130	180	350	800	350
V_{th}	0.5	-	-	0.22	0.5	-	-	-
g_m technique	CS	DD	CD	BD	BD	CD	GG	TR
Power [nW]	61.75	200	-	10	13	5700	230	114
I_{bias} [nA]	10	20	-	10	2.5	14.55	1700	-
A_v [dB]	17.2	0	-	-	33.3	-	0	33.4
g_m [pA/V]	^a 59.2	0.7	3	22000	68000	5	100	1860
BW (-3dB) [Hz]	0.676	0.01	35	-	50	0.0318	0.066	14.8
Capacitor [pF]	0.8	0.8	0.025	20	220	18	70	20
CMRR [dB]	69.5	-	-	-	57	-	-	-
PSRR [dB]	20.5	-	-	-	39.9	-	-	-
THD [%]	^b 0.35	1.7	-	0.53	0.15	-	-	< 1
Area [mm ²]	0.090	-	0.025	0.053	0.035	0.073	0.1	-

CS = Current Subtraction; DD = Drain-Driven; CD = Current Division; BD = Bulk-Driven; GG = g_m^{-1}/g_m chains; TR = Triode region; ^a Absolute value; ^b Buffer configuration, $V_{in}=100$ mV_{pp}, and $f=100$ mHz;

Fig. 10: Different transistors configurations are shown. (a) Rectangular associations have the same size in the drain and source terminal transistors (b) Trapezoidal associations can be divided into two rectangular associations. On the drain terminal of this topology, the number of transistors in parallel is bigger than in the source terminal.

where $S_u=(W/L)_u$ is the aspect ratio of unit-size transistors, N_P and N_S are the number of unit-size transistors in parallel and series, respectively.

The trapezoidal associations were proposed for the first time in [25], and have been used in researches such as in [26, 27]. The original structure consisted of two transistors in the series association, in which the transistor connected to the drain terminal was wider than the transistor connected to the source terminal. Among the advantages of this topology, is that the trapezoidal transistors demonstrate a transconductance-to-output conductance ratio as higher as of a single long-channel transistor, by using shorter physical channel length, which allows area-saving and better matching. Hence, we use the lower output conductance presented by these associations in relation to those rectangular in order to apply our proposed current-subtraction technique.

The trapezoidal transistors are shown in Fig. 10 (b), and the equivalent size of the arrangement can be computed with (A-2).

$$S_T = \frac{\left(\frac{N_{PD}}{N_{SD}}\right) \cdot \left(\frac{N_{PS}}{N_{SS}}\right)}{\left(\frac{N_{PD}}{N_{SD}}\right) + \left(\frac{N_{PS}}{N_{SS}}\right)} \cdot S_u, \quad (A-2)$$

where $S_u=(W/L)_u$ is the aspect ratio of unit-size transis-

tors, N_{PD} and N_{SD} are the number of unit-size transistors in parallel and series in on the drain terminal transistor, and N_{PS} and N_{SS} are the number of unit-size transistors in parallel and series in transistor on the source terminal, respectively.

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