Special Issue on
Intelligent, Energy-Efficient, and Robust Computing Systems
Message of Guest Editors

Over the last half-century, computing systems evolved from costly, bulky, and unconnected machines to omnipresent technology powering an endless variety of connected products, devices, and systems. However, the need for computing systems keeps on increasing at a fast pace boosted by demanding environments and applications that include media processing, machine learning / deep neural networks, blockchains, autonomous vehicles, robotics, healthcare, avionics, and the internet of everything, among many others. Due to their stringent design constraints, these technologies fueled research and development towards designing intelligent, energy-efficient, and robust computing systems.

This Special Issues brings ten invited papers, from the experts of the field across the globe, focusing on different aspects of computing systems design and techniques to cope with the increasing level of complexity and specialization in modern computing systems. The readers will be provided with an extensive literature review followed by valuable insights on the major trends on future computing systems design. In the following, we present a brief description of the papers appearing in this Special Issue.

Caimi, Faccenda, and Moraes discuss security mechanisms for NoC-based many-core systems. The article focuses on the protection of the applications execution or on the access to shared memories whereas identifying the lack of solutions covering the entire application lifetime. Therefore, the authors argue that security for sensitive applications require systemic solutions able to deal with the application admission, computational and communications aspects, and memory and I/O access.

Gobatto, Rodrigues, Saquetti, Cordeiro, and Azambuja motivate for the importance of integrating hardware accelerators with network devices in order to potentialize network performance in the full-connected era. The authors survey in-network computing focusing on the use of hardware accelerators whereas providing a novel intuitive taxonomy. The manuscript brings a set of key challenges that include the definition of abstractions for network function accelerators, translation from Domain Specific Languages to the target hardware architectures, and network hardware visualization.

Santos, Carro, Kepe, Moreira, Cordeiro, Santos, and Alves focus on near-data processing to deal with the high latency and high-energy consumption associated to the data transfer between processor and memory. The authors present a historical perspective and survey near-data processing architectures for applications that feature data streaming behavior and/or coalescent data access. The discussion is carried out following a new taxonomy that classifies near-data processing solutions according to the accelerator placement w.r.t. the memory.

Soldavini and Pilato present a survey on the design of domain-specific memory architectures. Domain-specific architectures are tailored for the given application domain, with the introduction of hardware accelerators and custom memory modules while maintaining a certain level of flexibility. The manuscript discusses the main challenges, trending design methodologies, and main projects in the field. Authors conclude that automatic design methods are mostly immature and the gap between software and hardware designers must be filled in order to facilitate domain-specific memory architectures design.

Sekanina focuses on the design of approximate circuits and programs surveying evolutionary algorithm-based approaches. Evolutionary algorithms are applied as multi-objective optimizers to optimize parameters of approximate systems and to determine their architecture. Since evolutionary algorithms suffer from long execution time, their utilization is typically accompanied by a fitness estimation strategy. The discussion follows a newly proposed classification and covers all relevant design abstractions. The article also presents a discussion on the approximate hardware design for neural networks.

Calazans, Rodolfo, and Sartori focus on asynchronous circuits, particularly quasi-delay insensitive circuits, as an alternative to design robust and energy-efficient systems. After presenting a primer on asynchronous circuits, authors survey robust asynchronous circuit design techniques considering voltage, process, and temperature variations and circuit aging. The manuscript also presents design tools and points to major opened research challenges on asynchronous systems design.

Soares, Lima, Lellis, Finkenauer Jr., and Camargo discuss the design of secure cryptographic circuits focusing on hardware countermeasures against power analysis attacks. Information leakage through side channels has become a concern in digital system design that operates with confidential information. The authors provide a background on power analysis attacks and survey the literature considering both hiding and masking countermeasures. Costs, advantages, and limitations of the countermeasures are discussed in order to support advances in robust systems design.

Palau, Silveira, Domanski, Loose, Cerveira, Sampaio, Palomino, Porto, Corrêa, and Agostini concentrate on the challenges related to high-throughput low-energy hardware systems design for modern video coding. The demand for digital video applications with increased resolution associated to highly complex emerging coding standards poses severe design constraints. The authors survey hardware solutions for each step of modern coding process and highlight the opened research opportunities in the field, especially for AV1 and VVC codecs.

Seto focuses on the design of convolutional neural network (CNN) inference accelerators considering a perspective of system-level optimizations. Special attention is given to loop optimizations and memory access optimizations for nested loops in CNN layers. Based on the literature survey, the author points out key challenges that include providing compilers and design tools for CNN accelerators.

Benevenuti, Kastensmidt, Oliveira, Added, Aguiar, Medina, and Guazzelli discuss robust convolutional neural networks design in SRAM-based FPGAs by presenting a case study in the context of image classification. The authors present background on soft errors and a methodology for qualifying neural networks under faults using emulated fault injection and heavy-ions irradiation. Conclusions advocate that fault injection enhancements are necessary to cover other parts of the FPGA besides the configuration memory, especially memory blocks.

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