

Experimental Analysis of Trade-Off Between Transistor Efficiency and Unit Gain Frequency of Nanosheet NMOSFET down to -100 °C

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Abstract – This work presents a trade-off analysis between transistor efficiency (gm/I_D which is proportional to the intrinsic voltage gain A_v) and the unit gain frequency (f_T) of nanosheet (NSH) NMOS devices for temperatures from room temperature down to -100 °C. The analyses were performed experimentally as a function of the inversion coefficient (IC) in order to determine the optimal application region for optimization of both parameters. These analyses were performed with NSH NMOS for channel lengths of 28 nm, 70 nm and 200 nm. It was observed that the optimal operation point takes place in the transition between moderate and strong inversion (IC=10) for the three analyzed temperatures, where the highest value obtained for $gm/I_D \times f_T$ was found. In this optimum bias point the A_v is 45 dB (L=200 nm) and 39 dB (L=28 nm) and f_T is 9 GHz (L=200 nm) and 186 GHz (L=28nm) both for T=25 °C, which should be suitable for many applications.

Keywords— Nanosheet transistors, inversion coefficient, analog parameters, low temperature.

I. INTRODUCTION

New technologies of transistors have been developed to supply the industry's needs for better performance and efficiency. The nanosheet (NS) transistors were developed to supply these needs for the sub 5 nm technology node (presenting channel length lower than 20 nm). Due to the Gate-All-Around (GAA) structure, these NS transistors present a strong electrostatic coupling between gate and channel, providing a high immunity to parasitic effects such as the short channel effect (SCE) [1].

With the aggressively down-scaled CMOS technology and the new devices structures, the design of analog circuits has become a challenge, since it needs more complex devices models [2]. The complications involved in the CMOS design are related to the three degrees of design freedom that are considered: channel length, channel width and drain current. Aiming a better design optimization these three degrees can be: channel length (easily calculated for layout), drain current and inversion coefficient (IC). The IC is a quantitative measurement which demonstrates all inversion levels of the channel (weak, moderate, and strong) with no dependence on the bias or device's size, which enables a free design at any inversion level [3].

A previous work presented some analog parameters analysis for these devices, as a function of temperature and

for different metal gate stacks [4][5][6]. As a contribution, this work focuses on the analysis of some important analog parameters (transistor efficiency, unit gain frequency and intrinsic voltage gain) and the trade-off between transistor efficiency and unit gain frequency. All these parameters are analyzed as a function of inversion coefficient (IC) for the NMOS nanosheet transistors, where the influence of low temperature was also included. With this study it is possible to present the optimal point of operation of these devices, in terms of analog circuits.

II. DEVICES CHARACTERISTICS

In this work the NMOS lateral nanosheet transistors fabricated at imec, Belgium were analyzed. Each device is composed of two vertically-stacked nanosheets (corresponding to one fin in the device's layout) and twenty-two parallel fins in layout. Each transistor has the following characteristics: channel width (W_{NS}) about 15 nm, channel height (h_{NS}) about 11 nm, effective oxide thickness (EOT) about 0.9 nm, channel lengths (L) of 28 nm, 70 nm and 200 nm, and a metal gate stack thickness of 7.5 nm. Only for the capacitance measurements a device was used with a channel length of approximately 1 μ m. Fig. 1 presents the schematic cross section of a single stacked nanosheet fin.

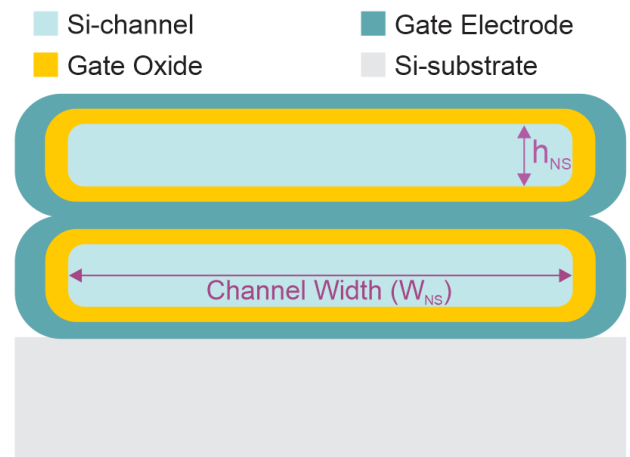


Fig. 1 – Schematic cross section of a stacked nanosheet NMOS transistor.

The measurements were performed for three

temperatures (T): 25 °C, -40 °C and -100 °C, with a gate voltage (V_{GS}) range from -0.5 V up to 1.0 V and a drain voltage (V_{DS}) of 700 mV, operating at the saturation region. Additional characterization is performed with a V_{DS} ranging from 0 V up to 1 V, and an overdrive voltage ($V_{GS} - V_T$ (threshold voltage)) of 200 mV. For all measurements, the substrate was grounded.

III. RESULTS AND DISCUSSION

The first results are the transfer curves, drain current (I_{DS}) as a function of V_{GS} in linear (right-axis) and logarithmic (left-axis) scales, presented in Fig. 2, with $V_{DS}=700$ mV, for the channel lengths of 28 nm and 200 nm, for temperatures from 25°C down to -100 °C (the $L=70$ nm was omitted in this graph to provide a better visibility of the temperature influence).

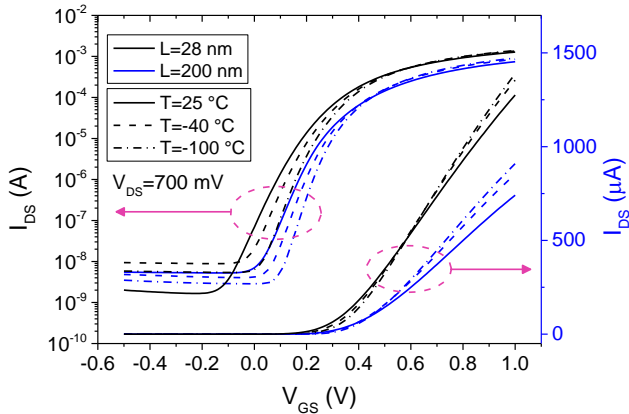


Fig. 2 – Drain current as a function of gate voltage in the saturation region, for $L= 28$ nm and 200 nm, with temperature from 25 °C down to -100 °C.

For longer channels, the I_{DS} level reduces, as predicted by the current equation [7] and it is clearly observed in both scales. When reducing the temperature it reduces the subthreshold slope, since it is directly proportional to temperature, as presented in equation (1) [8]:

$$SS = \frac{kT}{q} \ln(10) * n \quad (1)$$

where k is the Boltzmann constant, q is the elementary electron charge and n is the body factor. In the saturation region the decrease in temperature increases I_{DS} , due to the carrier mobility increase, since the phonon scattering is reduced [9].

The I_{DS} as a function of drain voltage (V_{DS}) is presented in Fig. 3, for $L=28$ nm, 70 nm, and 200 nm for the three temperatures: 25°C, -40 °C and -100 °C, with a gate overdrive voltage (V_{GT}) of 200 mV. The I_{DS} dependency with L is clearly noted (increasing L , I_{DS} reduces), such as the influence of temperature, where the drain current increases due to the carrier mobility increase when reducing the temperature.

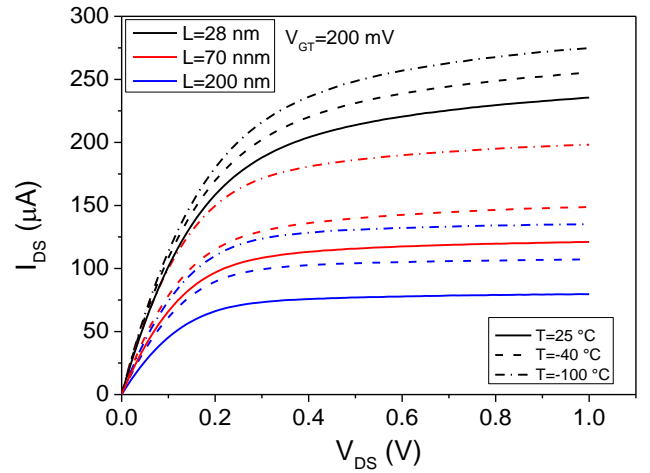


Fig. 3 – Drain current as a function of drain voltage, for different channel lengths and temperatures.

A. Inversion Coefficient

The inversion coefficient (IC) is a parameter that numerically represents the level of inversion in the channel (weak, moderate, and strong inversion). It is denoted as the ratio between the drain current (I_{DS}) and the transition current (I_{DS_t}), which is the current in the transition between weak and strong inversion [3]. In this work the transition current was considered as being the current corresponding to the threshold voltage of each device [10]. With the IC values it is possible to identify the inversion level:

$$\begin{aligned} IC < 0.1 & \rightarrow \text{Weak Inversion (WI)} \\ 0.1 < IC < 10 & \rightarrow \text{Moderate Inversion (MI)} \\ IC > 10 & \rightarrow \text{Strong Inversion (SI)} \end{aligned}$$

The use of IC facilitates the design process enabling a conscious choice of the region and level of operation of a MOS transistor, which allows achieving higher Figures-of-Merit (FoM) for a given design situation [2][3].

B. Trade-offs among analog parameters

In this work three very important design parameters for analog circuits have been analyzed: transistor efficiency (gm/I_D), unit gain frequency (f_T) and intrinsic voltage gain (A_V). All of them are analyzed as a function of the inversion coefficient (IC).

The transistor efficiency (gm/I_D) is presented in Fig. 4-A, for the three channel lengths and temperatures. There is a slight influence of the transistor geometry (for $L=28$ nm) on this parameter when analyzing the three inversion levels, as presented in reference [11], where these devices are barely affected by the short channel effect (SCE). The temperature, however, affects the transistor efficiency mainly in weak inversion, which is a region with a great inverse dependence of the subthreshold swing (that is directly dependent on temperature). When reducing the temperature, the transistor efficiency increases, which is possible to observe for all channel lengths, where the maximum gm/I_D (obtained in weak inversion, $IC < 0.1$) is about 35 V^{-1} at 25 °C, about 41 V^{-1} at -40 °C, and about 48 V^{-1} at -100 °C, for $L=70$ nm. When achieving strong inversion, the transistor efficiency is mainly ruled by the

carrier mobility and the series resistance [12] and, by decreasing the temperature, it tends to reduce while increasing IC, due to the velocity saturation.

The unit gain frequency (f_T) was calculated in this work through equation (2)[13]:

$$f_T = \frac{gm_{sat}}{2\pi C_{gg}} \quad (2)$$

where gm_{sat} is the transconductance when biased at saturation region (in this case, $V_{DS}=700mV$) and C_{gg} is the total gate capacitance. For extracting f_T , the capacitance of a transistor was measured with the same characteristics of the ones analyzed in this work, except for the channel length, that was $L \approx 1 \mu m$, required to provide a high enough transistor area, ensuring a reliable capacitance level for the measurements with the equipment. The capacitance measurement was done at room temperature ($25^\circ C$) with a frequency of 100 kHz and a V_{GS} range from -0.5 V to 1.0 V. Fig. 5 presents the measured capacitance curve.

Fig. 4-B presents the unit gain frequency as a function of IC, where the f_T was calculated through equation 2. The measured C_{gg} curve was normalized by the channel length, being possible to calculate C_{gg} for each device ($L=28$ nm, 70 nm and 200 nm), and then calculate f_T . It was chosen a gate capacitance as a function of V_{GS} , instead a fixed C_L (load capacitance), considering that the load capacitance is a transistor with the same size.

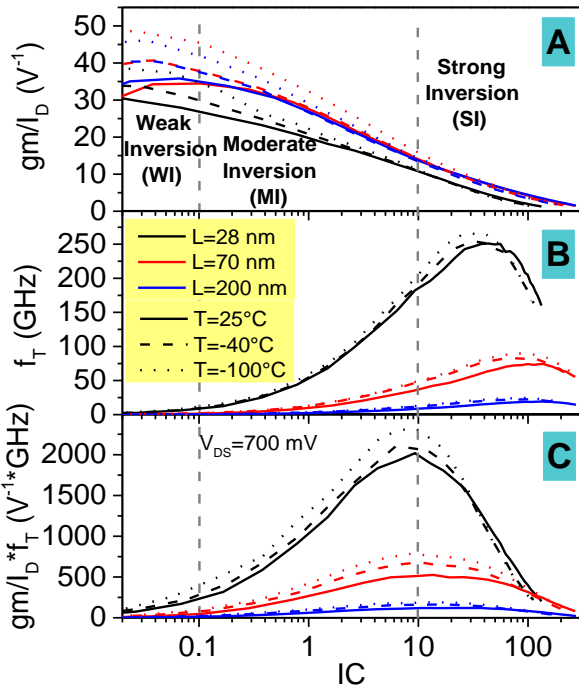


Fig. 4 – (A) Transistor efficiency (gm/I_D), (B) unit gain frequency (f_T) and (C) the product of gm/I_D and f_T as a function of inversion coefficient (IC), for different channel lengths and temperatures.

When increasing IC, the f_T also increases, achieving its maximum value at strong inversion ($IC > 10$). This f_T behavior is associated with the transconductance, which also increases with IC achieving its maximum value at strong inversion, and due to the degradation of velocity saturation [3] after achieving its maximum. The influence

of the channel length is clearly noted in this parameter since it affects gm_{sat} and C_{gg} . The temperature influence is also noticed in this case since it affects the carrier mobility, resulting in a slight f_T increase when temperature reduces.

The trade-off between transistor efficiency and unit gain frequency is very challenging, because while the transistor efficiency characterizes the DC performance, the unit gain frequency characterizes the frequency performance, and these two parameters behave differently when analyzing as a function of the IC levels. In weak inversion ($IC < 0.1$), the transistor efficiency achieves its maximum value (about $32 V^{-1} - 35 V^{-1}$), starting to degrade for higher IC values. Meanwhile the f_T is very low at weak inversion, limiting high frequency analog applications, but when in strong inversion it achieves its maximum value (~ 267 GHz for $L=28$ nm and $T=-100^\circ C$).

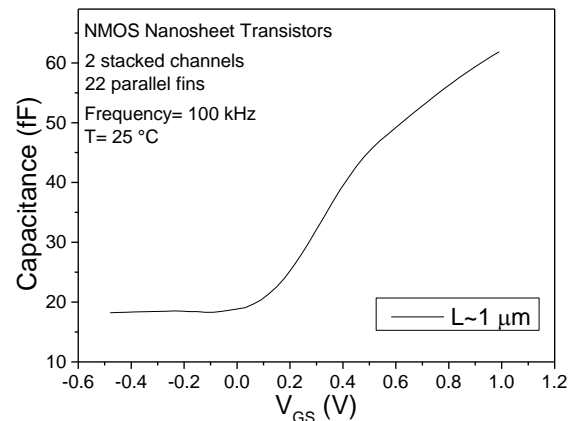


Fig. 5 – Gate capacitance as a function of gate voltage for a gate length of approximately $1 \mu m$.

In terms of design, making a compromise between these two parameters ($gm/I_D * f_T$), presented in Fig. 4-C, is a helpful tool to find an optimal point of application in a circuit design. The best application point for these devices, already considering the influence of temperature, is obtained in the transition from moderate to strong inversion, for IC between 10 ($L=28$ nm) and 15 ($L=200$ nm) resulting in the best performance of analog circuits.

Another important parameter in analog circuits is the intrinsic voltage gain (A_v), that is obtained through equation (3), where V_{EA} is the Early voltage extracted through the $I_{DS} \times V_{DS}$ curve, with $V_{GT}=200$ mV, presented in reference [4].

$$A_v = \frac{gm}{I_{DS}} \cdot V_{EA} \quad (3)$$

For a first order analysis, we considered V_{EA} as being constant for all IC levels, since it did not present a significant variation with IC, as reported in references [3][14]. Fig. 6 presents the Early voltage for each channel length and the respective temperature. The temperature did not cause a significant variation in this parameter, but the channel length does. The impact of the channel length modulation (CLM) becomes more pronounced for shorter channel, causing this degradation in the Early voltage.

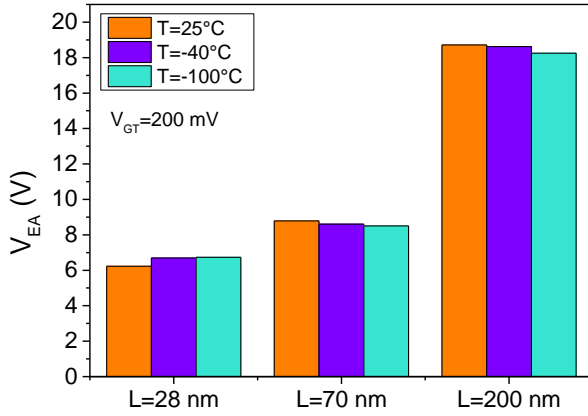


Fig. 6 – Early voltage for $L=28$ nm, 70 nm and 200 nm, for all temperatures.

From Fig. 7, where A_V as a function of IC is presented, it is possible to observe that the maximum gain is obtained at weak inversion, achieving about 58 dB for $L=200$ nm and $T=-100$ °C, since in this region the gm/I_D achieves its maximum. When reducing the temperature, the gain increases due to the influence of temperature on the gm/I_D , which is inversely proportional to the subthreshold swing (that is directly dependent on temperature) [8]. In moderate inversion this gain tends to degrade with a variation about 15 % from $IC=0.1$ to $IC=10$, but it still presents high values for $IC=10$ – from 45 dB ($L=200$ nm) to 39 dB ($L=28$ nm), both at $T=25$ °C, this degradation from weak inversion to strong inversion occurs due to the degradation in the gm/I_D , that degrades while increasing IC, because of the degradation in the carrier mobility that becomes more significant in moderate/strong inversion [8].

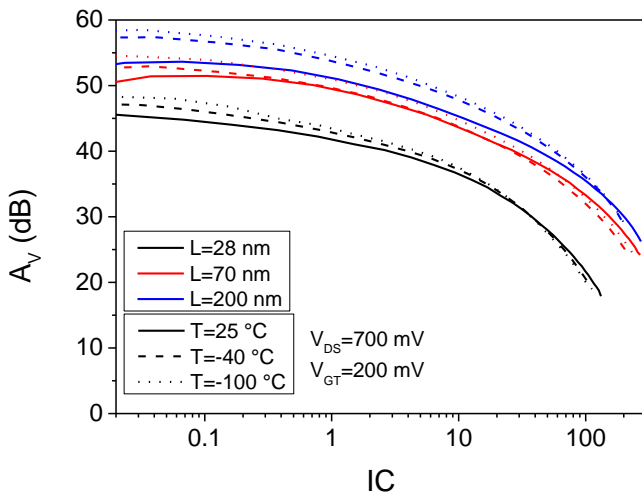


Fig. 7 – Intrinsic voltage gain as a function of inversion coefficient, for different channel lengths and temperatures.

From Fig. 4-C it is noticed that the best compromise (maximum point) between the transistor efficiency (proportional to intrinsic voltage gain) and the unit gain frequency is obtained in the transition from moderate to strong inversion. In spite of the maximum A_V takes place in weak inversion (Fig. 6), Table 1 shows that the intrinsic voltage gain decreases only approximately 8 dB from WI

to SI, corresponding to a reduction of about 0.85 times A_V ($IC=10$)/ A_V ($IC=0.1$) while in Table 2, it is shown that $gm/I_D * f_T$ improves (increase) from WI to SI: a value about 8 – 10 times higher than in WI.

Making this same compromise analysis between transistor efficiency and unit gain frequency it is possible to observe in Table 3 and Table 4, respectively that the improvement in f_T from $IC=0.1$ to $IC=10$ is very significant (about 20.4 to – 25 times higher), while the decrease in the transistor efficiency is about 0.36 – 0.40 times in strong inversion.

Table 1 – A_V for different inversion coefficient (IC)

| L (nm) | A_V (dB) | | $\frac{A_V(IC=10)}{A_V(IC=0.1)}$ |
|--------|------------|-------|----------------------------------|
| | IC=0.1 | IC=10 | |
| 28 | 48 | 39 | 0.81 |
| 70 | 52 | 44 | 0.85 |
| 200 | 53 | 45 | 0.85 |

Table 2 – $gm/I_D * f_T$ for different inversion coefficient (IC)

| L (nm) | $\frac{gm}{I_D} * f_T$ ($V^{-1} * GHz$) | | $\frac{\frac{gm}{I_D} * f_T(IC=10)}{\frac{gm}{I_D} * f_T(IC=0.1)}$ |
|--------|---|-------|--|
| | IC=0.1 | IC=10 | |
| 28 | 254 | 2039 | 8.03 |
| 70 | 48 | 505 | 10.52 |
| 200 | 13 | 122 | 9.38 |

Table 3 – gm/I_D for different inversion coefficient (IC)

| L (nm) | gm/I_D (V^{-1}) | | $\frac{\frac{gm}{I_D}(IC=10)}{\frac{gm}{I_D}(IC=0.1)}$ |
|--------|-----------------------|-------|--|
| | IC=0.1 | IC=10 | |
| 28 | 30.1 | 10.9 | 0.36 |
| 70 | 34.5 | 13.8 | 0.4 |
| 200 | 35.1 | 13.6 | 0.39 |

Table 4 – f_T for different inversion coefficient (IC)

| L (nm) | f_T (GHz) | | $\frac{f_T(IC=10)}{f_T(IC=0.1)}$ |
|--------|-------------|-------|----------------------------------|
| | IC=0.1 | IC=10 | |
| 28 | 8.82 | 186 | 21.1 |
| 70 | 1.37 | 38 | 20.4 |
| 200 | 0.36 | 9 | 25 |

Even with the A_V degradation the transition from moderate to strong inversion is still the optimal point for these devices in terms of analog application, since the obtained increase in $gm/I_D * f_T$ compensates the A_V reduction, but it still presents high values for this technology.

IV. CONCLUSIONS

In this work a trade-off analysis was presented between the transistor efficiency (which is proportional to the intrinsic voltage gain) and the unit gain frequency of the nanosheet (NSH) NMOS devices from 200 nm down to 28 nm channel lengths from room temperature ($T=25$ °C) to low temperatures ($T=-40$ °C and -100 °C).

When the channel length decreases the drain current and the unit gain frequency increase, although the intrinsic voltage gain degrades as expected.

The temperature also affected the devices' behavior, since carrier mobility increases when temperature decreases, due to the reduction of phonon scattering, which directly impacts the analyzed parameters: gm/I_D , f_T and A_V .

From the presented results it was shown that the optimal point of operation for the nanosheet transistors in terms of analog circuits is in the transition from moderate to strong inversion, where the maximum value in the $gm/I_D * f_T$ curve is obtained. As a result, in this point, which can be considered suitable for many analog applications, the A_V is 45 dB ($L=200$ nm) and 39 dB ($L=28$ nm) and f_T is 9 GHz ($L=200$ nm) and 186 GHz ($L=28$ nm), both at $T=25$ °C.

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