A 0.4 V Active Biased LNA for 2.4 GHz Low Energy RF Receivers

Giovana Pegoraro Ceolin and Lucas Compassi-Severo

Alegrete Campus, Federal University of Pampa, Alegrete, RS, Brazil
E-mail: {giovanaceolin.aluno, lucassevero}@unipampa.edu.br

Abstract—To reach the low power requirements for Internet of Things (IoT) applications, the power dissipation of RF transceivers must be very low. As the Low Noise Amplifier (LNA) is one of the most energy-consuming parts of an RF receiver, its power optimization is necessary for modern IoT devices. This work presents a 170 \( \mu \)W LNA capable of operating at 2.4 GHz when powered by a 0.4 V source. It is based on an inverter-based amplifier with improved gate bias voltage and automatic forward bulk biasing to operate at the moderated channel inversion level. A biasing metric is explored to analyze the best transistors sizes and bulk bias voltages for the NMOS transistor. Post-layout simulation results showed a 2.8 dB noise figure, 10.6 dB voltage gain, area of 0.19 mm\(^2\) and competitive specification values and FoM when compared to the state-of-the-art low-voltage LNAs.

Index Terms—ULP; ULV; LNA; Self-Bias Network.

I. INTRODUCTION

The Internet of Things (IoT) market has been growing a lot in recent years. This is mainly motivated by a large number of usage possibilities, with applications from agriculture to the biomedical areas. Some of the IoT devices are operating in energy-constrained environments, such as implantable devices and sensor networks. In this kind of application, the main challenge of modern IoT devices is to reduce the power dissipation in order to increase the battery life time or to be suitable to operate with only energy harvesting sources, known as battery-less devices.

The most advantage of modern IoT devices is their capability for wireless communication. However, the RF transceiver block used to spend most part of the energy in an IoT device. Thus, the optimization of this block is very attractive to reduce the overall energy consumption [1]. Several strategies have been proposed in the literature to reduce the power dissipation of IoT wireless communication, such as the relaxation of the hardware requirements by the modern communication standards and the development of new RF transceivers topologies [2].

The supply voltage lowering has been demonstrated as an interesting strategy to reduce the power dissipation at the receiver side. The works of [3] and [4] have shown that it is possible to design 2.4 GHz Bluetooth low energy (BLE) receivers with ultra-low voltage (ULV) operation. In these works, the RF front-end dissipates less than 400 \( \mu \)W when powered with 0.18 V and 0.55 V, respectively.

In the RF receiver chain, the low noise amplifier (LNA) is one of the main building blocks, since the receiver specifications, such as sensitivity and power dissipation, are mainly related to this. In general, around 40% of the RF receiver power dissipation can be dissipated by the LNA circuit [5].

II. LOW VOLTAGE AND LOW-POWER LNAs

In this section, we present the main characteristics of the ULV Low-Power LNAs presented in the literature, able to operate at the frequency of 2.4 GHz.

The LNA shown in [8] is based on a current reuse resistive feedback topology. This design presents all the transistors biased on the moderated channel inversion level (MI) to obtain higher voltage gain and improved performance. DC blocking capacitors are used to disconnect the RF and DC signals and allow the use of common-gate bias on the NMOS transistor. The circuit can present an input impedance of 50 \( \Omega \) when an input series inductor is used to cancel the imaginary part of the input impedance. The circuit biasing variability is compensated by a digital to analog converter that adjusts the LNA supply voltage around the 0.4 V level. This LNA reaches the power dissipation of 30 \( \mu \)W with operation at 2.4 GHz.

The work of [10], presents single-ended input and balanced outputs. It uses the current reuse technique to decrease the dissipated power, by sharing the DC bias current between the NMOS and PMOS transistors. The high-frequency transconductance is improved without any extra
energy consumption by using an inductor connected to the transistor gate terminal. Additionally, the use of the gate inductor reduces the effect of the parasitic capacitances. In another paper, the same authors have improved the previous LNA by using a $g_m$ boosting technique of shunt feedback cascode topologies to improve the bandwidth without increasing the energy consumption [11]. The forward bulk bias (FBB) is used at the NMOS transistor to reduce the threshold voltage and to allow the gate biasing by the output DC voltage level. In these implementations, the power dissipation of 410 and 160 $\mu$W are obtained, respectively.

In the paper of Ehsan Kargaran [12], a 0.8 V LNA is proposed for Wearable Sensor Wireless Networks (W-WSN) applications. To decrease its dissipated power, the LNA was designed using the reuse of the bias current by four stacked transistors and a source resistor. Additionally, the use of a high-quality factor integrated transformer is employed to improve the level of transconductance gain and to reduce power consumption. A simplified version of this topology is presented in [6] in which the LNA was able to operate with only 0.18 V of power supply, keeping the same power level of 30 $\mu$W.

The LNA proposed by Jian-Yu Hsieh [13], like the previous ULV LNAs, uses FBB biasing techniques to reduce the transistor threshold voltage. The circuit also employs the current reuse technique and multiple gate topology, which makes it possible to eliminate third-order distortion caused by the amplifier’s non-linearity and to improve the Input Third-order Intercept Point (IIP3) specification. Another interesting point is the use of a tunable negative feedback capacitor, which makes it possible to obtain the variable gain without additional energy cost, solving possible signal saturation problems.

In paper [14] an LNA designed for brain-machine interface (BMI) systems applications is demonstrated. The LNA proposed is designed using current reuse and a combination of a degenerate LNA cascode with an inverter-based LNA to reach the ultra-low voltage and low power operation, using a voltage supply of 0.75 V.

As demonstrated, several strategies have been proposed in the literature to reach low-power dissipation. The current reuse, moderated inversion operation and the FBB are the main used solutions.

III. LOW VOLTAGE BIASING ANALYSIS

The operation and design of RF circuits using sub-1V supply voltages is very challenging due to the reduced current density of the MOS transistors at that level.

Classically, the strong channel inversion level (SI) was used as a biasing reference to design the RF circuits. At this level, small transistor sizes can be used to reach the drain current level of mA. Due to this, reduced parasitic capacitances are present on the transistor terminals, and high-frequency operations are found. However, the SI operation is not suitable for ULV low-power RF circuits. The first limitation is due to the voltage level since it is not possible to reach the gate to source voltage ($V_{GS}$) level needed for SI operation. The transistor saturation voltage is higher at SI and it limits the transistor stacking and current reuse techniques. Additionally, the transistor efficiency defined by the gate transconductance ($g_m$) to the drain current ($I_D$) ratio ($g_m/I_D$) is very small at SI, resulting in higher power dissipation.

In contrast to SI, the weak channel inversion level operation (WI) presents the highest values of $g_m/I_D$, it is suitable for ULV and presents a reduced saturation voltage level (lower than 100 mV). However, large transistor sizes are needed to satisfy the transconductance values needed to operate at higher frequencies. Because of that, large parasitic capacitances are present.

Consequently, the moderated channel inversion level (MI) is the most favorable region of the CMOS transistors operation for the modern low-power RF circuits. The current density at MI is lower than the SI but an improved $g_m/I_D$ ratio can be obtained [15]. In comparison to the weak inversion, the operation at MI results in reduced parasitic capacitance due to the relatively lower transistor sizes. These characteristics are important to improve the figure-of-merits of a low-power LNA [8]. The MI operation is reached when the transistor gate to source voltage ($V_{GS}$) is around the threshold voltage ($V_T$) value. Because of that, MI is also called as near-$V_T$ operation. Thus, the use of the Forward Bulk Bias (FBB) is very important to reduce the $V_T$ and, consequently, reduce the DC $V_{GS}$ level needed to be in the MI operation [13].

To demonstrate the advantage of using MI for ULV and ULP designs in submicron CMOS technologies biasing metric (BM) introduced in [16] is analyzed. This metric is given by Eq. 1 and it is composed of the product of the transistor efficiency ($g_m/I_D$), the intrinsic voltage gain ($g_m/g_{ds}$) and the unity-gain frequency ($f_T$) obtained with Eq. 2.

$$BM = \left( \frac{g_m}{I_D} \right) \left( \frac{g_m}{g_{ds}} \right) f_T$$  \hspace{1cm} (1)

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gb})}$$  \hspace{1cm} (2)

In these equations, $g_m$ is the gate transconductance, $g_{ds}$ is the output conductance, $I_D$ is the drain current, $C_{gs}$ and $C_{gb}$ are the gate to source and gate to bulk parasitic capacitances, respectively. Using the simulation of the transistor operation point and analyzing the small-signal parameters for different $V_{GS}$ voltages, Eq. 1 can be evaluated. Fig. 1 shows the values of BM as a function of $V_{GS}$ with different values of channel length (L) for an Low-$V_T$ NMOS transistor in a 180 nm CMOS process. It is possible to see that the smaller the transistor length L, the better is BM. For the transistor used the smallest possible channel length value is 300 nm, this value is represented by the red curve in Fig. 1.

As expected, the peak of BM in Fig. 1 is obtained around the $V_{GS} = V_T$ due to the MI operation. To analyze the effect of the forward bulk biasing, a simulation of the BM for $L = 300$ nm is evaluated for the bulk to source voltages ($V_{BS}$) of 0 V, 0.2 V and 0.4 V. The result is shown in Fig. 2. It can be seen that the lower the bulk excitation for the NMOS transistor, the higher its BM. When $V_B = 0$ V the largest value of BM is when $V_{GS}$ is close to 0.4 V.

Additionally, the use of low voltage supplies also limits the maximum number of stacked transistors in an LNA due
increasing the $V_{GS}$ voltage. Similarly, the gate terminal of the NMOS transistor is biased by resistor $R_{BN}$, tied to $V_{DD}$. With these bias improvements, it is possible to operate near the peak of the Bias Metric, as shown in the last section.

Furthermore, the DC $V_{ctrl}$ voltage provides an FBB to the PMOS transistor, reducing it $V_T$. As the $V_T$ of the PMOS transistor is larger than the $V_T$ of the NMOS, the connection of $R_{BP}$ to the ground makes the transistor operate also near to the peak of the Bias Metric.

The main LNA input impedance ($Z_{in}$) can be estimated according to (3) that was obtained with the small-signal analysis. Due to the low power dissipation of the proposed LNA, the real part of $Z_{in}$ will be higher than 50 $\Omega$ at the operation frequency and its imaginary part will be dominated by the input Miller capacitance due to the feedback parasitic capacitor ($C_{io}$). Thus the C-L network shown in Fig. 5 is used to match $Z_{in}$ with the 50 $\Omega$ source impedance.

Using the same small-signal analysis, the voltage gain ($A_v$) and noise figure ($N_F$) can be estimated according to (4) and (5), respectively.

In these equations, the letters "n" and "p" were used to relate to NMOS and PMOS transistors respectively. The $g_m$ is the gate transconductance, $g_{ds}$ is the output conductance, $\gamma$ is the thermal noise parameter, $K$ is the Boltzmann’s constant, $T$ is the temperature in Kelvin, $s$ is the Laplace’s frequency and the rest are circuit components.

$$Z_{in}(s) = \frac{1}{s(C_{1o}+C_i)+sC_{io}g_{mn}+g_{mp}}$$  \hspace{1cm} (3)

$$A_v(s) = \frac{sC_{io} - g_{mn} - g_{mp}}{s(C_{1o} + C_i) + g_{dsn} + g_{dsp}}$$  \hspace{1cm} (4)

As the LNA circuit operates at a low voltage level, which increases the design difficulty and makes the circuit more sensitive to variations in the fabrication process. An automatic biasing network is also proposed in this work. It is detailed in the next section.
V. SELF-BIAS NETWORK

To obtain the maximum low frequency gain from the LNA and to improve the output voltage swing, the output DC voltage ($V_{out_{DC}}$) of the LNA should be equal to $V_{DD}/2$. Thus, it is possible to guarantee that the transistors are operating at the saturation region, reducing it output conductance value ($g_{ds}$). According to Eq. 4, which represents the LNA gain, it is possible to observe that the $g_{ds}$ has an inverse relation to the gain value, therefore, the smaller the $g_{ds}$, the greater the LNA gain. To make the output voltage to be equal to $V_{DD}/2$, the $V_{DS}$ of both transistors should be equal to $V_{DD}/2$. For that, it is proposed to control the bulk terminal of the PMOS transistor in order to change the $V_{T}$ and to obtain the voltage drop of $V_{DS} = V_{DD}/2$, obtaining $V_{out_{DC}} = V_{DD}/2$.

Thus, a self biasing network is proposed to reduce the circuit sensitivity to process variations. The objective of the proposed biasing circuit is to stabilize the $V_{out_{DC}}$ of the LNA.

In order to ensure that the variation of the bulk terminal of the PMOS transistor between 0 and $V_{DD}$ will result in $V_{DD}/2$, the graph seen in Fig. 6 has been plotted. This figure is obtained with simulations and shows the variation of $V_{out_{DC}}$ when the bulk terminal voltage is changed from 0 V to $V_{DD}$. It is possible to see that there is a large output voltage control range operating with $V_{DD}$ equal to 0.4 V.

In order to perform the self biasing circuit, a closed-loop error amplifier is used to adjust the PMOS bulk voltage. The automatic calibration will be performed using a closed-loop error amplifier that compares $V_{out_{DC}}$ with the reference level of $V_{DD}/2$ and adjusts the voltage $V_{ctrl}$ to make $V_{out_{DC}} \approx V_{DD}/2$. The error amplifier used in this project can be seen in Fig. 7. This circuit is a pseudo-differential amplifier able to operate at low supply voltage levels.

However, the direct connection of the error amplifier to the LNA output terminal adds considerable capacitive load, reducing its operating frequency and gain. To get around this problem, with a small increasing in the power dissipation, a replica bias circuit based in [17] is proposed in this work. Thus, the self-biasing network block diagram shown in Fig. 8 is proposed in this work.

The replica circuit can be seen in Fig. 9. The replica transistors have the same bias voltage and sizes of the main amplifier, but a single multiplicity is used to save power. Thus the closed-loop error amplifier is used to control the PMOS bulk voltage and to make the replica output voltage equal to $V_{DD}/2$. As the replica $V_{ctrl}$ voltage is also applied to the main amplifier, the LNA output voltage is also controlled without any extra load.

VI. DESIGN AND RESULTS

The LNA proposed in this work was designed using a CMOS 180 nm process with 40kÅ UTM to operate at the frequency of 2.4 GHz when powered with a 0.4 V power and with a low output swing. The replica circuit is shown in Fig. 9. The replica transistors have the same bias voltage and sizes of the main amplifier, but a single multiplicity is used to save power. Thus the closed-loop error amplifier is used to control the PMOS bulk voltage and to make the replica output voltage equal to $V_{DD}/2$. As the replica $V_{ctrl}$ voltage is also applied to the main amplifier, the LNA output voltage is also controlled without any extra load.
supply. The transistors were biased with the maximum $V_{GS}$ available of 0.4 V to operate near-$V_T$ at the moderate inversion level and to present an improved biasing metric. The PMOS bulk terminal ($V_{ctrl}$) is connected to an automatic FBB that allows this voltage to be adjusted to make the output DC voltage equal to $V_{DD}/2$.

The transistors of the main LNA were sized using an iterative simulation-based process on the Cadence Virtuoso environment. Equations (1) to (3) were used to analyze the specification trade-offs and to lead the iterative process of changing the transistor sizes in order to obtain the smallest power dissipation, higher voltage gain, lower noise figure, and good input matching. It results in the dimensions of $L = 300 \text{ nm}$ and $W = 5 \mu \text{m}$ to the NMOS and $L = 250 \text{ nm}$ and $W = 4.2 \mu \text{m}$ to the PMOS transistor, both with 15 multipliers. The transistors used in the replica circuit have the same sizes as the main LNA transistors, but using only one multiplier.

The bias resistors ($R_{BP}$ and $R_{BN}$) are equal to 100 k$\Omega$ to reduce its effect at the input and the DC block capacitor $C_2$ and $C_3$ are designed using 8 pF MiM capacitor to present low reactance at 2.4 GHz. The impedance matching was based on post-layout simulations performed in Cadence’s Virtuoso software, where the parasitics were extracted from the layout to obtain a more accurate result. Then, through the Smith chart analyses, the capacitor and inductor are designed to be equal to 0.525 pF and 12.313 nH, respectively.

The layout of the designed LNA is shown in Fig. 10. The complete circuit occupies an area of 0.1051 mm$^2$. Addition-}

![Fig. 10 Layout of the designed 0.4 V LNA.](image)

ally to the previous circuits, an output buffer was used at the LNA output to allow the circuits characterization after the fabrication, using 50 $\Omega$ RF microprobes.

To evaluate the LNA specifications, post-layout simulations were performed using the circuit test bench shown in Fig. 11. Ports with an impedance of 50 $\Omega$ are added to the input and output of the proposed LNA. At the output, a unity gain ideal buffer composed of a voltage-controlled voltage source was employed to allow the voltage to power conversion and to drive the output port. The CL capacitor of 100 fF was used to emulate the LNA output load, equivalent to the output buffer input capacitance.

The total power dissipation of the LNA reaches the value of 169.8 $\mu$W when powered with 0.4 V. The automatic bias control circuits dissipate about 11.5 $\mu$W, less than 7% of the total dissipated power. Fig. 12 shows the post-layout simulation frequency response of the voltage gain and noise figure (NF). The voltage gain varies from 11.07 dB to 3.758 dB when the frequency varies from 2 to 3 GHz and it is equal to 10.62 dB at 2.4 GHz. The voltage gain at 2.4 GHz can be improved by reducing the input capacitance of the output buffer. The Noise Figure (NF) is equal to 2.786 dB at the frequency of 2.4 GHz. The input third-order intercept point ($IIP_3$) is equal to -8.12 dBm and the 1dB compress point ($P_{1dB}$) is around -14 dBm, as can be seen in Fig 13.

The input impedance matching was analyzed by using the
\( S_{11} \) parameter as a function of the frequency. Fig. 14 shows the simulation of \(|S_{11}|\) from 2 to 3 GHz that results in -25.63 dB at 2.4 GHz, showing a good input matching. If the level of \(|S_{11}| < -10 \) dB is considered to evaluate the bandwidth limit, the designed LNA can reach the bandwidth of 357 MHz, operating from 2.222 GHz to 2.579 GHz.

To analyze the effects of auto biasing, some simulations were performed using the Monte Carlo method to visualize the effects of the process and mismatch variations suffered by the circuit. It can be seen in Fig. 15 the frequency histogram for the LNA output voltage without the automatic bias circuit, with \( V_{dd} = V_{DD}/2 \). It can be noticed that the voltage varies widely between approximately 112 and 300 mV. Therefore, without automatic calibration, the circuit is more susceptible to variations and can lead to operation with a low gain value.

Fig. 16 shows the simulation of the Monte Carlo method for the output voltage \( V_{out} \) when the auto-bias circuit is connected. As can be seen, using the automatic calibration, the output voltage is much more stable and with reduced variation, showing the importance of the proposed biasing circuit.

In order to compare the results presented in this work with the circuits in the literature, some Figures-of-Merits (FoMs) will be used. For this, the FoM1 seen in (6) will be initially calculated, which is described in the work of [8] as an FoM defined by the International Technology Roadmap for Semiconductors (ITRS) for LNAs. This metric uses gain \((S_{21})\), the non-linearity due to third order intermodulation \((IIP_3)\), the operating frequency \(f\), the noise figure \(NF\) and the power dissipated by the circuit \(P\).

\[
FoM1 = \frac{S_{21}|_{lin.} IIP_3[mW] f_{op}}{(NF|_{lin.} - 1) P_{mW}}
\]

To make the comparison with low voltage LNAs fair, FoM2 is proposed in this work, seen in (7). In addition to the parameters proposed in FoM1, FoM2 also uses the parameters of nominal process voltage \(V_{ddN}\) and simulation voltage \(V_{dd}\) to enhance low voltage designs.

\[
FoM2 = \frac{S_{21}|_{lin.} IIP_3[mW] f_{op} (\frac{V_{ddN}}{V_{out}})}{(NF|_{lin.} - 1) P_{mW}}
\]

FoM3 was also used, seen in 8, which is proposed in [14], where it shows that this FOM is suitable for comparing the performance of low voltage and low power LNAs. It uses similar terms to FoM2 but still includes the circuit area in its metric.

Fig. 13: Output vs input power to obtain the third-order intercept point. The IIP3 is equal −8.117 dBm at 2.4 GHz.

Fig. 14: Frequency response of the \(|S_{11}|\) parameter. \(|S_{11}|\) is equal to −25.63 dB at 2.4 GHz.

Fig. 15: Frequency histogram of the output DC voltage (\(V_{out,DC}\)) variation obtained with Monte Carlo simulations, without the self-bias circuit.

Fig. 16: Frequency histogram of the output DC voltage (\(V_{out,DC}\)) variation obtained with Monte Carlo simulations, with the proposed self-bias circuit.
Table I. Comparison with some of the state-of-the-arts low-voltage and low-energy LNAs

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<td>0.18</td>
<td>0.6</td>
<td>0.75</td>
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<td>dB</td>
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<tr>
<td>Frequency</td>
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<td>0.6 ↔ 3.1</td>
<td>2.4</td>
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<td>2.8</td>
<td>2.4</td>
<td>2.4</td>
<td>GHz</td>
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<tr>
<td>IIP3</td>
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<td>-10</td>
<td>-13.2</td>
<td>-8.6</td>
<td>0</td>
<td>-8</td>
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<td>LNA Area</td>
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<td>0.37</td>
<td>0.19</td>
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<td>40</td>
<td>180</td>
<td>180</td>
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<td>nm</td>
</tr>
<tr>
<td>FoM1</td>
<td>4.6</td>
<td>0.9 ↔ 4.8</td>
<td>17.3</td>
<td>23.9</td>
<td>-</td>
<td>1.6</td>
<td>8.2</td>
<td>GHz</td>
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<tr>
<td>FoM2</td>
<td>13.7</td>
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FoM3 = $\frac{S_{21[\text{lin.}]} \times IIP3[\text{mW}]}{(NF_{\text{[lin.]}-1})P_{\text{[mW]}}/\text{Area}_{[\mu m^2]}}$ (8)

Table I shows the results obtained with the proposed LNA and a comparison with the state-of-the-art low voltage and low power LNAs, analyzed in section II. It is possible to see that the NF of our work is the lowest value compared to the other papers, even presenting reduced power dissipation.

The FoMs analyzed showed that this work has potential, having a good FoM1 value compared to other works. Its FoM2 showed great results, only behind [6] and [10] in the case of having its better performance at 10 GHz. For FoM3, this work stands out, having improved results in comparison to the other works. The rest of the specifications are in the average range of the other papers.

The post-layout simulation of the proposed LNAs showed comparable performances with the state-of-the-art LNAs presented in the literature. Besides the lower voltage gain, it can be used in low voltage and low power RF receivers. If a higher gain is required, more stages can be added to the receiver chain at the RF front-end or intermediary frequency stages, since a reduced NF was obtained.

VII. CONCLUSION

A low-power 0.4V LNA with a self-bias network is presented in this work to operate at a frequency of 2.4 GHz. Its auto-bias network shows good results making the output voltage more stable and less susceptible to the fabrication process variations.

The results show better performance in terms of noise figure and good values of gain, IIP3 and power dissipation specifications, with good input matching, compared to the latest generation works. The comparison made between the works through the figures of merits (FoM) shows that this work stands out when compared with metrics for low voltage.

The circuit is currently being manufactured, in future works, it is intended to measure and compare the simulated results with the measured ones.

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