FinFET SRAM cell with improved stability and power for low power applications

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***Abstract*— In this paper, a new 11T SRAM cell using Double gate FET (FinFET technology) has been proposed, cell basic component is the 6T SRAM cell with 4 NMOS access transistors to improve the stability over CMOSFET circuits and also makes it a dual port memory cell. The proposed cell also used a header scheme in which one extra PMOS transistor is used which is biased at different voltages to improve the read and write stability which helps in reducing the leakage current, active power. The cell shows improvement in RSNM (Read Static Noise Margin) with LP8T by 2.39x at threshold and subthreshold voltage 2.68x with D6T SRAM cell, 5.5x with TG8T. The WSNM (Write Static Noise Margin) and HM (Hold Margin) of the SRAM cell at 0.9V is 306mV and 384mV.At subthreshold operation also, it shows improvement. The Leakage power reduced by 0.125x with LP8T, 0.022x with D6T SRAM cell, TG8T and SE8T. Impact of process variation on cell stability also been analyzed.**

***Index Terms*— Double-gate FETs, CMOSFET Circuits, SRAM cells, Threshold voltage, Leakage currents.**

I. INTRODUCTION

A remarkable growth in the semiconductor industry has been seen over the few decades. Gate length has been predicted to be 4-5nm by 2023 according to the ITRS (International Technology Road-map for Semiconductor). In the past few decades CMOS scaling feature has revolutionize the semiconductor industry in few years. More than Moore (MTM) rule has overtaken the Moore's Law which predicted that transistor count will be double in 18 months. MTM says that incorporation into services of functional that do not necessarily scale according to Moore law but provide additional value in different ways as per ITRS 2009 [1] glossary. Major area of a die is consumed in memory components. Every chip nowadays has 60-70% of its chip by Memory Circuits. The prevailing memory in this market is SRAM even though the SRAM size is larger than embedded DRAM. The reason being that SRAM does not have yield issues and cost is not high as compared to DRAM. At the same time, the other attractive feature for the SRAM was speed and also it can be used for low power applications. CMOS SRAMs are the crucial component in microprocessor chips and applications and as stated earlier major portion of the area is dedicated to SRAM arrays so CMOS SRAM is considered to be the stack holders in memory market. Since due to the scaling feature of CMOS, SRAM was it having its hold in the market over the last few decades.

The limitations of the CMOS drives the need for an alternative devices which leads to FinFET. FinFET is emerging as one of the suitable alternative for CMOS and in the region of memory circuits it becomes a promising device and in some factors superior choice over conventional MOSFETs because of the property of the low leakage reduction and smaller in size. FinFET dominates over the CMOS as: it has superb control to the gate over the channel which in turn reduces the source/drain leakage current. It also reduces the Short Channel Effects (SCE). FinFET is a multi-gate transistor and so because of the several gates acting on the channel, it has excellent electrostatic properties. Above all the beauty of MOSFET device "Scaling" exists in FinFET [2].

II. REVIEW WORK

A. FinFET Technology

The SCE limitation of nano-scaled CMOS has been consistently been the focus of the researchers. To have a better control over the SCE, multi-gate devices have been evolved from single gate devices. Since shrinkage of the gate length has led to SCE which are increase in sub-threshold, Variation in threshold voltage, punch through between drain and source [3].

To overcome the limitation various solutions have been proposed like to reduce the gate oxide thickness and channel doping should be increased .But capacitance of gate to channel increases due to reduction in oxide thickness and there is a reduction of charge sharing between source and drain and increases GIDL. So, then the other approach of controlling the SCE is to have two or more gate electrode and a thin fully depleted semiconductor body. The vital parameter is the thickness of the thin body which is Fin width in multi-gate transistors. This was the main idea behind the FinFET structure as to keep this body very thin such that there is no leakage path from the gate and gate can have reasonable control. Silicon on Insulator or bulk silicon is used to for FinFETs. The 3D structure of FinFET consists of the thin body known as Fins. The gate covers the channel from the three sides which gives excellent to the gate. The channel is vertical in FinFET, so the width of the device is determined by the height of the Fin. The current can be increased by increasing the width of the device or by increasing the number of Fins. The double gate FinFET has two gates back and front, which are electrically coupled to reduce the SCEs effect by reducing the sub-threshold slope and DIBL.

IG-FinFETare more appropriate for low power applications as they can significantly contribute in reduction of standby power dissipation and leakage power [4].

B. SRAM Cells

FinFET started replacing the CMOS because of the low leakage current. In [5] the 6T SRAM proposed used a com-

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mon a common back-gate bias to improve the Read Performance, Read Margin, Write delay. The cell uses a reverse bias also to reduce the leakage. Since the cell nodes are not disturbed by the Read current in the 8T cell, Read stability is the same as Hold stability, in the Read mode, the drain current increases with an increasing back-gate voltage. Thus, the Read performance is improved. To reduce the leakage current during the standby mode the back-gate voltage is switched to a negative voltage or zero voltage. To optimize Read/Write margins for stable SRAM operation, one would like to have a higher supply voltage during the Read operation to maintain an adequate noise margin, and a lower supply voltage during the write operation to facilitate writing [6]. In [7] FinFET 8T-decoupled SRAM has been proposed where an "and gate" is used which completely removes half select stability problems because of the word line which remain ON of an un-selected cell. The authors improved the cell stability without affecting the performance of the design. A 6T-Decoupled SRAM Cell has been proposed in [7] which works good for low voltage and half select column also. 8T SRAM in [8] proposed for low power and improved stability. In [9] for enhanced stability SRAM using FinFET with dynamic gate voltage adjustment has been proposed SRAM cell with pass gate feedback has been proposed in [10].

The other SRAM cell with pass p-type access transistor has been discussed in [11]. 8T FinFET SRAM cell has been with enhanced read and write margin 8T SRAM cell reported in [12]. Sub-threshold FinFET SRAM has been proposed for low power applications in [13]. Robust 6T SRAM cell using FinFET has been discussed and proposed in [14]]. Due to the impact of process variations and varying supply voltages in 6T Conventional SRAM using FinFET as shown in Fig. 1 it is very difficult maintain both the operation, which results majorly in read failure [15]. In [16, 17, 18, 19, 20] the read and write assist circuit has been discussed which helps in reducing the functional failures during read and write operations. Though the disadvantage of the also exists like larger delay, area additional circuitry for voltage source to control the voltage level of word-line or bit-line [16].

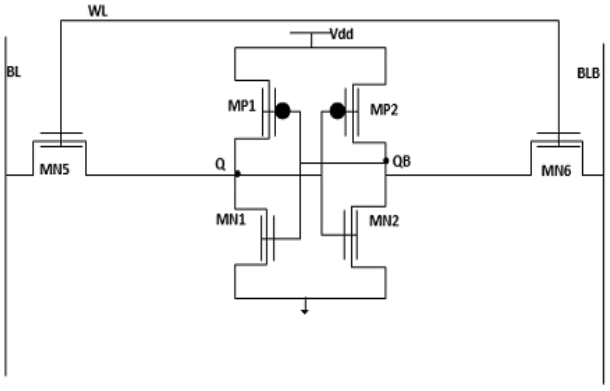

Fig. 1 Conventional 6T SRAM Cell with FinFET

Different single port and multiple port SRAM bit cells are being reported by the researchers for low operating voltages, high stability and for robust operations. In [21] a differential 8T SRAM-NEW for improved read data stability and higher write ability is depicted. The Schmitt trigger configuration in [22] makes the inverter pair of 10T ST has proposed for improvement in SRAM but it leads to low SNM with larger read delay. The 10T SRAM cell discussed in [23], however, compensates the read-disturbance problem of [22] as it has separate read and write ports for read and write which is responsible for decoupling the storage nodes from the bit lines during read operation. This configuration has extra signal VGND (virtual ground) in the read path to reduce bit line leakage. In 10T P-P-N SRAM cell [24] attains the equal RSNM and HSNM as the bit-lines are isolated during read operation from the real storage node through pseudo storage node. 10T SRAM as shown in Fig. 2 has been proposed in [25] for near threshold having high read and write margins, this paper also has extra virtual ground for improving the stability. The cell works well for super threshold and near threshold but the active power was high .In this paper an 11T SRAM has been proposed for low power applications.

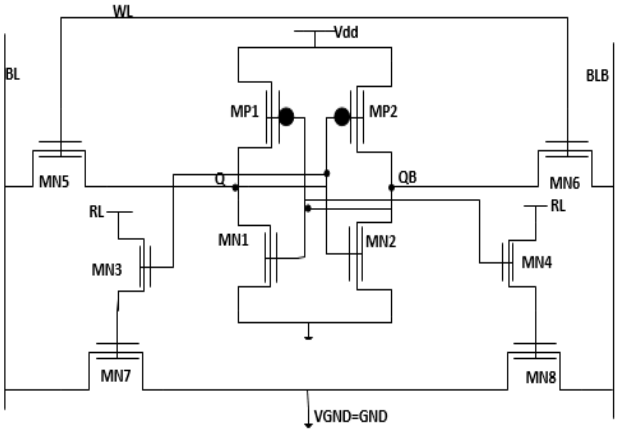

Fig. 2 10T FinFET SRAM Cell

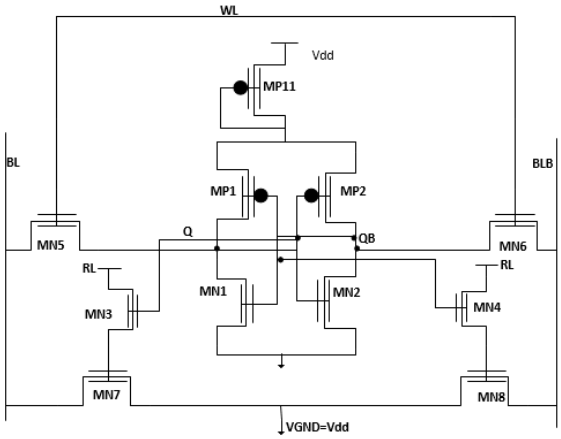

Fig. 3 Proposed-I FinFET SRAM CELL.

III. PROPOSED SRAM CELL

The proposed work is an 11T SRAM having different ports for read and write as shown in Fig. 3. The Cell is originally having a 6T SRAM which is having word line and bit line similar to all the 6T SRAM transistors. This cell has separate port for read and has two read lines (RL). The two access transistor of the 6T SRAM is connected with the bit line (BL and BLB) and word line (WL) similar to conventional 6T SRAM cell. The pass transistors MN5 and MN6 remain on during the write operations as Word line (WL) remain high. The bit line value depends on the data to be written in the cell. The others transistors MN3 and MN4 are the switching transistors which are being controlled by the value of Q and QB. MN7 and MN8 basically the pass transistors which will get on during read operation. These two transistors are to be connected to ground mode in read operation and to Vdd during the other two operation of hold and write mode such that bit line leakage current from the read path can be controlled.

In this scheme by changing the back gate bias voltage of the header transistor MP11, the supply voltage can be varied during read and write operations. During the read operation, the lower gate bias voltage can improve the read margin and during the write operation the higher back gate bias voltage will improve the write margin. During hold mode lower supply voltage is needed to control leakage. The advantage of this scheme over the conventional dynamic supply voltage is complexity and hardware increased as it requires the external two power supplies or voltage regulator or generators to arrange for the extra supply level and routing of the two supply voltage lines is also needed [21]. In context to the above-mentioned scheme here routing is needed for the virtual supply voltage line.

As discussed, in [21] the header scheme needs only one header diode while the conventional uses two pass transistors, also in the conventional scheme the drain of the pass transistors are directly connected to the supply voltages due to which most of the charge is required in charging and discharging of the voltage rail capacitance. While scheme used in this paper the virtual supply control line used to charge and discharge the back-gate capacitance, and the front gate current is used to charge or discharged the voltage rails. Consequently, in the header scheme the settling time of the virtual supply is smaller.

As mentioned the proposed cell is a dual port memory cell, so during write operation Word line is enabled and the Read Word line (RL) is disabled, Fig. 3 shows the values of each input during the write operation. If we assume that initial some data is written, Assuming Q to be logic 0 and in this node if logic 1 needs to be write we need to enable BL to the high value and BLB to logic 0.The node which was holding a logic 1 can now be discharged through access transistor MN6 and through MN2 and the node which was holding a value Q can now be charged to Vdd through MN5 and MP1 as MN1 will no longer be on to discharge the node. During write operation the back gate of the PMOS transistor is kept at high voltage to improve the write margin. During write operations the virtual ground is kept at Vdd. The MP11 transistor back gate voltage is also kept at high voltage to improve the write stability.

During read operation the Read word line is enabled and the word line is disabled both the bit lines are pre-charged to supply voltage as shown in Fig. 4. During read operation the virtual ground is discharged to ground. Since the data stored at Q is at logic 0 and WL is also at logic 0 both the pass transistors are off .The transistor MN4 is off which results in switching off the MN8 also. So BLB cannot discharge through this path but BL discharges through MN3 and MN7.The back gate bias voltage of transistor MP11 is also kept at low voltage which will help in improving the read stability.

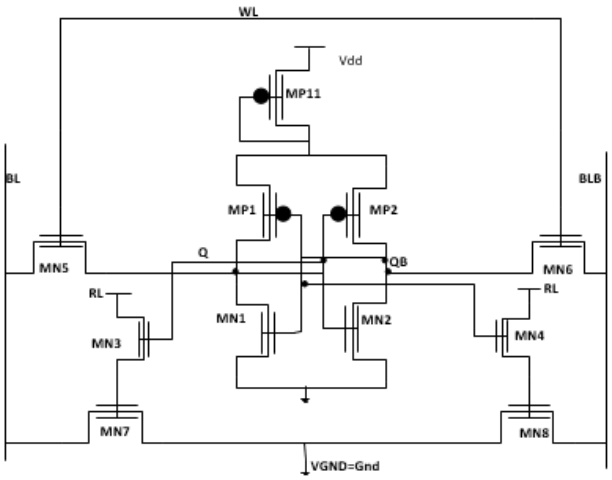

Fig. 4 Proposed-II SRAM CELL: Read Operation

As discussed, in the write operation section the hold operation also has the same connections and voltage levels for transistor MP11 where its back gate bias voltage is kept at high voltage, the virtual ground is also pulled up to supply voltage. The hold operation is the ideal state of the cell where the word line and the bit lines are disabled and the bit lines are pre-charged to Vdd. The reason behind keeping the virtual ground at Vdd is that turn off the potential leakage path of the bit lines to virtual ground which will improve the leakage power of the SRAM. The Proposed SRAM cell has the important feature of the header transistor which help in improving the power and stability of the cell. The virtual ground node and the four access transistors also helps in improving the performance of the cell as discussed in the previous sections

IV. SIMULATION RESULTS

The projected bit cell is simulated using HSPICE with 20nm FinFET and 16nm technology at room temperature with typical process corners .The PTM-MG model for FinFET is used to calculate and access the various performance parameters. The cell has been simulated for above threshold voltage and subthreshold voltages. The technology parameters are different for 20nm and 16nm which are being used to simulate the 11T SRAM cell is shown in Table1.The pro-

posed cell has having 11 transistors and each PMOS transistor is considered with 1 Fin and the access transistors MN5 and MN6 are with 2 Fins and remaining all are with 1 Fin transistors. The cell has been simulated from 0.9V to 0.1V to evaluate the performance of during the Super threshold and Sub-threshold. If the cell shows a good performance is good it can be used in the high performance constrained application and if it shows better performance in sub-threshold region it can be considered for low power applications.

TABLE I TECHNOLOGY PARAMETERS FOR FINFET

Parameter	Value for 20nm	Value for 16nm
Supply Voltage	0.9V	0.85
Channel Length(Lg)	24nm	20nm
Fin Thickness(tsi)	28nm	26nm
Fin Height(Hfin)	20nm	12nm
Equivalent Oxide thickness	0.84nm	0.68nm

V. RESULTS

As discussed in this paper the proposed SRAM cells which is an 11T SRAM FinFET is suitable for low supply voltage SRAM design. But, the FinFET technology is still not developed and matured as CMOS technology so various concerns needs to be taken care like failures during read and write operation and stability parameters. Read operation, read stability, active read power are few issues needs to be taken care in every memory design. This paper has addressed the issues and solution on performance of the SRAM cell for different performance metrics like read and write stability in normal conditions and with process variaion conditions also, standby Power and delays of the cell has been evaluated to judge the performance of the memory cells

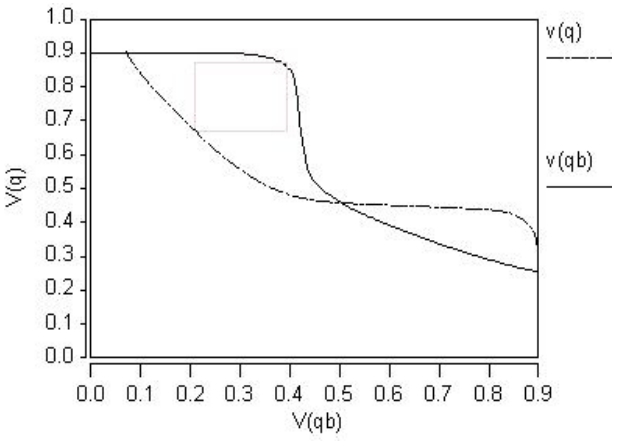

Fig. 5 Read SNM for the proposed Cell at 0.9V

Since, the cell has three modes as discussed and so each mode can define its own margin which reflects the stability of the cell in each mode section. In [26] it has been discussed that Static Noise Margin is a common measure of the ability of the cell to retain the states, it is the minimum noise voltage present at each node of the cell required to flip the data. The conventional method to calculate the Read Static Noise Margin is using butterfly curve using the VTC curve of the inverters. Here, to calculate the stability criteria butterfly curve is used. The RSNM is calculated using the butterfly curve.

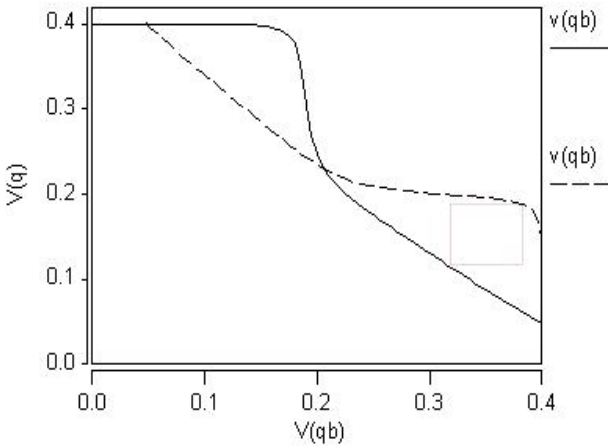

Fig. 6 Read SNM for the proposed Cell at 0.4V

During read operation, both the bit lines are kept at the high voltage equal to Vdd and so the storing nodes of conventional SRAM cell are not insulated from discharging path of the bit line and hence may responsible to increase the voltage of the node storing bit 0 which may also cause flipping of the data. To improve the Read Stability in this proposed bit-cell, the back gate bias voltage is kept at lower voltage also, also the data storage node which is isolated from the bit.

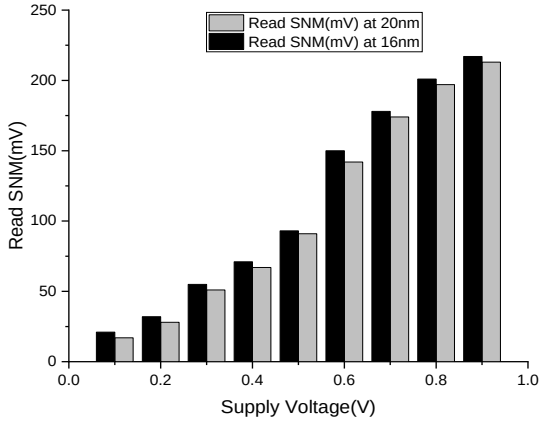

Fig. 7 RSNM variation with Supply Voltage

line discharging path suppresses increases in voltage level during read 0. The RSNM calculated using butterfly curve during different supply voltages of 0.9V to 0.4V. The butterfly curve for 0.9V and 0.5V is shown can be seen in Fig. 5 and Fig.6.

The RSNM at 0.9V is 213mV and at 0.4V is 67mV. The SNM for a bit cell with ideal VTCs is still limited Vdd/2 because of the two sides of the butterfly curve. An upper

limit on the change in SNM with Vdd is thus 0.5 V only. As shown in the above figures the Vtrip point is close to VDD/2.The RSNM using butterfly for various voltages is as shown in Fig.7 at technology parameters of 20nm and 16nm. SRAM cell and thus the RSNM value increases at higher temperature.

At higher temperature the threshold voltage of PMOS reduces more as compared to NMOS [27] and thus, it increases the Vtrip point of the inverter pair of the SRAM cell and thus the RSNM value increases at higher temperature. However, reduction in absolute value of threshold voltage at higher temperature reduces the RSNM. The rise in RSNM of the proposed cell which can be observed in Fig. 8 at the higher temperature.

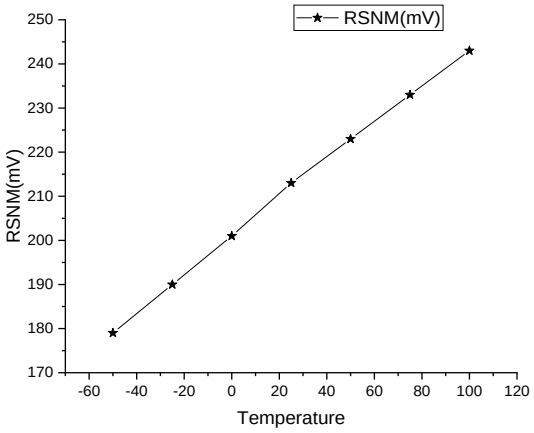

Fig. 8 RSNM variation with Temperature

The read power or the active power is one of the important performance parameters which actually depends on the read current.

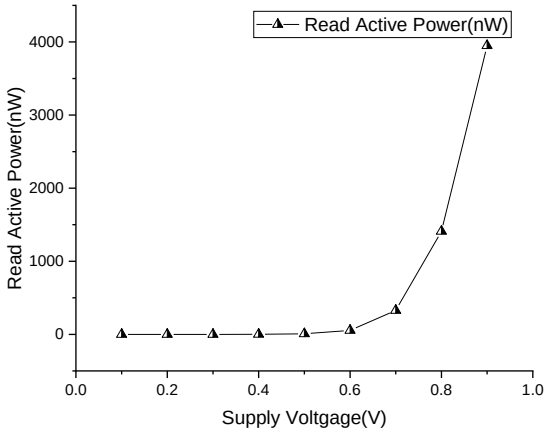

Fig. 9 Read Active Power

The Read power estimated for the cell at 20nm technology is as shown in Fig. 9. The read power reduces drastic

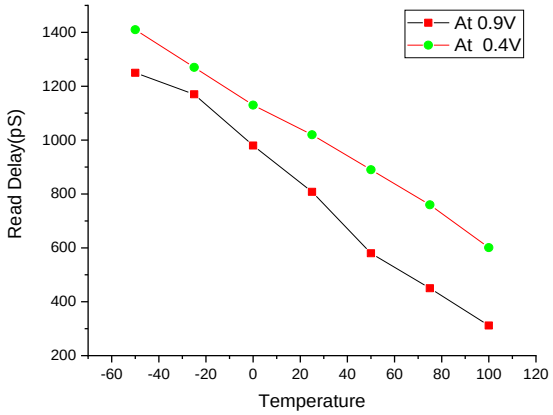

Fig. 10 Read Delay Variation with Temperature

cally due to the lower back gate bias which helps in reducing the read power as compared to other cell reported in [25].

This helps in improving its read delay. Temperature is also one of the role players in manipulating the performance of the circuit, here we have varied the temperature from 100ºC to 50ºC to observe the effect on the read delay. The effect has been observed at 0.9V and at the subthreshold supply voltage of 0.4V. The delay at lower voltage has been increased [25]. There is larger variation with respect to variation in temperature. The larger fall in delay at higher temperature can be seen in Fig. 10.

During 0.9V the read power is 3.95 µW and during subthreshold it is 1nW only. The read power is also calculated at 16nm technology and observed for super-threshold voltage of 0.9V which is 3.74µW 0.813nW at the sub-threshold voltage of 0.4V. Access time is one of the important factors of judging the performances of the memory circuit. Here, in this paper, read delay has been evaluated to know the performance of the cell. Basically read delay is defined as the time needed to develop a differential voltage (100mV) between the bit lines after 50% activation of reading signal [3]. It depends on read current value and number of transistors present in bit line discharging path. In this cell during the operation of read logic 0 there is only one access transistor path for bit line discharging.

The important parameters to study the write operation are write stability, write delay and write margin are the important metrics. Butterfly curve is used to find the WSNM of the proposed bit-cell when WL is kept high and RL=“0”. The values of the Bit-lines BL and BLB are oppositely determined according to the data to be written in the cell. Write delay is measured from 50% of the WL signal voltage level to the voltage level of the WL at which the cell flips to complete the write operation [28].Write voltage margin (WM) is the voltage difference between the supply voltage and the minimum WL voltage that results in a successful write operation [28].

For determining WM of the cell, Word line is being the sweep from zero to the voltage where the bit-cell completes the operation.

As known, SRAM cell with larger WM shows easy write operation compared with the cell having smaller WM. Write Static Noise margin has been calculated using butterfly curve at various supply voltages which is shown in Fig. 11 and Fig. 12.The WSNM at 0.9V is 306mV and at 0.4V is 115mV.

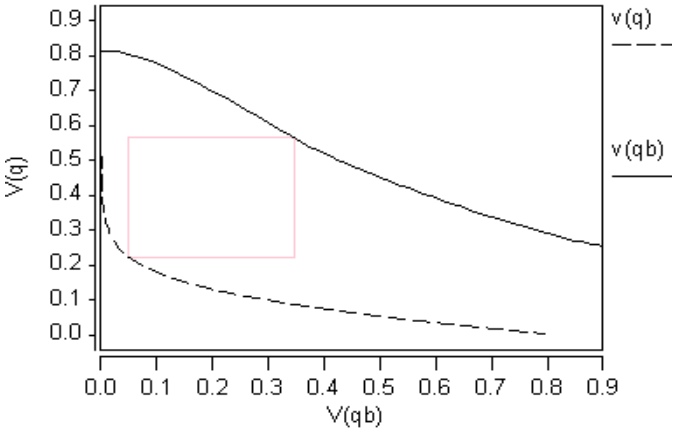

Fig. 11 Write SNM for the proposed Cell at 0.9V

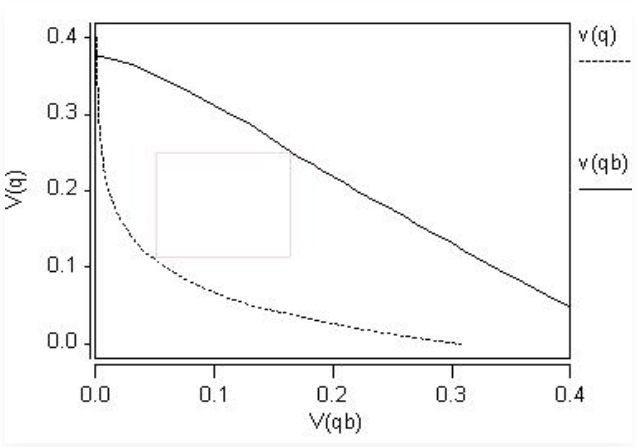

Fig. 12 Write SNM for the proposed Cell at 0.4V

The WSNM has been evaluated for both the technology parameters 20nm and 16nm. Fig. 13 shows the WSNM at both the technology i.e. 20nm and 16nm. The WSNM for 16nm at 0.8V is 310mV and at 0.4V is 119mV. Write Power is considered to be the active power of the cell. In this paper write power has been calculated and is shown in Fig. 14 for varying voltages from 0.9V to 0.1V.

The write power at 0.9V is 65nW and at 0.4V is 80pW. The write power is very less as compared to projected in [25]. The write metrics for the cell including WSNM and Write power is better as compared to RSNM and read power. Like the read delay, write delay also been calculated in this paper. As mentioned in [21], write delay is measured from 50% of the word line voltage level to the voltage level of the word line at which the cell flips for successfully completing the write operation [28].

The delay has been calculated at 0.9V and at the subthreshold voltage with variation in temperature as shown in Fig. 15 and the curve verifies that one of the drawbacks of reducing the supply voltage is the increase in the delay. Write margin is another metrics which plays a vital role in evaluating the write performance of the SRAM cell.

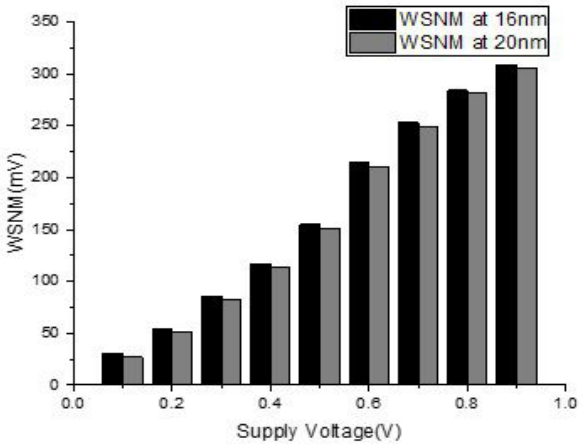

Fig. 13 SNM variation with supply voltage

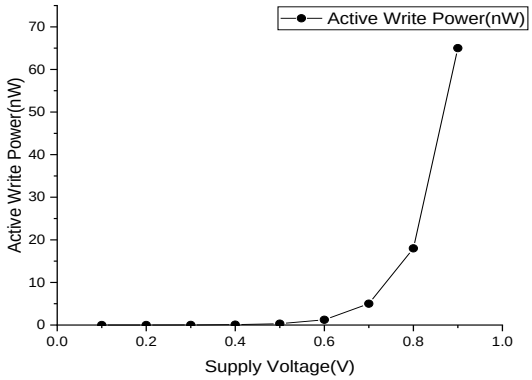

Fig. 14 Write Power variation with supply voltage

The Write Margin is defined the difference between the supply voltage and the minimum WL voltage for a successful write operation [28]. The word line varies from 0V to the voltage where it completes the write operation, this is how WM is being measured. As understood, Cell with high WM exhibits easy write operation compared to the cell with smaller WM.

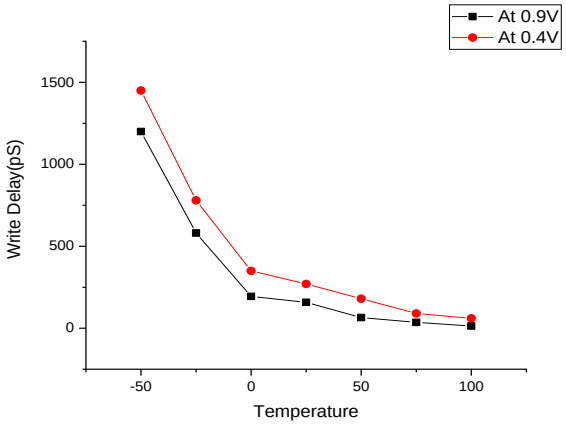

Fig. 15 Variation of the Write delay with temperature

The Write Margin has been calculated at super Vt and sub-threshold voltage, Fig. 16 shows the variation of the WM with respect to the supply voltage and the variation of the temperature on the Write Margin is given in Fig. 17. The SRAM operates in the hold mode during the idle state. The Hold static Noise margin is found using Butterfly curve. HSNM has been found for voltage range from 0.9V to 0.1V at 20nm and 16nm technology respectively. In hold state, the cell does not read and write but stores the previous value. The parameter metrics calculated in this state are important as the power dissipation directly relates to the leakage power dissipation.In this paper, the HSNM is moderately high than the write margin. The HSNM for Super Vt (0.9V) is 384mV as shown in Fig. 18 and at sub-threshold (0.4V) it is 181mV for 20nm technology as can be seen from the butterfly curves in Fig. 19.

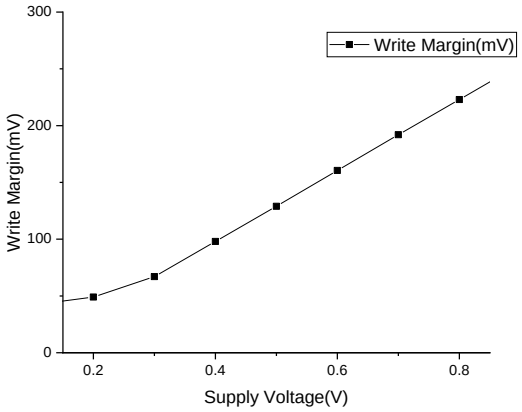

Fig. 16 Variation of the Write Margin with supply voltage

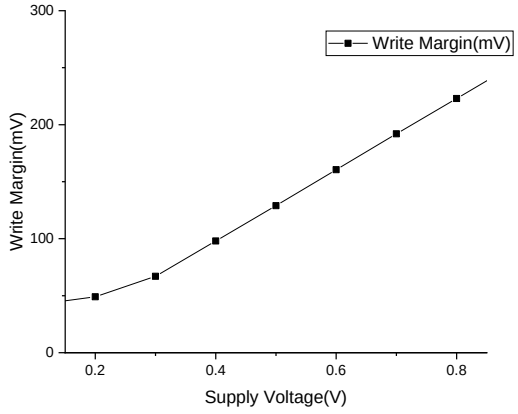

Fig. 17 Variation of the Write Margin with Temperature

And the PMOS and the stacking transistors helps in reducing the static power dissipation. The hold power or the Static power dissipation of the SRAM cell is as shown in the Fig. 20. It is obvious from the Fig. that static power reduces at lower voltages. In the Idle state, the virtual ground signal is kept at the high voltage equal to Vdd which checks the possible leakage path from BL and BLB to ground and finally helps in reducing the power during hold mode and write mode. The static power dissipation for 20nm at 0.9V is 158pw and at 0.4V is 11pw.For 16nm the power at 0.9V is 153pW and at 0.4V is 8.8pW.

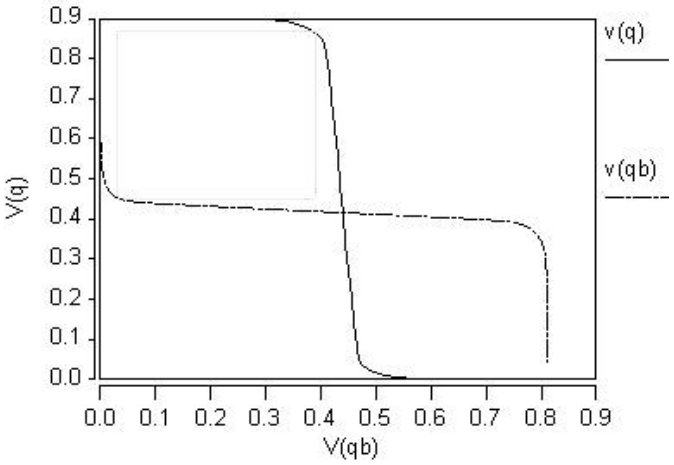

Fig. 18 Hold SNM for proposed cell at 0.9V

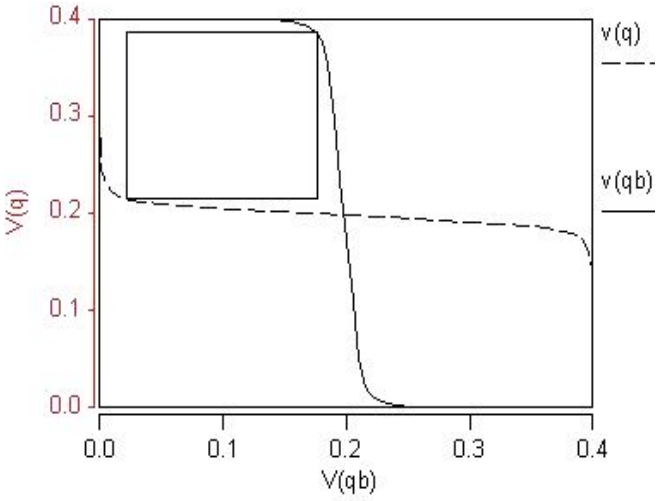

Fig. 19 Hold SNM for proposed cell at 0.4V

VI. Conclusion

Here, a SRAM cell has been proposed using header transistor scheme with LP mode of FinFET at 20nm and 16nm technology has been proposed. The cell has been simulated at two technology nodes of 20nm and 16nm. The cell has been simulated and analyzed in the three modes read, write and hold. The simulation has been done for super-threshold and sub threshold voltage. Comparison of the proposed work with various SRAM cells reported in [25] for sub-threshold operation has been done. Improved results in RSNM during sub-threshold operation. At 0.4V the cell has 2.39x better than the LP8T SRAM cell, 2.68x with D6T SRAM cell, and 5.5 x with TG8T and 1.6x with SE8T. The WSNM has also been improved over TG8T SRAM cell by

1.33x and slightly with LP8T SRAM i.e. with 0.95x.The comparison has been shown in Table II.

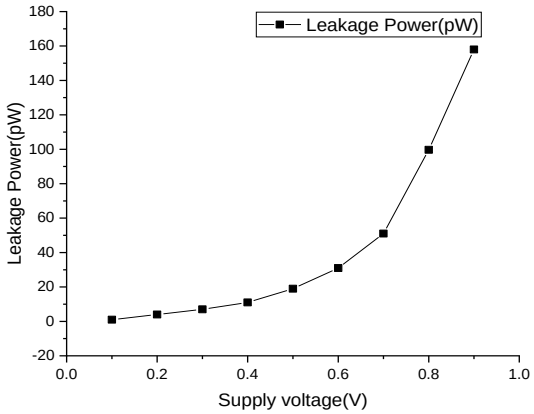

Fig. 20 Leakage Power

Table II Comparison with existing SRAM Cells

Proposed SRAM Cell	LP8T SRAM Cell	D6T SRAM Cell	TGT SRAM Cell	SE8T SRAM Cell
Improvement in Leakage Power at 0.4V	0.125x	0.022x	0.026x	0.025x
Improvement in RSNM at 0.4V	2.39x	2.68x	5.5x	1.8x
Improvement in WSNM at 0.8V	0.95x	--------	1.33x	-------

The effect of temperature variation and the supply voltage on RSNM, WSNM, and HM has also been analyzed for the cell at different voltages and temperatures. Read delay and write delay has also been calculated with respect to the temperature and supply voltages. Overall, the cell has better hold and write ability at Super-threshold voltages and the good read and hold ability at sub threshold voltages. The cell is very much suitable for all the low power applications because of the header scheme used in this paper.

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