Integrated Hybrid Switched Converters: A Review

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***Abstract*— The requirements of portable devices and other applications for a compact and efficient power converter drives the integration of power converters. However, conventional switched-inductor and switched-capacitor converters struggle with these requirements in integrated circuit dimensions. This paper introduces the state-of-the-art of a growing trend in integrated power converters, called hybrid switched converters. Here, the issues of conventional topologies are introduced, as well as the improvements addressed by hybrid converters, in terms of power efficiency, power density and voltage conversion ratio. Also, the characteristics of the four main trends in fully and highly integrated hybrid switched converters topologies are discussed. Finally, their state-of-the-art metrics are presented and compared to the metrics of conventional integrated switched converters.**

***Index Terms*—Hybrid power converter, integrated switching power converter.**

I. INTRODUCTION

Current and emerging electronic devices (portable, wearable, IoT, etc) demand for efficient power converters that adapt the voltage input from the energy sources (mains, batteries or harvesting sources) to the voltage and power required by sensors, actuators, screens, microcontrollers, etc. Moreover, these devices should accomplish the requirements for small size and compact form factor [1] [2], high-power efficiency, and smart functionalities in a wide range of voltage conversion ratios (VCR). These are clear motivations to look for an integrated solution with the minimum quantity of external components. However, power efficiency can easily be jeopardized when scaling the power devices to integrated circuit (IC) dimensions [3].

Typically, power converters are based on linear regulators, Switched-Inductor Converters (SICs) or Switched-Capacitor Converters (SCCs). Linear regulators control the output voltage using a dissipative element in series with the load. They offer the most compact solution, but at the expense of efficiency. Its power efficiency (η) depends on the VCR (V_{out}/V_{in}), i.e. the efficiency reduces when the output voltage is much smaller than the input voltage. Additionally, they are unable to increase the output voltage beyond the input voltage. SICs are composed mainly of switches and magnetic components (inductors or transformers). They accumulate energy in the form of a magnetic field to later be delivered to the load. SICs are widely used because of their high efficiency and wide VCRs; but they require large inductance (L) values with low resistance (R_{DC}). Since the energy density and L/R_{DC} ratio for integrated inductors are lower than for discrete inductors [4] [5], their integration and efficiency in small packages or on-chip is limited. Additionally, the switches should be rated to withstand the full input or output voltage. This may require transistors with a higher breakdown voltage [6]. SCCs are composed mainly of switches and capacitors. The capacitors accumulate energy in the form of electric field, which is later transferred to the load. Integrated capacitors offer higher energy density than integrated inductors, thus they offer a good IC integrability, i.e. small form factor and size [5]. Additionally, SCCs enable the use of switches rated at lower voltages, decreasing its on-resistance per area and reducing the conduction loss. However, SCCs suffer from charge transfer loss [7]. It limits the power efficiency of the converter, even using ideal components. Also, the VCR of SCCs cannot easily be modified to regulate efficiently the output voltage [8].

The main challenge for conventional integrated power converter is to achieve maximum power efficiency in a reduced size (integrated in package or on-chip) while offering efficient voltage conversion ratio control. Each one of the conventional converter offers complementary strengths that can be merged in a hybrid converter to alleviate its weakness. A hybrid converter can be understood as the combination of two or more types of converters (SIC, SCC or linear). Some combinations are already used in commercial products, such as converters based on SCCs and linear regulators, intended for LED drivers [9]. Also, combinations of SICs with linear converters are common and treated as two-stage converters [10] [11]. However, the combination with a linear converter does not help to solve the efficiency and VCR issues of SCCs, or the integrability issue of SICs.

New topologies using SCCs and SICs together have been proposed and matured in the later years to merge its advantages [12], called Hybrid Switched Converters (HSCs). They aim at three main goals: reduce the size of components, reduce power losses, and enable continuous conversion ratios with good efficiency. These goals can be translated in improvements on power density, power efficiency and VCR. This paper reviews the concepts and trends of integrated CMOS power converter based on HSCs.

This review is organized as follows. Section II describes efficiency, power density and VCR issues of conventional converters. Section III introduces the trends of HSCs' topologies. Section IV presents the state-of-the-art metrics of

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HSCs and compares with conventional integrated power converters. Finally, conclusions are drawn in Section V.

II. Efficiency, Power Density and VCR

To understand the strategies implemented by HSCs is important to be aware of the challenges faced by conventional power converters. The three main features of power converters are: power efficiency, power density and VCR. They will be addressed as well as their trade-off.

A. Power Efficiency

Power efficiency depends on the total power losses, i.e. $\eta = P_{out}/P_{in} = P_{out}/(P_{out} + P_{loss})$. Power losses can be broadly classified in two types: conduction loss and switching (or frequency-dependent) loss.

The conduction loss (P_{cond}) is caused by resistive elements in the path of the current. The main contributors in SICs are the on-resistance of the switches (R_{ON}); and the resistance of the inductor (R_L), also known as DCR. In general terms, P_{cond} of a converter with N switches can be modelled as:

$$P_{cond} = I_{L_{RMS}}^2 R_{DCR} + \sum_{i=1}^{N} I_{RMS,sw_i}^2 R_{on,sw,i} \quad (1)$$

where $I_{L_{RMS}}$ is the rms inductor current and I_{RMS_i} is the rms current in each switch. Likewise, losses due to interconnections (bondwires, PCB and IC paths) can also be included in (1).

Inductors with lower DCR occupies larger area, for the same inductance value [13]. Likewise, integrated switches with lower R_{on} demands larger IC area, or switches rated at lower voltage [14]. Therefore, reduction in conduction losses implies larger inductor and switches (i.e. lower R_{on}) sizes. However, this is in the opposite direction to the fully integrated power converter. Also, it can be achieved with lower operation voltage to use low-voltage rated switches; or lower rms currents (e.g. through faster switching). However, it may limit the application of the converter or increases switching losses.

Switching losses depend directly on the switching frequency. In SICs, the main contributors are: P_{tran}, P_{Ciss}, P_{Coss}, P_{driver} and P_{core}. Transition or Miller plateau loss (P_{tran}) at the switches are associated to the power dissipation created by non-zero drain current (I_d) and non-zero drain-source voltage (V_{ds}) during the turn-on and turn-off commutation of the power MOSFETs [15]. The duration of the commutation depends on the gate charge (Q_G) and the current provided by the gate driver (I_{driver}) to charge the gate-drain and gate-source capacitance as explained in [16]. Then, this loss can be modelled as:

$$P_{tran} = \sum_{i=1}^{N} \frac{V_{bk,i} I_{d,i}}{2} f_{sw} \left(\frac{Q_{G,i}}{I_{drv_{PD}}} + \frac{Q_{G,i}}{I_{drv_{PU}}} \right) \quad (2)$$

where f_{sw} is the switching frequency, N is the number of switches, $V_{bk,i}$ is the blocking voltage of each switch, $I_{drv_{PD}}$ and $I_{drv_{PU}}$ are the current of the gate driver in the high-low and low-high transitions, respectively.

Charge transfer loss occurs when a capacitor is charged from a voltage or from another capacitor with different potential [16]. P_{Ciss}, P_{Coss} are losses associated with the charge transfer loss in the input capacitance ($C_{iss} = C_{gd} + C_{gs}$) and output capacitance ($C_{oss} = C_{ds} + C_{gd}$) of the power switch [15] [17]. They can be modelled as:

$$P_{C_{iss}} = \sum_{i=1}^{N} C_{iss,i} f_{sw} V_{drv}^2, \quad (3)$$

$$P_{C_{oss}} = \sum_{i=1}^{N} C_{oss,i} f_{sw} V_{bk}^2 \quad (4)$$

where V_{drv} is the voltage used to drive the gate-source of the MOSFET switches.

Gate drivers are needed to drive the large input capacitance of the power switches, therefore they incur in switching losses. For example, a basic implementation of the gate driver is a tapered buffer, a cascade chain of N digital inverters sized by a factor β per stage. The switching loss due to N drivers is modelled by [18] as:

$$P_{driver} = \sum_{i=1}^{N} \left(f_{sw} V_{drv} \left(Q_i + \beta Q_e \right) \frac{\beta^n - 1}{\beta - 1} \right) \quad (5)$$

where the intrinsic charge (Q_i) is the charge needed by an unitary inverter without load, and the unitary effort charge (Q_e) is the additional charge needed to drive the next inverter stage. However, depending on the switch implementation, voltage level conditioning can be necessary. It can demand for level shifters and bootstrapping circuits (e.g. a buck SIC with a nMOS high-side switch), adding additional switching losses.

Inductor's magnetic loss (P_{core}) depends on the inductor dimensions and can be calculated as [19]:

$$P_{core} = K_{FIT} f_{sw}^{\alpha} (\Delta I_L)^{\gamma} \quad (6)$$

where K_{FIT}, α and γ are parameters given by manufacturers and ΔI_L is the inductor current ripple.

Therefore, reduction of switching losses in SICs are accomplished with the reduction of switching frequency, operating voltages and lower parasitic capacitances on the switches, i.e. smaller switches. However, it may limit the application or increase conduction loss.

In SCCs, besides P_{Ciss}, P_{Coss} and P_{driver}, the conduction loss and the charge transfer loss due to flying capacitors' charge are modelled as P_{SC}. These losses are modelled by an output impedance (R_{OUT}) as:

$$P_{SC} = R_{OUT} I_{L_{RMS}}^2 \quad (7)$$

where R_{out} is approximated to:

$$R_{OUT} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \quad (8)$$

The conduction loss due to the R_{on} of the switches in the SCC is given by [5]:

$$R_{FSL} = \sum_{i\_switch} \sum_{j\_phase} \frac{R_{on,i}}{D_j} \left(a_{r,i}^j \right)^2 \quad (9)$$

where D_j is the duty ratio of the j phase of the SCC and $a_{r,i}^j$ is the ratio of charge flow (in each switch per phase) and the total charge flow. The switching losses due to the charge transfer loss of flying capacitors charge/discharge is modelled in [5]:

$$R_{SSL} = \sum_{i\_caps} \frac{a_{c,i}^2}{f_{sw} C_i} \quad (10)$$

where C_i is the flying capacitor and $a_{c,i}$ is a ratio between the charge flow in each capacitor and the total output charge. For slow switching (SS) frequency, the charge transfer loss dominates over the conduction loss, while for fast switching (FS) frequencies, conduction loss is dominant. The current waveform profile in the flying capacitor of SCC in the SS and FS regions, as well as the behaviour of R_{out} across the switching frequency (f_{sw}) are shown in Fig. 1 [16]. SCCs with integrated flying capacitors can also suffer from additional charge transfer loss due to top and bottom plate parasitic capacitances.

Note that lower charge transfer loss is obtained at higher switching frequencies, however a limit is set by the other switching losses present in the converter. Hence, optimal designs use switching frequencies close to the crossover frequency (f_c). Also note that larger capacitors reduce the level of SS losses as well as larger switches reduces conduction loss. However, this is also in the opposite direction to the fully integrated power converter.

B. Power density

Power density relates the output power to the area occupied by the converter ($P_d = P_{out}/Area$). Thus, achieving large power density depends on the size of passives (capacitors or inductors) and switches, as well as the capacity to stand for the voltage/current required for the application. In SICs, high quality inductors are desired to improve power efficiency, i.e. large inductance values with low DCR. However, on-chip inductors require larger area than discrete components for the same L/R_{DC} ratio. A state-of-the-art integrated inductor have a ratio of 5.2µH/Ω [20] while commercial SMD components can offer inductors of 78.3µH/Ω for the same inductance value and area [21]. Additionally, the energy density for integrated inductors is also lower. For instance, in this previous example, the commercial SMD inductor have 3 orders of magnitude larger energy density (662nJ/mm^2) [21] than the integrated inductor (0.21nJ/mm^2) [20].

In SCCs, large capacitance values reduce the charge transfer loss while integrated capacitors offer higher energy density than integrated inductors. For instance, in standard bulk CMOS commercial technologies, Metal-Oxide-Metal (MOM) can reach densities as high as 450nJ/mm^2 (1.27nF/mm^2), while Metal-Insulator-Metal (MIM) can reach densities of 88nJ/mm^2 (7.05nF/mm^2) [22] at lower bottom plate parasitic capacitances. Moreover, special silicon processes and interposers using deep trench capacitances and ferroelectric capacitors can reach 150µJ/mm^2 (250nF/mm²) [23] and 425µJ/mm2 (105nF/mm^2) [24], respectively. While in SICs, the switches must be rated to withstand the full input/output voltage. In SCCs the number of switches is higher but at lower rated voltage. Using low-voltage switches can offer lower on-resistance per area and operate at higher switching frequencies than switches with higher breakdown voltages (e.g. LDMOS, HVMOS)[14]. For instance, in [25], two stacked low-voltage NMOS switches ($V_{DS,max}$=4.4V) accomplish 2 and 3.6 times lower energy loss than 5V NMOS and 5V PMOS, respectively; and smaller layout area.

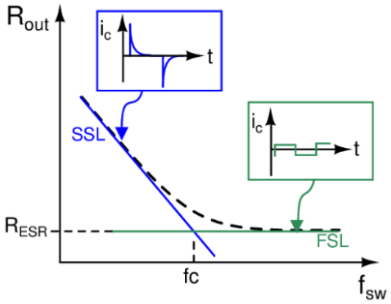

Fig. 1. Output resistance vs. Switching Frequency [16].

There are mainly two alternatives to integrate SICs and SCCs, also followed by HSCs: fully-integrated or highly-integrated. Fully-integrated converters realize the implementation using all the passives on-chip. This is the most challenging option as the passives are limited by low density and large losses in CMOS technologies. Some SICs converters use bond-wire inductors to realize the power inductor as [26]. Highly-integrated converters realize the implementation using external passives, that can be SMD components mounted over the die or dedicated interposers. This technique increases the power efficiency, but it requires special 3D assembly to avoid larger total areas. Although, state-of-the-art of integrated SICs and SCCs shows similar power densities, SICs show lower power efficiency for the same integration level [1]. For instance, state-of-the-art fully integrated SICs can reach power efficiencies up to 80.5% and SCCs show 90% efficiency[1]. Highly-integrated SICs can reach power efficiencies up to 97.4% [27], while SCCs reached 95.7% [1] [28].

C. Voltage Conversion Ratio - VCR

VCR is the ratio between output voltage and input voltage ($m = V_{out}/V_{in}$). It can be classified in step-down (m<1), step-up (m>1) or step-up/down, which enables the converter to provide either $m > 1$ or $m < 1$. The type of VCR depends on the converter's topology. The three types of conversion are possible in SICs. Ideally, SICs can reach any VCR by varying the duty cycle or the switching frequency. However, SICs at high frequencies are limited by the narrow duration of the control pulses in extreme duty cycles, *i.e.* large VCRs.

On the other hand, SCC's topology establishes a fixed-VCR for the converter, either step-down or step-up. Literature mentions three main methodologies to vary the VCR. The first one changes the output resistance, more specifically, R_{SSL} by modifying the switching frequency or the capacitance of the power train. The second strategy is to change the R_{FSL} by modifying the duty-cycle or modifying the on-resistance of the switches through the gate driver's voltage or switches size. These two methodologies adjust the VCR through varying R_{out}, thus its voltage drop. Hence, it limits the maximum power efficiency of the SCC. The third methodology consists of a multi-ratio converter, where the SCC topology changes according to the desired VCR. In this case, the VCR does not vary continuously but in discrete steps; and the complexity and power losses increase with the addition of new switches, drivers, and capacitors [5] [28].

Additionally, based on the power levels of fully and highly integrated converters state-of-the-art, integrated SICs are more suitable for high power levels while SCCs dominate low-power applications [1][28].

III. Trends in HSCs

Based on the previous discussion, HSCs aim to take advantages of the continuous VCR without efficiency penalties of SICs, high energy density of capacitors and low-rated switches of SCCs. State-of-the-art of fully and highly integrated HSCs can be broadly classified in four main topology trends (Fig. 2): Series Capacitor (SC-HSC) [8] [29]-[36], multilevel (M-HSC) [6] [37]- [54], Resonant (Re-HSC) [19] [25] [55]-[57] [60] and Passive-Stacked 3rd-order (PS3-HSC) [61] [62].

HSCs mainly target portable, wearable and IoT applications involving battery power management. However, converters for dedicated applications such as automotive and solid-state lighting (SSL) have also been reported.

A. Series Capacitor HSCs

SC-HSC merges SIC and SCC taking advantage of soft charging (full or partial). Placing a capacitor in series with the power inductor reduces charge transfer loss, extends duty cycle and decreases switching losses and inductor ripple [63, 64]. Step-down SC-HSC is shown in Fig. 3. Step-up SC-HSC is obtained by reversing this topology (exchanging the input by output and vice versa) or connecting one more capacitor in a cross-commutated scheme [34]. This step-down converter works in three phases with two simultaneous current paths (I_{La} e I_{Lb}) in each phase. For this reason, this specific topology is called dual path SC-HSC.

As seen in the previous section, charging a capacitor from a voltage source causes charge transfer loss. This is because of the large capacitor current peaks. In this way, capacitors must be charged/discharged using constant current or constant power methods [30], this is called soft-charging. In SC-HSC, flying capacitor is charged using the inductor that acts as current source, decreasing the charge transfer loss. Additionally, series flying capacitor in Fig. 3 acts as a voltage source of $V_{in}/2$. Then the inductor has half of the voltage variation, meaning that the duty cycle doubles its value for a given VCR, i.e. $D = 2V_{out}/V_{in}$. Consequently, the operating voltage in the components is reduced. Switching losses are also reduced as they are strongly dependant on the operating voltage, as shown in (2)-(5). Likewise, the current ripple of the inductor is also reduced for a given switching frequency, reducing exponentially core loss. Another approach is designing for the same ripple but using lower inductance values. Waveforms of this converter have a similar behaviour of a 2:1 SCC cascaded with buck SIC [64].

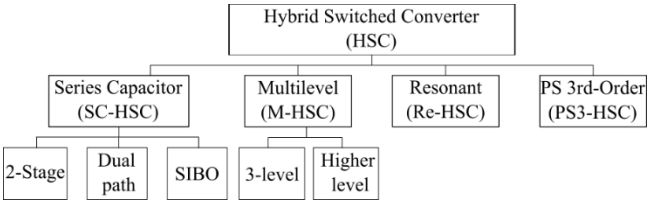

Fig. 2. Classification of state-of-the-art integrated HSCs.

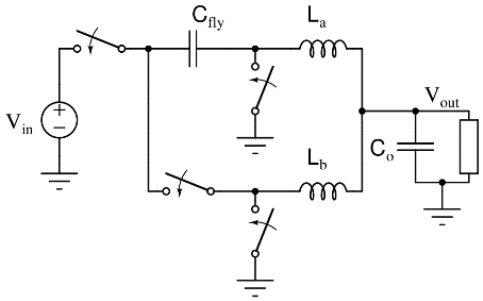

Fig. 3. Step-down Dual path SC-HSC [64]

It is possible to extend this concept to larger VCR SCC ratios cascaded with a SIC stage, i.e. 2-stage SC-HSC. For instance, the 3:1 SCC cascaded with a SIC is shown in Fig. 4 [29]. Here, the first stage is composed by a series-parallel SCC using high voltage (HV) switches at low switching frequency, which steps down the input voltage into an intermediate voltage, V_{unreg}. A second stage is a buck SIC, which performs the regulation of the output voltage, uses low voltage (LV) switches at higher switching frequency. This reduces the size of switches and inductor. In this approach the fast SIC behaves as a constant power load. In series, the SCC flying capacitors are connected to V_{in} through the buck converter. Hence, most of the energy $C(\Delta V)^2/2$ is used by the SIC and delivered to the load. Likewise, soft-charging occurs when the capacitors are connected in parallel if the values of the capacitors (C_1 and C_2) are identical [30].

The 2-stage approach can be applied as single inductor multiple output (SIMO) HSC with two regulated outputs. In [8], a boost SIC first stage is in a LV domain, while a SCC second stage is in HV domain. The first output (and second stage input) is regulated by the SIC, while the second output has a fixed 2:1 VCR. This fully-integrated converter uses 180nm CMOS technology and integrates on-chip flying capacitor (SCC) and output capacitors (SIC). The inductor is designed using bond-wires. The efficiency reaches 77% with a total output of 0.2W. Moreover, this converter has two additional characteristics: (a) a π-filter at the SIC's output, which isolates the noisy power ground from the boost and (b) 11 interleaved SCCs used as second stage, which improves ripples, power efficiency and reduces the output capacitance value of the SIC converter.

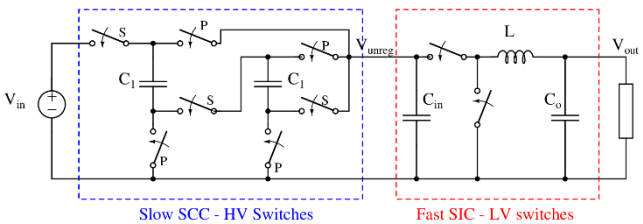

Fig. 4. 2-stage SC-HSC buck. Adapted from [29]

Likewise, single inductor bipolar output (SIBO) HSC uses the dual path SC-HSC principles to realize one positive regulated output (V_{op}) and one negative regulated output (V_{on}). SIBO converters are typically used in OLED displays [31], [33]. The most recent integrated SIBO topology is shown in Fig. 5 [33]. Its operation is based in two phases: build-up (ϕ_b) phase and simultaneous energy transferring (ϕ_{set}). In ϕ_b, the inductor current (I_L) flows from the input to ground charging the inductor. At the same time, flying capacitor (C_f) is charged to V_{in}. In ϕ_{set}, the current from the inductor flows from V_{on} to V_{op} through C_f. Regulation of V_{op} is achieved through the main feedback control of the inductor current. V_{on} regulation is achieved by the delay controller, which generates two additional temporal-phases in the middle of ϕ_{set} and ϕ_b. One phase to only charge/discharge C_{on} (ϕ_{tn}) and another to charge/discharge C_{op} using I_L, therefore increasing V_{on} and V_{op}, respectively. In SIBO SC-HSC, the flying capacitor reduces the voltage applied to the inductor; hence, reducing the current inductor ripple. Consequently, conduction loss is lowered and switching losses are decreased as operation voltage of the switches is reduced. The main characteristics of integrated SC-HSC are summarized in Table I.

B. Multilevel HSCs

The general structure of a M-HSC is shown in Fig. 6. It is based on a SCC (without output capacitor and regulation) capable to deliver n different outputs levels in a switching node (V_x). Switching periodically between two adjacent voltages (V_k and V_{k+1}), a LC low-pass filter extracts the DC level at the output, i.e. the mean value of V_x. The output regulation is made by a closed-loop control. It adjusts the voltage levels that composes V_x through the configuration of the SCC and duty-cycle, i.e. duration of V_x in each level [42].

The voltage amplitude applied to the inductor in M-HSCs is lowered by the number of available voltage levels. This reduces the current ripple, enabling smaller inductor size, lower conduction loss and switching losses. Additionally, the required duty-cycle is more relaxed than SICs at the same switching frequency [49]. The minimum realization is a 3-level M-HSC, as the step-down shown in Fig. 7a. However, literature also reports integrated 3-level step-up [48] and step-up/down [38] [47], 4-level [42] [43] [44], series-parallel [40], Ladder [49], Dickson [37] [6] [53] and Fibonacci [54] based M-HSC.

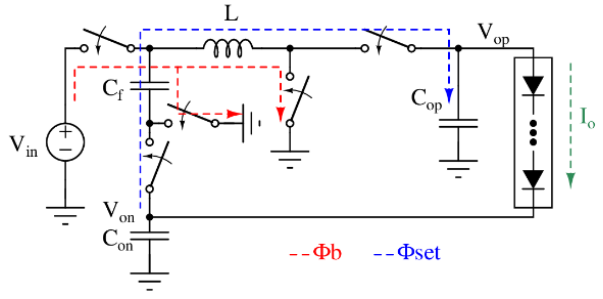

Fig. 5. SIBO SC-HSC. Adapted from [33]

Table I. Integrated SC-HSC summary.

	[32]	[33]	[34]	[51]	[35]	[8]
Year	2018	2020	2020	2021	2019	2021
Topology	Dual Path	DP SIBO	Dual Path	Dual Path	Dual Path	2-stage
Technology (nm)	180	500	350	180	65	180
Integration level	High	High	High	High	Full	Full
V_{in} (V)	2-4.2	3.7	2-4.4	2.8-4.2	1.2	1.2-2.7
V_{out} (V)	3 - 5	4.6/-4.9	9-20	3.3	0.6-0.9	1.4/3.2
F_{sw} (MHz)	1	1.4	2	1	450	120
$P_{out,max}$ (W)	3.1	2.8	5	3.3	0.475	0.2
η_{peak} (%)	95.2	94.1	93.5	96.6	78	77
Area (mm²)	5	1.46	0.86	8.26	0.65	0.82

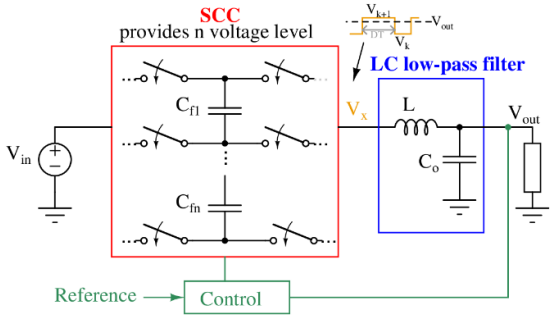

Fig. 6. General M-HSC. Adapted from [42]

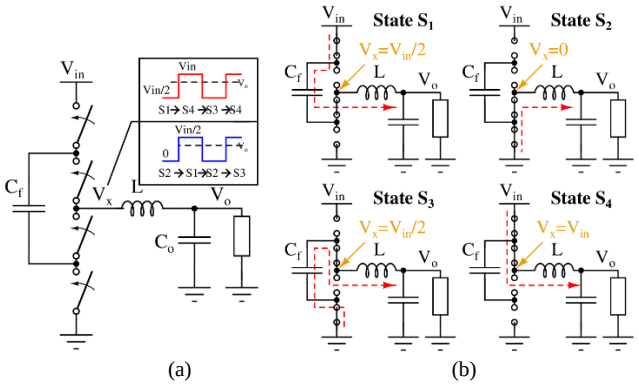

Fig. 7. 3-level step-down M-HSC: (a) basic structure and (b) operation states.

In the 3-level M-HSC, the switching voltage, V_x, can swing between 3 values: V_{in}, $V_{in}/2$ and zero. This operation occurs in 4 states (Fig. 7b). State S_1 and S_3 charge and discharge the flying capacitor through the inductor without charge transfer loss, i.e. soft charging. S_2 connects the switching node to zero while S_4 connects to V_{in}. Using the sequence $S_1 \rightarrow S_4 \rightarrow S_3 \rightarrow S_4$, the output voltage is controlled from $V_{in}/2$ to V_{in}. Whereas, using the sequence $S_1 \rightarrow S_4 \rightarrow S_3 \rightarrow S_4$, the output voltage is controlled from 0 to $V_{in}/2$.

Despite the advantages, M-HSC requires multiple switches that are not referenced to ground or V_{in}. It demands a more complex driving scheme, including level shifters and bootstrap schemes. Also, M-HSC still suffers from relatively high conduction loss because of the several switches connected in series. In higher level converters, this loss is even larger. A recent study in [27] reports a step-up topology

that reduces the number of switches of 3-level M-HSC from 4 to 3. It reports a power efficiency of 97.4%. Also, using NMOS switches leads to lower R_{on} than PMOS switches for the same area; however, when NMOS switch is connected to the input, it requires a gate voltage larger than V_{in} to guarantee its on-state. Typically, larger gate voltages are provided by an auxiliar charge pump or external supplies. On the other hand, using NMOS and PMOS switches simplify the driving scheme at the cost of larger IC area for the same R_{on}. An additional care should be taken when drain (or source voltage) is lower than bulk in the PMOS switches of the M-HSC, because of the potential leakage and latch-up coming from the bulk junctions. Similar situation happens with NMOS switches, where the bulk cannot be at higher potential than the drain or source terminal. To solve this issue, some converters use body-switching [38], where the bulk terminal is dynamically connected to drain or source according to the voltage level conditions. Moreover, some components (switches or capacitors) of the M-HSC may have voltage rating limitation beyond the minimum voltage rating of the converter ($V_{in}/(n-1)$) [49]. This issue requires to use additional stacking or higher voltage devices.

Soft charging requires the series connection of the flying capacitors to the inductor. However, according to the topology, some capacitors can be connected among them without the presence of the inductor. In such cases, the converter exhibits charge transfer loss in some of the flying capacitors. This is the case of the Dickson based M-HSC shown in Fig. 8.

The conventional Dickson structure switches between ϕ_{1A} and ϕ_{2A}. In this two phases, there is partial charge sharing among C_1, C_2 and C_3, because of the capacitor-voltage mismatch. Therefore, complete soft-charging is not achieved. Two additional phases (ϕ_{1B} and ϕ_{2B}) are added in aim to equalize the capacitor voltage mismatch. The sequence is $\phi_{1A} \rightarrow \phi_{1B} \rightarrow \phi_{2A} \rightarrow \phi_{2B} \rightarrow \phi_{1A}$. In this way, after ϕ_{1A}, the inductor charges C_1 and discharges C_2 in ϕ_{1B}. This happens until there is not voltage mismatch, then it goes to the next phase ϕ_{2A}. Similar behaviour occurs with the transition $\phi_{2A} \rightarrow \phi_{2B} \rightarrow \phi_{1A}$. This scheme is called split-phase [6].

Flying capacitors voltage imbalance is considered one of the most critical issues in a practical implementation. This issue happens when the flying capacitor voltage differs from the nominal, causing excessive voltage stress across some switches. Consequently, the switches should be over-rated. Capacitor imbalance can be caused by input source impedance, gate signal delay mismatch and R_{on} variations of the switches [65]. To maintain the balance, gate delays should be equalized, and capacitors' voltages (or inductor current) should be monitored. Then, if the imbalance is detected, the charge or discharge in the flying capacitors increases, e.g. the capacitor-calibrating pulse frequency modulation (ACC-PFM) controller in [54]. Also, phase-shifted pulse width modulation can be used to have natural balance. Natural balance occurs when the voltage imbalance increases the inductor current ripple, which increases the power dissipation in the series resistance in such a way that flying capacitors are charged/discharged towards the nominal value. Further details about natural balancing are given in [65].

The most representative integrated M-HSC in terms of efficiency and power density are summarized in Table II.

C. Resonant HSCs

Re-HSCs reach resonance state when an inductor is connected to the flying capacitor(s) of SCC and switches at the proper frequency. If the switching frequency is at the resonance frequency ($f_o = \frac{1}{2\pi\sqrt{LC}}$), then the inductor shapes the charging current of the capacitor in a sinusoidal form. Based on [66], the output resistance in Re-HSCs follows the expression:

$$R_{out,Re-HSC} = R_{ESR}\pi^2/8 \approx 1.23R_{ESR} \quad (11)$$

where R_{ESR} is the equivalent series resistance. This value is close to the minimum output resistance in SCCs (i.e. R_{ESR}).

Therefore, if the resonance frequency (f_o) is lower than the cross-over frequency (f_C) (in Fig. 1), it is possible to achieve better output resistances compared to SCCs at the same frequency. As shown in Fig. 9, the output resistance of Re-HSC at f_o approaches to the minimum resistance of the SCC, but using switching frequencies of one order of magnitude lower than the crossover frequency of the equivalent SCC [67]. Hence, the switching losses are reduced. This resonance behavior is reached with the addition of inductors that are smaller than the ones used in SICs. For instance, in [68] is used an external PCB inductor as small as 1.1nH.

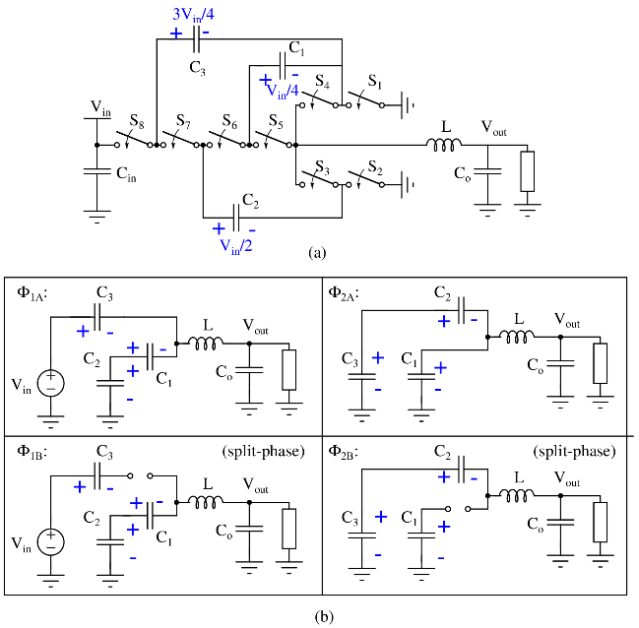

Fig. 8. Dickson based M-HSC: (a) basic structure and (b) operation phases. Adapted from [6]

Table II. Integrated M-HSC summary.

	[38]	[47]	[48]	[53]	[27]	[42]
Year	2017	2020	2020	2021	2021	2018
Topology	3-level	3-level	3-level	Dickson	3-Switch	4-level
Technology (nm)	180	90	65	130	250	65
Integration level	High	High	High	High	High	Full
V_{in} (V)	3.4-4.2	2.5-5	0.3-3	20-60	6	1.2
V_{out} (V)	3.4	0.4-9	2.4-5	3-3.6	30	0-1.1
F_{sw} (MHz)	1	0.8-3	0.5-45	0.32	0.4-2.3	0.3
$P_{out,max}$ (W)	6.8	9	0.33	9.9	36	0.11
η_{peak} (%)	96.6	96.8	96.8	95.3	97.4	93
Area (mm^2)	5.7	2.8	0.28	12.87	0.89	2.34

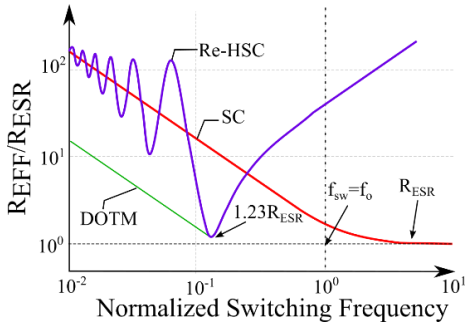

Fig. 9. SCC and Re-HSC output resistance. Adapted from [67]

One should note from Fig. 9 that additional minimum points in the $R_{out,Re-HSC}$ occur at odd sub-multiples of the resonance frequency [66], but at higher resistance values. Thus, basic frequency modulation reduces efficiency depending on the desired output. At light load, it is desired that frequency reduces as load current decreases. In this way, better performance is reached in Discontinuous Conduction Mode (DCM), i.e. adding off-time between the operation phases. This is called Dynamic Off-Time Modulation (DOTM) [67]. Output resistance in DOTM is shown in Fig. 9. Therefore, pulse duration needs to be tuned to turn-off some switches in such a way that the inductor current is kept at zero, otherwise the current turns negative, this is called diode emulation. Also, the typical ramp waveform of the SIC inductor current (Fig. 10a) becomes sinusoidal in Re-HSCs (Fig. 10b), thus zero-currents points can be used to switch the power switches. This is called Zero-Current Switching (ZCS) [3], which reduces the transition loss, P_{tran}, mentioned in (2). To achieve diode emulation, a Zero-Current Detector (ZCD) is required. Typically, this circuit is implemented using voltage monitor, which observes the drain-source voltage (V_{DS}) of one or more switches. At the time that V_{DS} changes polarity, a control signal is generated to turn-off a power switch. Its implementation is described in [55].

In Continuous Conduction Mode (Fig. 10b), Re-HSC regulates the output using additional phases to charge or discharge the inductor, called quasi-resonant behavior [69]. A typical Re-HSC topology is the 3-level M-HSC (Fig. 7) switched at resonance frequency [55] [59] [60]. In general, M-HSC can transition between resonant, quasi-resonant and inductive behavior according to the duty-cycle and switching frequency [3]. In literature has been reported series-parallel [19] [60], ladder [57] and multi-ratio [25] based Re-HSC.

The multi-ratio Re-HSC is shown in Fig. 11. This converter has 3 possible VCRs: 1/2, 2/3 and 1/3. While in 1/2 ratio, all flying capacitors are in parallel; in the other ratios, the flying capacitors are connected in series in one of the phases. Here, all switches and passives are integrated on-chip (C_{in}, C_o, C_{f1},C_{f2} and L). The converter uses switch conductance regulation (SwCR) to tune the output while scaling down the switching losses for low output powers. In this way, the power switch is segmented; i.e composed by an array of transistors stacked switches, level shifters, charge pump and logic, that actives as required. This improves efficiency and output ripple [25]. The most representative integrated Re-HSC in terms of efficiency and power density are summarized in Table III.

D. Passive-stacked 3rd order HSCs

PS3-HSCs focus on the better usage of integrated inductors while preserving the VCR characteristics of SICs. As discussed in section II, integrated inductors tend to have high DCR, so it is advantageous to place inductors in low-current/high-voltage side of the converters, e.g. input side of a buck converter. Step-down PS3-HSC, shown in Fig. 12 [61], places the inductor at the input side and splits the inductor in two. One part on top and another below of the input capacitor. This topology turns the pulsating input current of SICs into a continuous current, which decreases the ripple, thus the conduction loss and reduces the passives area required for filtering. Additionally, PS3-HSC uses only 2 power switches and 3 power pads, in comparison to the 4 switches and 4 pads of the 2-phase buck converters.

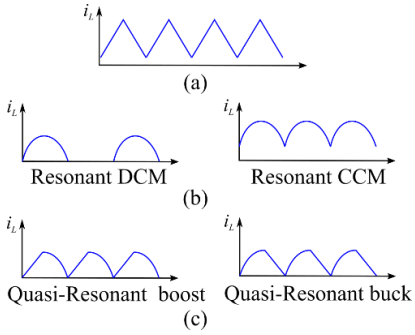

Fig. 10. Inductor current waveform: (a) SIC, (b) DCM and CCM resonant, (c) quasi-resonant.

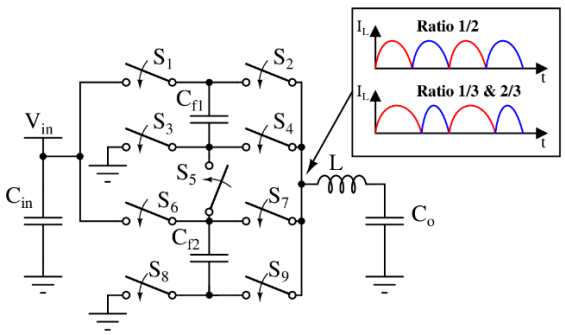

Fig. 11. Fully-integrated Multi-ratio Re-HSC. Adapted from [25]

Table III. Integrated Re-HSC summary.

	[60]	[55]	[57]	[19]	[25]	[59]
Year	2017	2018	2018	2021	2019	2020
Topology	3-level	3-level	Ladder	Series-Parallel	Multi-ratio	3-level
Technology (nm)	180	180	2500	180	130	180
Integration level	High	High	High	High	Full	Full
V_{in} (V)	7.4	5	180	2.3-5	3-4.5	2.4-4.4
V_{out} (V)	3.7	2.8	45.3	10-35	1.5-1.8	1-2.2
F_{sw} (MHz)	0.7	2-6	0.3-0.4	0.1-1	35-50	47.6
$P_{out,max}$ (W)	3.7	2	22	0.22	0.87	3.5
η_{peak} (%)	94.8	93.3	92.2	91.15	85	85.5
Area (mm^2)	10	7.5	14.1	2.76	7.8	8.9

The PS3-HSC works in two phases (Fig. 12). In phase 1 (ϕ_1), L_1 is charged from V_{in} to V_{out}, and L_2 is discharged through C_F, which is discharged too. In phase 2 (ϕ_2), S_2 is closed (S_1 is off) to charge L_2 from V_{out} and L_1 is discharged through C_F, which is charged. The VCR of this converter is $V_{out}/V_{in} = D$, same as the buck SIC, however using 3 reactive elements, i.e. 3rd-order converter [61]. In this topology, power switches in PS3-HSC requires level-shifters and bootstrapping capacitors, which are implemented on-chip. S_1 is a NMOS switch while S_2 is a PMOS, thus two bootstrap capacitors are used to generate the proper gate voltages: $V_{in} + V_{out}$ and $V_{out} - V_{in}$, for the NMOS and PMOS, respectively. To turn-off the power switches, the gate charge is dumped into the source terminal (V_{out}). Also, power switches, bootstrap and flying capacitor can be rated to V_{in}. In addition, the bulk of the IC implementation in [61] is biased at V_{out} instead of ground, this is because power MOSFETs and most of the gate driver are referenced to V_{out}.

The previous PS3-HSC is improved replacing conventional gate drivers by adiabatic charge-recycling (CR) gate driver [62]. Instead of dumping the gate charge (hard switching), it is transferred from one power switch to another using an auxiliar PCB-trace inductor of 4nH (L_R), this is called charge-recycling, as shown in Fig. 13. When S_1 starts to turn-off, S_{11} is activated to discharge the gate charge through the inductor, L_R. After the total discharge of the S_1 gate, S_{11} is deactivated and S_{22} is activated to charge the gate of S_2 from the energy stored at L_R. Then, the drivers are activated to tie the gate voltage level [62]. Charge-recycling technique increases the peak power efficiency and light load. The main characteristics of integrated PS3-HSC are summarized in Table IV.

IV. State-of-the-art comparison

Based on the state-of-the-art for SICs and SCCs in [1] and [28], the follow section relates the maximum peak efficiency with the converter's power density, maximum output power and maximum VCR. Note that a straight comparison between the converters is difficult as it must consider the characteristic of the specific application. Thus, the follow considerations of the state-of-the-art intend to guide design and implementation of HSCs rather than compare each HSC.

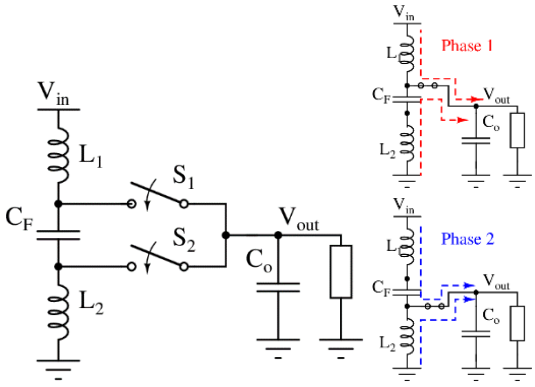

Fig. 12. Passive-stacked 3rd-order HSC (PS3-HSC). Adapted from [61]

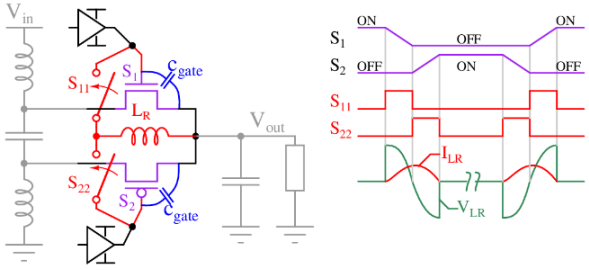

Fig. 13. Charge-recycling in PS3-HSC. Adapted from [62].

Table IV. Integrated PS3-HSC summary.

	[61]	[62]
Year	2019	2021
Topology	PS3 Buck	PS3 Buck
Technology (nm)	180	180
Integration level	High	High
V_{in} (V)	1.8	1.8
V_{out} (V)	0.5 – 1.5	0.3 – 1.5
F_{sw} (MHz)	6.5	3
$P_{out,max}$ (W)	3.75	4.125
η_{peak} (%)	94	98.2
Area (mm^2)	1.85	5.7

In Fig. 14 is shown the state-of-the-art for HSCs, classified by the four types of converters. As discussed in section II, the performance of the converter is highly dependent on the integration level of the converter, for this reason, a comparison among the HSCs requires attention to distinguish between highly-integrated HSCs and fully-integrated HSCs. The last ones are identified with a red border.

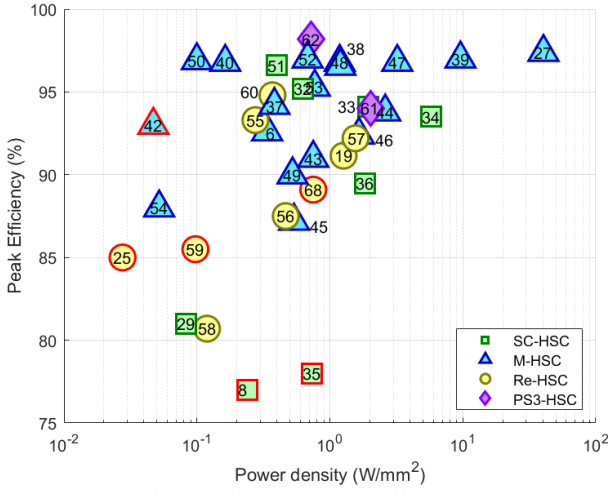

Fig. 14. State-of-the-art form HSCs: Peak efficiency vs. Power density.

Fully-integrated HSCs show a maximum of 93% power efficiency, achieved by a 4-level M-HSC. The best power density is achieved by a Re-HSC and SC-HSC 0.73W/mm^2 and 0.7W/mm^2, respectively. No fully-integrated PS3-HSCs have been reported. Also, most of the fully integrated HSCs of this review switch at frequencies larger than 35MHz. Moreover, in the last 5 years, 65nm to 180nm CMOS technologies are mostly used for the implementation of fully-integrated HSCs. Their capacitive components are implemented on-chip using triple MIM (6.6nF/mm^2) [68], simple MIM (2.3nF/mm^2) or MOS (9-10nF/mm^2) capacitors [42] [35]. The inductors were constructed using top metal layer [35], bond-wires [42] or PCB connection form by filled-vias and the pads of a flip-chip die [68]. In contrast, fully-integrated SIC state-of-the-art converter reports 80.5% peak efficiency and a power density of 0.17W/mm^2 [28]. This translates in a state-of-the-art improvement of 12.5% in power efficiency and 4 times more dense converters. In terms of fully-integrated SCC state-of-the-art, the maximum efficiency can reach 90%, while power density extends up to 1W/mm^2, using conventional silicon technology and 2.191W/mm^2, using trench capacitor technology [28]. This means 3% more power efficient and 0.7 times less dense converters.

On the other hand, highly-integrated HSCs reaches up to 98.2% power efficiency, achieved by a PS3-HSC. While the power density reaches up to 40W/mm^2 using M-HSC converter intended for SSL. Small SMD components are used to provide the passives of the topologies, sometimes even stacking the SMD components directly on top of the die [67]. In Fig. 14, it is possible to observe the dominance of M-HSC research in HSCs. However, comparison of efficiencies and power densities in a fair way is not possible, as the number and sizes of the external passives are not always reported, and their characteristics change broadly according to the intended application. For the sake of illustration, if the passive interposer size of [62] is considered, the power density will be almost unaltered (0.7W/mm^2). However, if in [19] is considered the footprint area of the SMD inductor in the total area, the converter reduces its power density 8 times. In a similar way, considering the total area of the M-HSC implementation in [44], the power density reduces by a factor of 13 times. Additionally, in the last 5 years, highly-integrated HSCs are fabricated in larger variety of CMOS technology nodes from 22nm up to 2.5µm.

The reader should note that power density of state-of-the-art fully-integrated HSCs is at the same order of magnitude than the highly-integrated HSC with the best efficiency, but with a power efficiency penalty of 8.7%.

Fig. 15 relates the peak efficiency with the maximum output power of HSCs. A wide range of output power is attended by M-HSC, reaching a maximum of 240W (intended for automotive and high current distributed power systems [39]) and a minimum of 0.11W (intended for portable and wearable applications [42]). Re-HSC also attends a broad range of output power from 0.2W to 22W (intended for portable oriented electronics, SSL and automotive applications), but with lower efficiency than M-HSC. Alternatively, SC-HSC and PS3-HSC tends to be limited to tens of watts focusing on portable applications and AMOLED displays, respectively. Fully-integrated HSCs covers the output power range from 0.11W to 6.3W. In perspective, state-of-the-art fully-integrated and highly-integrated SICs can achieve large output powers of 1W and 36W, respectively, and a minimum output power of 0.1W [1]. On the other hand, state-of-the-art fully-integrated SCCs covers a lower range of output power from 250µW to 1.65W [1].

The relation peak efficiency vs. maximum VCR that HSCs achieved is shown in two figures. Fig. 16 shows the step down converters as well as the maximum VCR of step-up/down HSCs using $m \leq 1$. Fig. 17 shows the step-up converters as well as the maximum VCR of step-up/down HSCs using $m > 1$. Note that this information relates the maximum peak efficiency (for any VCR) with the possible maximum VCR that the converter can achieve. A more suitable metric will be the power efficiency for the maximum VCR, however, this information is not always provided in literature.

The state-of-the-art highly-integrated HSCs offers converters able to perform the three types of conversion. The four types of converters show implementations with step-down ratios, while only three types of converters offer step-up ratios. To our knowledge, step-up or step-up/down integrated have not been yet introduced using PS3-HSC topologies. Extreme step-down VCR of 0.01 (100:1) is achieved by the Re-HSC in [58], with peak efficiency of 80.7%. HSCs with higher efficiencies (more than 95%) are achieved from a VCR of 0.07 (14:1) using M-HSCs. Fully integrated M-HSC can achieve a maximum of 0.08 (12.5:1) conversion ratio. In terms of step-up conversion, the automotive aimed M-HSC with 95.3% efficiency reaches an extreme VCR of 20 (1:20).

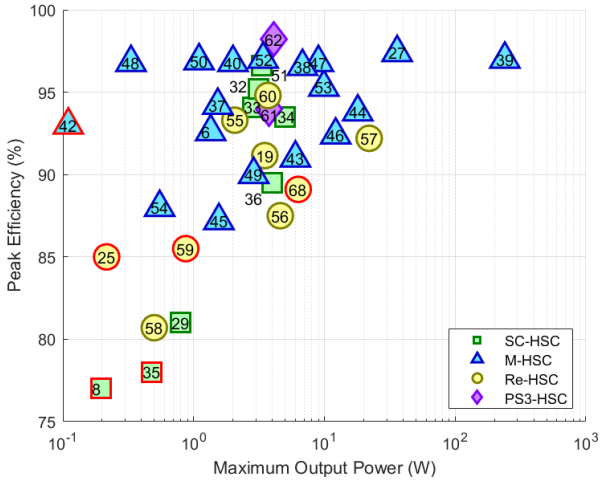

Fig. 15. State-of-the-art form HSCs: Peak efficiency vs. Max. output power.

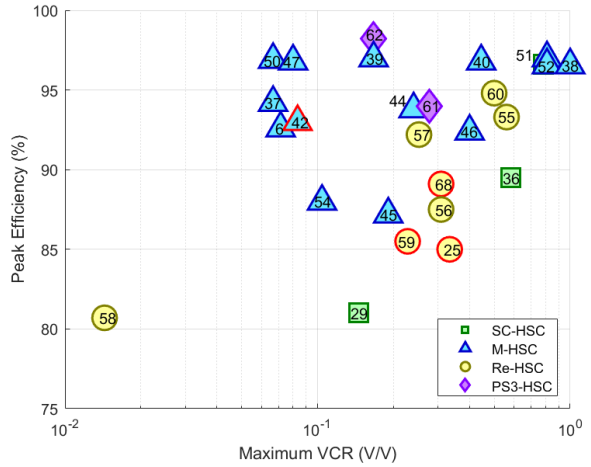

Fig. 16. State-of-the-art form HSCs: Peak efficiency vs. maximum VCR: step-down conversion.

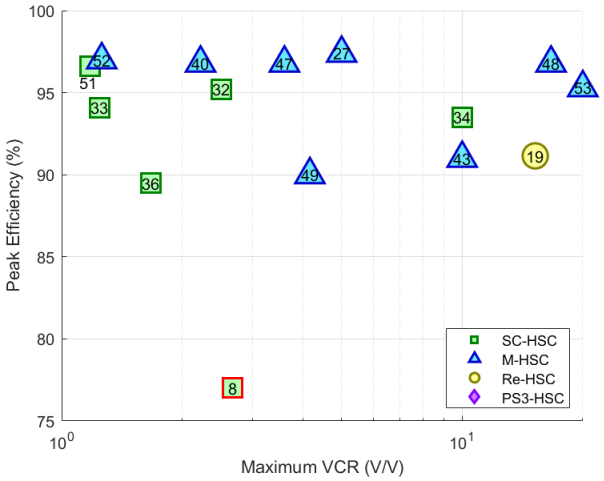

Fig. 17. State-of-the-art form HSCs: Peak efficiency vs. maximum VCR: step-up conversion.

V. Conclusions

This paper introduces the state-of-the-art of fully-integrated and highly-integrated HSCs. It identifies four main trends for HSCs topologies: Series-Capacitor (SC-HSC), Multilevel (M-HSC), Resonant (Re-HSC) and Passive-Stacked 3rd-order (PS3-HSC). The improvements in relation to SICs and SCCs are focused on three characteristics: power efficiency, power density and voltage conversion ratio. State-of-the-art benchmarking shows fully-integrated converters up to 93% efficiency, covering applications in a power range from 0.11W to 6.3W with a power density limitation of 0.7W/mm^2. Also, it shows highly-integrated converters up to 98.2% efficiency, 40W/mm^2 in a broad power range of output power applications. M-HSCs show to be able to perform at higher than 95% power efficiencies in a wide range of output power. Re-HSCs and SC-HSC are the dominant topologies for fully-integrated applications, while M-HSCs are predominantly highly-integrated. Also, high-order converters as PS3-HSC have risen as a new trend in HSC in the last years. Its efficiency reaches the state-of-the-art while the power density and output power follow the trend of other topologies. Also, System-In-Package (SIP) implementations allow to use high quality passives in a limited space. HSCs use interposers with the passives or discrete passive components on top of the die as an alternative to on-chip passives. Finally, the HSCs have been proved in portable, wearable, solid-state lighting, and automotive applications.

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