A Review of Offset and Noise Reduction Techniques for CMOS Amplifiers

Carlos A. dos Reis Filho

Universidade Federal do ABC, Santo André, SP, Brasil
e-mail: carlos.reis@ufabc.edu.br

***Abstract*—Input referred offset voltage, 1/f noise and thermal noise are amplifier properties that directly restrict the ability of discerning signals beyond a certain limit. The ever-increasing spectrum of applications of integrated circuits and trends in the semiconductor market have pushed engineers to design circuits with successively lower voltage, less power consumption, higher dynamic range, accurate gain and wider bandwidth, preferably altogether. Amplifiers input errors are key properties, which have to be minimized; however, with the least negative impact upon the other equally important properties. This paper reviews some of the most relevant techniques applied to reducing input errors of CMOS amplifiers, aiming to provide a condensed set of information that can help designers at the starting point of a new design of a precision analog circuit. The focus in all cases that were selected to be studied in this review work was the reduction of offset and noise regardless of any commitment of the used technique with other characteristics of the amplifier and its impacts on figures of merit like NEF and PEF.**

***Index Terms*—Amplifier; CMOS; Precision analog; Noise.**

I. INTRODUCTION

The design of analog front-end circuits that precede the digitalization of signals upcoming from sensors of diverse nature, biological sources and the like, whose amplitudes span ranges of microvolts or millivolts around common mode voltages that take on any value within the power rails, is a frequent demand for IC-design engineers. The ever-increasing requirements particularly in higher resolution, lower voltage operation and lower power consumption, aggravate the difficulty of discerning signals amid noise and yet upgrade the overall performance of the front-end circuitry. The key component of the front-end stage, in this case, is an instrumentation amplifier, which, by definition, features differential input, high CMRR and bandwidth, accurate gain, low input referred offset voltage and low noise, in addition to other properties that make it suitable for processing signals with the above mentioned characteristics. The interdependences among these properties often call for sacrificing some of them in order to optimize others. Furthermore, there are few or no applications which ultimately require an overall perfect amplifier. Among the many properties of an instrumentation amplifier, two are directly related to the capacity that the addressed system has to discern signals; i.e., its resolution: the input referred offset voltage and noise. Offset is an imperfection that outcomes from circuit design and fabrication, while noise is due to the very nature of the transistors. Therefore, efforts have been constantly devoted to developing mechanisms to repair these imperfections and to reduce their influences upon the overall performance of front-end stages. A few decades ago, when bipolar technology was dominant in the fabrication of analog ICs and circuits operated essentially in continuous time, important process and design techniques were developed to mitigate those problems. Laser trimming [1], common-centroid layout [2], averaging, and proper gain sorting in multi-stage circuits [3] are examples of techniques that allowed to accomplish (commercial) amplifiers with offset voltages of a few microvolts, voltage noise density below 10nV/√Hz (at 0,1Hz) and CMRR in excess of 120dB [4]. Current switching and current steering, normally used in the design of earlier monolithic DACs in bipolar technology, were techniques further expanded to other applications that benefited from signal averaging. Despite the poor performance of BJTs as analog switches, the concept of switching applied to interchange elements of a network formed by or divided into nearly equal elements as a means to accomplish resulting signals with values more accurate than the accuracy of the undivided or basic network originated the so-called Dynamic Element Matching technique [5]. DEM soon became an indispensable practice in the design of precision analog circuits.

The superior performance of MOS transistors as analog switches compared with BJT's was an important contributing factor in the merging of analog and digital onto a single chip, thus consolidating the dominance to date of CMOS technology, by providing means to implement mixed-signal systems with precision analog. High-performance instrumentation amplifiers, specially of the type used to implement the analog front-end of integrated systems, are currently designed incorporating auto-correction mechanisms. This paper reviews the most relevant design techniques to improve the performance of front-end amplifiers in the latest years, with particular focus on the reduction of offset and noise.

With regards to the organization of this paper, Section II briefly describes the amplifier architecture that has been mostly adopted in successive state-of-the-art precision amplifiers in the last decade, a reason why most of the techniques reviewed in this work refer to it. Section III summarizes the concepts of auto-zero and chopper stabilization and discusses critical issues associated with these techniques, which designers have tackled in order to achieve results progressively better over time. Section IV reviews the most significant recently developed solutions. The paper ends with some conclusions in Section V.

II. FRONT-END AMPLIFIER

A comparative assessment of instrumentation amplifier architectures used in the design of integrated systems dedicated to conditioning low-level signals suggests that the

Digital Object Identifier 10.29292/jics.v17i1.572

current feedback instrumentation amplifier is the one that gathers most of the fundamental functional requirements for the role [6]. For this reason, it has been the preferred amplifier architecture used at the front-end of high-precision integrated systems since it was first proposed in [7] as an "indirect feedback instrumentation amplifier". The basic structure of the amplifier comprises transconductance stages G_{m1} and G_{m2} and a high-gain loop amplifier A interconnected as shown in Fig. 1.

Assuming that $A.R_0 \rightarrow \infty$, the corresponding transfer function is given by:

$$\frac{V_{out}}{V_{in}} = \frac{G_{m1}}{G_{m2}}\left(1+\frac{R_1}{R_2}\right) \quad (1)$$

Notice that the accuracy of the overall gain does not require accurate absolute values of the transconductances, but rather the ratio of them, as well as of the ratio of the gain setting resistors. As a result, matching of the two transconductance stages is of crucial importance in its design.

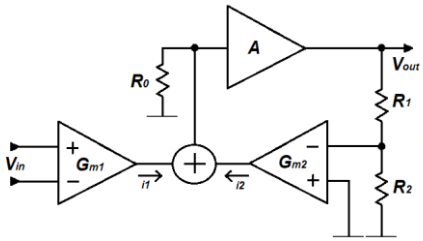

Fig. 1: Simplified structure of the indirect feedback instrumentation amplifier

Another particular virtue of this amplifier architecture is that in addition to providing high input impedance, the input terminals are coupled to the feedback summing node through a high impedance path, which intrinsically allows the input voltages to span over a large range, thus enabling the amplifier to achieve high CMRR. Lower impedance coupling, as occurs in the classical resistive feedback instrumentation amplifier, implies in CMRR strongly dependent on matching of the resistors network [8]. In capacitively-coupled instrumentation amplifiers [9], which normally feature very low power consumption and competitive performance in comparison with its current-feedback counterpart regarding the amplification of low-level signals, the input impedance depends on the input capacitors and switching frequency, being therefore limited to lower impedance levels. The capacitively-coupled amplifier architecture is more appropriate for conditioning biopotential signals [10-15], since it rejects DC offsets generated at the electrode tissue interface. The use of high performance capacitively-coupled amplifiers in applications other than biopotentials has also been reported [16-17] and there are prospects that in the coming years this architecture may become dominant in the design of analog front-end circuits due to the ever-growing concern on energy consumption.

A review of the literature reveals that in the last decade the incremental improvements in performance of current-feedback instrumentation amplifiers, which have been used in a wide spectrum of applications, mainly result from the development of mechanisms devoted to reducing the detrimental effects that outcome from applying auto-zero and/or chopper stabilization, which are the two most used techniques to minimize input referred errors, namely offset and 1/f frequency.

III. AUTO-ZERO AND CHOPPER STABILIZATION

Auto-zero is a well-known widespread error correction technique in which a capacitor is used to hold the voltage that remains either at the input or output of the amplifier, while the input terminals are short-circuited, thus memorizing the instantaneous error. While this happens, the output samples a constant value (e.g., zero). In a subsequent time cycle, the memorized error is subtracted from the error-affected signal. During this time, the output follows the input signal with constant level shifting. So, in one phase the output samples a constant value, and in the other phase it operates in continuous time. Alternatively, in one phase the input signal is directly connected to the amplifier, so that the signal to be amplified is $V_{in}[t]+V_{error}[t]$ and the amplified signal is then memorized. In a subsequent phase, the polarity of the input signal is inverted and the new signal at the amplifier input is $-V_{in}[t+\Delta t]+V_{error}[t+\Delta t]$. By subtracting two consecutive output values, the offset component of V_{error} is zeroed. If the sampling frequency is much higher than the amplifier corner frequency, consecutive samples of the 1/f noise are strongly correlated, therefore 1/f noise is also canceled, or drastically reduced. The auto-zero technique, in this case, is often named correlated double sampling. A subtle distinction between this and the firstly described autozeroing mechanism is that in the correlated double sampling there is no continuous-time period.

Clearly, the auto-zero technique is efficient at canceling out any constant error, like offset voltage, and greatly reduces random time-varying errors, as is the case with 1/f noise. However, due to the signal-sampling nature of the technique there occurs an increase of the noise power spectral density in the range from *0* to f_{AZ} (auto-zero sampling frequency) part of which is due to the foldover components of all the tails of the 1/f noise, despite its narrow band, and part due to aliasing of the wideband thermal noise.

Fig. 2 illustrates the effect of auto-zero on the input referred noise PSD [18-20]. A detailed analysis of the auto-zero technique [21] shows that the resulting value of the input referred noise PSD up to twice the Nyquist frequency is larger than the original thermal noise PSD by a factor that is equal to the ratio of the equivalent noise bandwidth to the Nyquist frequency.

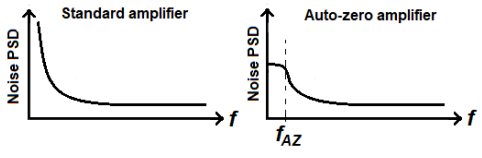

Fig. 2: Noise PSD reduction as a result of auto-zero.

The auto-zero technique is more efficient when the storage capacitors are large and the noise at the amplifier input is low. Larger capacitors, though, means increased chip area and more current consumption. The input noise can be reduced by increasing the amplifier bias current. Hence, auto-zero is not always advisable when either chip area or power consumption are design priorities. An uncommon yet effective means to reduce 1/f noise in MOS transistors consists in alternating the bias current so that it changes constantly between inversion and accumulation mode [22].

Chopper stabilization is a long standing technique based on switching modulation used to cancel out low-frequency errors in amplifiers. Roughly, chopper stabilization consists in moving the input signal band, which starts at DC, to a higher frequency region of the spectrum, amplify it, and move it back to the origin. Some vacuum tube amplifiers already implemented the very same basic concept as a means to accomplish zero stability (zero output for zero input) and gain stability as well [23-24]. Even before that, a description of the chopping stabilization principle appears in the patent for an electromechanical recording device [25].

Fig. 3 shows an amplifier with gain G_m and input error $e(t)$ with two sets of cross-coupled ideal switches, one at the input and the other at the output, which are driven by a two-phase clock, *CK(t): CK1/CK2*, with frequency f_{CHOP}, along with the shapes of the signals in the front side of the amplifier.

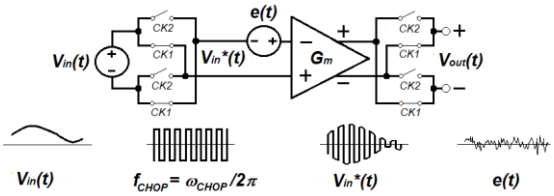

Fig. 3: Basic components of a chopper-stabilized amplifier

When the polarity of the input signal is periodically inverted by alternating the terminals of its source with the cross-coupled switches, the frequency band of the signal is moved upwards in the spectrum and replicated around odd multiples of the switching frequency, reminding that this is the result of modulation, i.e., the multiplication effect of the input continuous time signal $V_{in}(t)$ by $CK(t)$:

$$V_{in}^{*}(t) = V_{in}(t) \times CK(t) \quad (2)$$

where:

$$CK(t) = \frac{4}{\pi}\left[\cos(\omega_{CHOP}t) - \frac{1}{3}\cos(3\omega_{CHOP}t) + \frac{1}{5}\cos(5\omega_{CHOP}t) - \ldots\right] \quad (3)$$

The modulated signal $V_{in}*(t)$ is added to $e(t)$ and conveyed to the output of the gain stage G_m, where another periodical inversion of polarity synchronized with the first occurs to eventually produce $V_{out}(t)$.

This second polarity-alternating stage, or demodulation, causes the frequency band of the amplified input signal $G_m.V_{in}*(t)$ to move back to the origin while the frequency band of the amplified error $G_m.e(t)$ is replicated around f_{CHOP} and its odd multiples, as Fig. 4 illustrates in the frequency domain.

The modulation of $G_m.e(t)$ results in a square wave (ripple) with frequency f_{CHOP} that is further added to switching-induced spikes, which are intrinsic to MOS switches, namely charge injection and clock feedthrough [26]. Ideally, these components would be eliminated by low-pass filtering, but often they still cause a residual offset at the output. The noise at the baseband is essentially thermal noise, with a nearly constant PSD whose value increases, tending to the value of the input thermal noise, as the ratio of the amplifier cutoff frequency to the chopping frequency increases [21].

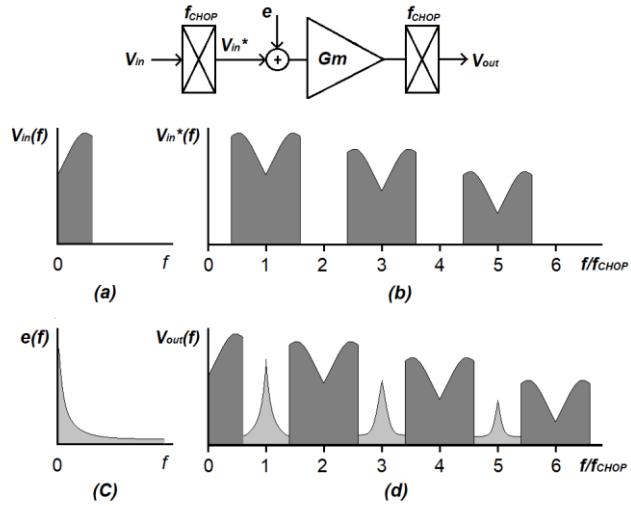

Fig. 4: Chopper-stabilized amplifier signals in the frequency domain

IV. OFFSET AND NOISE REDUCTION TECHNIQUES

The available explicit knowledge about the limits and issues of auto-zero and chopper stabilization techniques, as roughly outlined above, was crucial to devising design strategies in order to realize successively improved precision amplifiers in CMOS technology.

A. Chopper Stabilization and Notch Filtering

Given that the main limitations of the chopping technique are the resulting noise and ripple with frequency f_{CHOP} at the amplifier output, a solution was described in [27], in which a notch filter tuned at f_{CHOP} is used to reduce it. Fig. 5 shows the simplified diagram of a circuit that provides two parallel paths for the differential input signal: a high-frequency path with gain G_{m4} and a low-frequency path that includes a chopper amplifying stage with gain G_{m1} followed by a notch filter and two other cascaded gain stages. The circuit derives from a continuous-time amplifier with the same basic structure, but excluding the choppers and the filter [28]. In its original version, the three gain stages that build up the low-frequency path are frequency compensated employing a Nested Miller technique [29]. Since amplifier G_{m1} contributes more to the propagation of noise, the bias current was increased, thus compromising the overall power consumption. Chopping and filtering were so introduced as

a solution to reduce consumption and yet preserve low output noise. Notice in the circuit of Fig. 5 that a chopper-stabilized amplifying stage now replaces the mentioned over-biased gain stage, while a notch filter, implemented with switched-capacitor technique, is used to suppress all spurs in f_{CHOP}. The DC precision of the amplifier is determined by the low-frequency path, while the high-frequency response and phase margin are taken over by G_{m4}. Measured amplifiers, which implemented this technique showed an input offset of 2uV and 55nV/√Hz of noise PSD from DC to 20KHz.

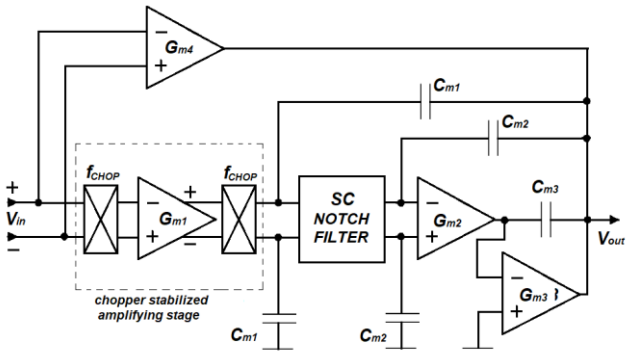

Fig. 5: Chopper stabilized amplifier with notch filter

A clear fragility in the circuit in Fig. 5 resides in the fact that the offset and *1/f* noise that appear at the output of the chopping stage as a square wave is feed forwarded to the output of the amplifier through the Miller compensating capacitor. As a remedy to this issue, in [30] a buffer A_1 is inserted between the amplifier output and C_{m1}, which blocks that path in the direction towards the output, as shown in Fig. 6. It is further suggested to use a continuous time notch filter instead of a switched capacitor. In that case, since the frequency response of the filter depends on the values of resistances and capacitances, whose drifts would affect the filter tuning frequency, it is recommended to generate f_{CHOP} with an RC oscillator, with matched resistors and matched capacitors so as to ensure that the filter tuning frequency tracks the chopping frequency.

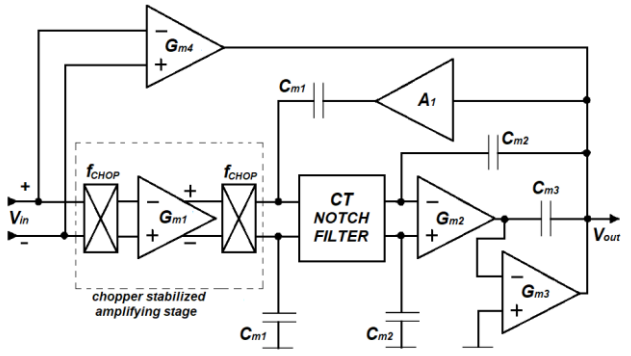

Fig. 6: Chopper stabilized amplifier with CT notch filter and feed-forward blocking buffer

A notch filter was also used to suppress offset and ripple at the output of a chopper stabilized amplifier, whose simplified diagram is shown in Fig. 7, [31-32] by nulling the low-frequency unwanted signal components at the input of chopper X_2, since there resides the root cause of the output ripple. The devised approach includes a closed-loop controller that senses the ripple and tries to null it by adding a correction signal to the input of chopper X_2.

Notice that the signal at the output of chopper X_2 is $(G_{m1}.V_{in})$ summed with a square wave with frequency f_{CHOP} and amplitude determined by the errors from G_{m1}. After being amplified by G_{m3} and modified by chopper X_3, the signal is composed of a slowly varying DC term that equals the sum of the input errors from G_{m1} and G_{m3} added to a square wave whose amplitude is V_{in} and frequency f_{CHOP}.

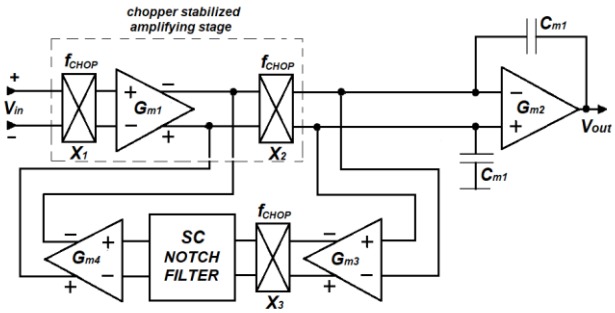

Fig. 7: Simplified diagram of the auto correction feedback approach

When this signal passes through a notch filter tuned at f_{CHOP}, only the error term remains, which, in this case, is subtracted from the input of chopper X_2, thereby zeroing the ripple at the output of the amplifier. Measured samples of an amplifier that implements this technique showed an offset voltage with a typical value of 1.3uV and worst value of 10uV and a voltage noise density of 95nV/√Hz.

B. Chopper Stabilization, Filtering and Spread-Spectrum Chopper Clock

A closed-loop-controller approach was also used in the design of a wideband precision amplifier described in [33]. The transfer function of the amplifier is defined by two signal paths: a high-frequency path with components G_{m0} and G_{m1} and a low-frequency path, which includes choppers X_1-X_3 and gain stages G_{m2}-G_{m6}. It is particularly interesting to focus on the dynamics of the LF path because it is responsible for the offset and noise characteristics of the amplifier.

Similar to the previous cases reviewed in this section, the simplified block diagram in Fig. 8 shows a chopper stabilized amplifying stage whose output voltage is the sum of the amplified input signal with a square wave of frequency f_{CHOP} and amplitude equal to the amplified errors at the input of G_{m2}. The bandpass filter defined by G_{m5} and the associated resistors and capacitors both at its input and output, confines the output voltage to a limited frequency band around f_{CHOP}. The resulting voltage signal in then demodulated by chopper X_3, producing a low frequency current signal by way of G_{m6} that is subtracted from the error-contaminated signal. The described closed-loop control reduces significantly the amplitude of chopper-induced ripple at the amplifier output.

The ripple canceling process, in this case is further improved by replacing the normally used fixed-frequency

oscillator that drives the choppers by a spread-spectrum generator, so that the clock frequency varies continuously between 50KHz and 150KHz. It is worth noting that this measure does not affect the amplitude of the ripple, but it decreases the spectrum density, thus decreasing the chopping noise and its harmonics.

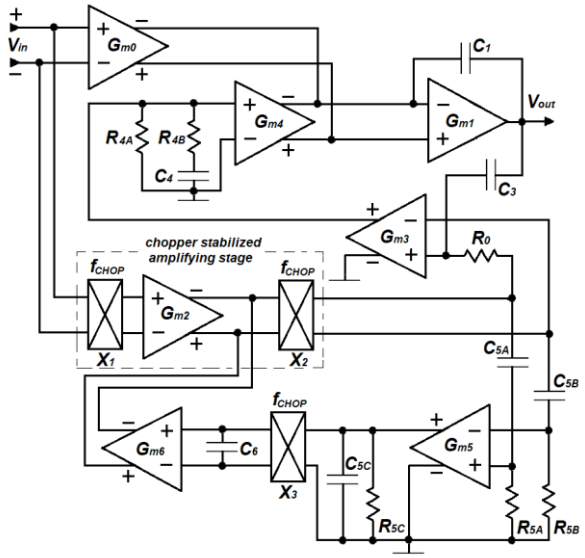

Fig. 8: Chopper stabilized amplifier with BP filtering and spread-spectrum clock

Amplifying stages G_{m3} and G_{m4} are part of a circuitry, not completely shown, that adjusts the transition of signals between the LF and HF bands and also reduces the amplifier settling time.
Measured samples of the amplifier showed an offset voltage of 3.5uV and noise voltage PSD of 6.5nV/√Hz.

C. Auto-zero and Chopper Stabilization

A combination of auto-zero and chopper stabilization was first reported in [18] describing a CMOS amplifier that achieved an offset voltage of 3uV, 20nV/√Hz of input noise density at DC and a unity gain bandwidth of 2.5MHz. The autozeroing section of the amplifier was implemented using a ping-pong structure [34], inserted between two choppers. The ping-pong autozeroing circuit enabled the amplifier to operate in continuous time by using two auto-zero stages that run parallelly in alternated mode, i.e., while one stage is disconnected from the signal path and memorizes its offset, the other stage subtracts the offset that was memorized in the previous phase from the offset-containing signal, thus delivering an offset-free signal at its output. Nulling the offset prior to demodulating with the second chopper, practically cancels out the chopper induced ripple at the amplifier output. The simplified block diagram in Fig. 9 shows how the signal components are modified in a ping-pong chopping structure: The first chopper simply moves up the signal in the spectrum so that it is replicated around the odd harmonics of the chopping frequency. The so-modulated signal is added to all unwanted components at the input of the ping-pong auto-zero circuit, namely V_{os}, *1/f* noise, and thermal noise.

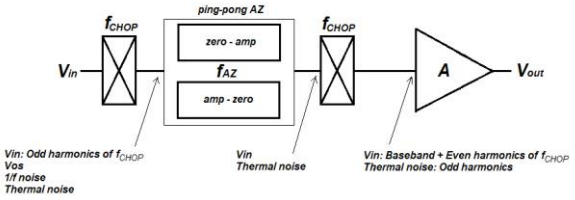

Fig. 9: Simplified block diagram of a ping-pong chopper structure

As already explained, V_{os} is zeroed and *1/f* noise is very much attenuated. The remaining unwanted component at the output is thermal noise, whose PSD value in the baseband is about the same as the PSD value in the baseband that outcomes in a chopper stabilized amplifier.

The improved performance comes at the cost of larger chip areas and increased power consumption, since the auto-zeroing circuitry is duplicated.

The same conceptual approach, ping-pong auto-zero combined with chopper stabilization, was later adopted in the design of a current-feedback instrumentation amplifier [35] in which one particular system-level difference calls more attention: a full auto-zero cycle is done within one half cycle of chopping. In other words, $f_{CHOP}/f_{AZ}=0.5$, while in previous designs [18-20, 36] $f_{CHOP}/f_{AZ}>1$. In general, $f_{CHOP}/f_{AZ}=2$ was the criterion to follow. As a consequence, the undersampled thermal noise with bandwidth limited by f_{AZ} is moved upwards in the spectrum with replicas around the odd harmonics of f_{CHOP}. At the same time, the original noise PSD around f_{CHOP} is moved down to the origin. Clearly, this criterion is satisfactory to the extent that the remaining noise PSD at DC is low enough for the intended application. However, chopper transitions during a full auto-zero cycle, as it happens when $f_{CHOP}/f_{AZ}=2$, may add some undesirable offset at the output, since the amplifier has finite bandwidth. This error is completely avoided if the frequency ratio is inverted because no chopper transition ever occurs during a full auto-zero cycle. On the other hand, at frequency $f_{AZ}/2$, noise is undersampled and moved downwards to the origin by the chopper, which may eventually result in increased noise at DC. This undesirable side-effect can still be fixed by reducing the noise bandwidth at the region where it would increase. For this end, in [35] it was used a slow-settling zeroing loop. Theoretically, the described new approach should result in better values for both offset and noise PSD at DC. Nevertheless, the reported values of offset voltage and input noise, 2.8uV and 27nV/√Hz, respectively, are very close to the values that were obtained in the previously mentioned amplifier.

In an alternative approach that also combines auto-zero with chopper stabilization [37-38], the chopper at the output of the front gain-stage is replaced by a correlated double sampling autozeroing block formed by an array of capacitors as shown in Fig. 10.

Since there occurs no more chopping of the amplified offset, no ripple is produced.

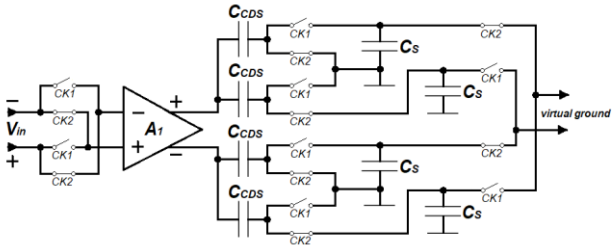

Fig. 10: Chopper stabilization combined with CDS auto-zero

A simple explanation of how the proposed amplifier works can be given considering the status of voltages and capacitor charges in each one of the two clock phases. The analysis assumes that all capacitors with the same name are equal and that the virtual ground at the output is ideal. That said:

In phase *CK1*:

$$Vo(1) = A_1\left[-Vin(1) + Vos + Vn(1)\right] \quad (3)$$

$$Q_{C_{CDS}}(1) = -Vo(1)\cdot C_{CDS} \quad \text{and} \quad Q_{C_S}(1) = 0 \quad (4)$$

Vo, Vos and Vn are the output voltage, offset voltage and input noise of A_1, respectively.

In phase *CK2*:

$$Vo(2) = A_1\left[Vin(2) + Vos + Vn(2)\right] \quad (5)$$

$$V_{C_S}(2) = C_{CDS}\frac{-Vo(1) + Vo(2)}{C_{CDS} + C_S} \quad (6)$$

The sampled output voltage is:

$$V_{C_S}(2) = \frac{A_1 C_{CDS}}{C_{CDS} + C_S}\left[Vin(1) + Vin(2) - Vn(1) + Vn(2)\right] \quad (7)$$

The above equation shows that the remaining error is significantly reduced when noise is correlated, as is the case with *1/f* noise. On the other hand, there is an increase in the noise PSD due to thermal noise. This effect was attenuated in the proposed solution by forging a bandpass frequency characteristic to A_1, i.e., reducing the gain at low frequencies. Measurements with samples of an amplifier designed with basis on this technique showed a voltage offset standard deviation of 1.94uV and an input noise density of 37nV/√Hz.

D. Chopper Stabilization with Integrated Automatic Differential-Pair Trimming

Any mismatch of the differential pair of transistors at the input of an MOS amplifier gives rise to an error at the output with an amplitude that is directly proportional to the amplifier gain. Therefore, reducing the mismatch of the differential pair is a means to accomplish a cleaner signal at the amplifier output. Based on this reasoning, in the technique described in [39] the usual single pair of transistors is replaced by two arrays of equal transistors. Six paralleled transistors connected to the inverting input and six others to the non-inverting input. Each individual transistor can exchange position with another one from the opposite side by means of a digitally-assisted circuit named Calibration Logic that controls the devices that interconnect the transistors to each input side. As such, the 12 transistors can be arranged in 924 different combinations, which are sequentially tested during a calibration phase seeking for the minimum offset. A simplified schematic of a chopper stabilized amplifier that implements this approach is shown in Fig. 11.

During the calibration phase, the amplifier inputs are short-circuited and held at a reference level, V_{ref}, the choppers stop switching and the amplifier is configured as a continuous time three-stage amplifier with a closed loop gain of 60 dB.

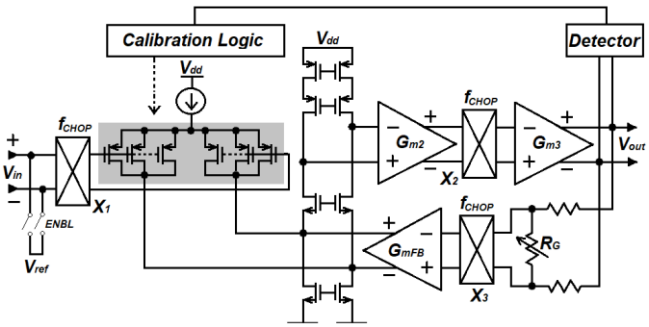

Fig. 11: Chopper stabilization with integrated differential-pair trimming

The block named Detector measures the output voltage and interacts with the Calibration Logic in order to find the best arrangement of the input transistors. It is worth noting that both the Detector and the Calibration Logic remain turned off during normal operation; i.e., they are active only during the calibration period. As a consequence, no static power is spent on zeroing the chopper-induced ripple. Measured values of offset voltage and input noise PSD with samples of an instrumentation amplifier built in accordance with the described technique were 3.5uV and 13.5nV/√Hz, respectively.

E. Digitally Assisted Auto-zero Stabilization

The auto-zero stabilization approach [40-42] was primarily devised aiming at reducing the input current of amplifiers in applications that require very high input impedance, like reading voltages from very high output impedance sources. Low offset voltage and low noise are targeted as well.

Despite the well-known low-offset feature of the chopper stabilized structure, it was avoided because the direct connection of the signal source with the chopper switches, which normally operate at high frequencies, implies an input current that may not be tolerated. The auto-zero is also a circuit with switches directly connected to the signal source, which, however, can operate at a lower switching rate, thus draining less current from the signal source.

The developed technique makes use of an auto-zero amplifier that is part of a feedback loop dedicated to nulling the offset of the main amplifier. In the block diagram of Fig.12, the mentioned auto-zero amplifier is G_{m1} and the main amplifier is G_{mMAIN}.

Considering that the offset voltage of both G_{m1} and G_{mMAIN} are in the same order of magnitude, the offset voltage of G_{m1} must be nulled before the offset correction

loop that comprises G_{m1}, G_{mINT} and G_{m3} enters into action.

The whole offset nulling process is done in two clock phases: During phase *CK1* the inputs of G_{m1} are short-circuited and the resulting output is integrated by G_{mINT}, which in its turn drives amplifier G_{m2} that closes a local negative feedback loop. In equilibrium, the voltage difference at the input of G_{m2}, V_{EF}, is the voltage that makes $V_{os1}=0$. During the subsequent phase, *CK2*, the amplifier G_{m1}, now with no offset voltage, reads V_{osMAIN}, the offset voltage of the main amplifier, and the same correction dynamics takes place. At the end of this phase, V_{GH}, the differential input voltage of G_{m3}, is the voltage that makes $V_{osMAIN}=0$.

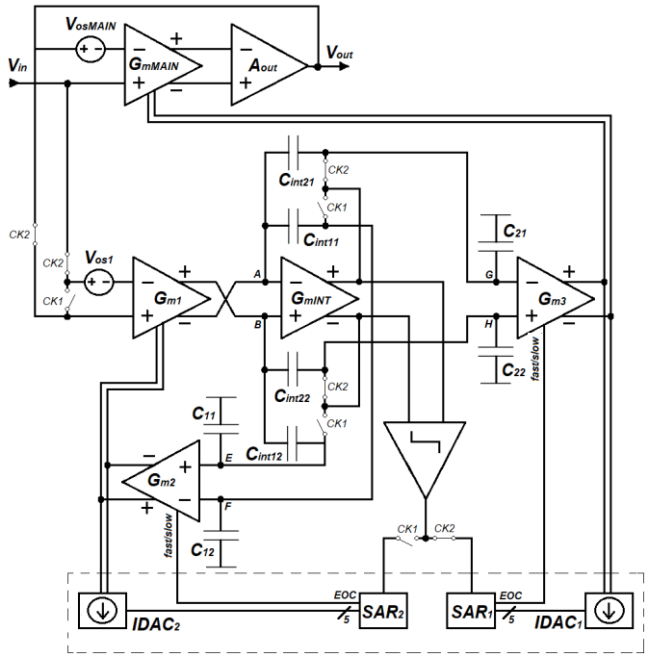

Fig. 12: Auto-zero stabilized amplifier

The use of an auto-zero-based system that operates at a slower pace favors the reduction of the input current; however, at the cost of an increased thermal noise in the amplifier baseband. As mentioned at the end of section III, the input referred noise PSD increases with the increasing ratio of the equivalent noise bandwidth to the auto-zero frequency. Since an increased auto-zero frequency is not an option because it jeopardizes the low-input-current targeted feature, the noise bandwidth must be reduced in order to reduce noise. The frequency band of noise is limited by the frequency response of the active signal path, which in this case commutates between the closed loop that nulls V_{os1} and the closed loop that nulls V_{osMAIN}. Assuming that the transconductances of G_{mMain} and G_{m1} have the same value, the cutoff frequencies of the first and second loops are, respectively given by, $G_{m2}/2\pi C_2$, and $G_{m3}/2\pi C_1$, where $C_2=C_{int21}=C_{int22}$ and $C_1=C_{int11}=C_{int12}$. Clearly, from these results, either G_{m2} and G_{m3} must be reduced and/or C_1 and C_2 must be increased in order to accomplish lower noise at the baseband.

As larger capacitors imply in larger chip area, G_{m2} and G_{m3} should be reduced. The latter is obviously a more suitable approach, but requires G_{mMAIN} and G_{m1} to be increased because for a given integration capacitor, the resulting noise is proportional to the ratio G_{m3}/G_{mMAIN}.

A concerning consequence of using large values of G_{mMAIN} and G_{m1} concurrent with low values of G_{m2} and G_{m3} is the possible saturation of the integrator, since the offset appears at its output multiplied by the so-established large transconductance ratio.

To solve this issue in the proposed technique, an auxiliary circuit was included, which is comprised of a comparator at the output of the integrator, two successive-approximation registers, SAR_1 and SAR_2, and two current *DACs*. The purpose of the added circuitry is to sense the integrator output and perform an initial zeroing of the offsets of both G_{mMAIN} and G_{m1} by means of two other control loops. With the offsets of G_{mMAIN} and G_{m1} already nulled in this initial phase, successive commutation of the two (inner) loops will cancel the residual offset due to drifts and leftovers from the limited resolution of the current *DACs*.

Measured values of the offset voltage and voltage noise density in samples of an amplifier that implements this technique were 0.4uV and 31nV/√Hz, respectively. The amplifier further achieved an input current of 0.8pA.

V. CONCLUSIONS

In this paper, some of the most important techniques applied to reduce offset voltage and input noise PSD in CMOS amplifiers were reviewed with basis on a collection of selected design examples developed in the last decade, most of which became the momentary state-of-the art.

The assessed material showed that the most efficient techniques developed within this time period are combinations of auto-zero and chopper stabilization, which are fundamental mechanisms for this purpose. However, while these mechanisms aim at reducing amplifiers input errors, they give rise to diverse side effects, such as increased chip area, increased power consumption, and output ripple, to name a few.

The ever-increasing diversity of applications added to market requirements like higher resolution, lower energy consumption, lower operating voltage and larger bandwidth have posed design challenges to accomplish successively better values for other properties of amplifiers in addition to offset voltage and input noise. In the current precision analog design arena, the effort is not devoted to minimizing only offset and input noise, but rather a larger group of properties altogether.

The challenge that designers currently have to face resides in the proper exploitation of the favorable aspects of both auto-zero and chopper stabilization and the ability to reduce their influences upon the other targeted properties.

The most recently developed techniques applied to reduce amplifier input errors clearly show an increase in the digital portion of the circuits, thus reinforcing that digitally-assisted analog is an effective strategy for accomplishing ever better results.

ACKNOWLEDGEMENTS

Thanks are due to M. Pessatti, R. Rotava and W. Prodanov from Chipus Microelectronics for tantalizing discussions about precision amplifiers.

REFERENCES

[1] G. Bulger, "Stability Analysis of Laser Trimmed Thin Film Resistors," *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. 11, no. 3, pp. 172-177, September 1975.

[2] Pease, B., "What's all this common-centroid stuff, anyhow?" Electronic Design, S. 91-94, October 1, 1996.

[3] G. Erdi, "Amplifier techniques for combining low noise, precision, and high-speed performance," IEEE Journal of Solid-State Circuits, vol. 16, no. 6, pp. 653-661, Dec. 1981.

[4] Analog Devices Inc., "LT1028 data sheet", <http://www.analog.com/media/en/technical-documentation/data-sheets/LT1028fd.pdf>.

[5] R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters," IEEE Journal of Solid-State Circuits, vol. 11, no. 6, pp. 795-800, Dec. 1976.

[6] T. N. Lin, B. Wang and A. Bermak, "Review and Analysis of Instrumentation Amplifier for IoT Applications," 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS, pp. 258-261), 2018.

[7] B. J. van den Dool and J. H. Huijsing, "Indirect Current Feedback Instrumentation Amplifier with a Common Mode Input Range That Includes the Negative Rail," ESSCIRC '92: Eighteenth European Solid-State Circuits conference, pp. 175-178, 1992.

[8] J. Szynowski: "CMRR Analysis of Instrumentation Amplifiers, Electron. Lett., 19, pp.547-549, 1983.

[9] Q. Fan and K. Makinwa, "Capacitively-coupled Chopper Instrumentation Amplifiers: An Overview," 2018 IEEE SENSORS, 2018, pp. 1-4.

[10] R. R. Harrison, "A low-power, low-noise CMOS amplifier for neural recording applications," 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353), 2002, pp. V-197 – V-200.

[11] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley and A. Kelly, "A 2uW 100nV/√Hz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials," in IEEE Journal of Solid-State Circuits, vol. 42, no. 12, pp. 2934-2945, Dec. 2007.

[12] J. Zheng, W. Ki, L. Hu and C. Tsui, "Chopper Capacitively Coupled Instrumentation Amplifier Capable of Handling Large Electrode Offset for Biopotential Recordings," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 12, pp. 1392-1396, Dec. 2017.

[13] H. Bhamra, J. Lynch, M. Ward and P. Irazoqui, "A Noise-Power-Area Optimized Biosensing Front End for Wireless Body Sensor Nodes and Medical Implantable Devices," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2917-2928, Oct. 2017.

[14] S. Pokamisas, D. Baxevanakis and P. P. Sotiriadis, "A 0.6V, 700nW Chopper Capacitively-Coupled Instrumentation Amplifier for Biomedical Applications," 2019 8th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2019, pp.1-4.

[15] X. T. Pham, N. T. Nguyen, V. -N. Nguyen and J. -W. Lee, "Area and Power-Efficient Capacitively-Coupled Chopper Instrumentation Amplifiers in 28 nm CMOS for Multi-Channel Biosensing Applications," in IEEE Access, vol. 9, pp. 86773-86785, 2021.

[16] Q. Fan, F. Sebastiano, H. Huijsing and K. Makinwa, "A 1.8μW 1μV-offset capacitively-coupled chopper instrumentation amplifier in 65nm CMOS," 2010 Proceedings of ESSCIRC, 2010, pp. 170-173.

[17] L. Xu, B. Gönen, Q. Fan, J. H. Huijsing and K. A. A. Makinwa, "A 110dB SNR ADC with ±30V input common-mode range and 8μV Offset for current sensing applications," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, 2015, pp. 1-3.

[18] A. T. K. Tang, "A 3 uV offset operational amplifier with 20 nV/√Hz input noise PSD at DC employing both chopping and autozeroing," 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, pp. 386-387 vol.1.

[19] T. Yoshida, Y. Masui, T. Mashimo, M. Sasaki, and A. Iwata, "A 1 V supply 50 nV/√Hz noise PSD CMOS amplifier using noise reduction technique of autozeroing and chopper stabilization," IEICE Trans. Electron., vol. E89-C, no.6, pp.769–774, June 2006.

[20] Y. Masui, T. Yoshida, M. Sasaki, and A. Iwata, "A 0.6 V supply CMOS amplifier using noise reduction technique of autozeroing and chopper stabilization," Ext. Abst. of 2006 Int. Conf. on Solid State Devices and Materials (SSDM), pp.374–375, Sept. 2006.

[21] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," Proc. IEEE, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[22] I. Bloom and Y. Nemirovsky, "1/f noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation," Appl. Phys. Lett., vol. 58, no. 15, pp. 1664–1666, Apr. 15, 1991.

[23] A. J. Williams, Jr., R. E. Tarpley and W. R. Clark, "D-C Amplifier Stabilized for Zero and Gain," in Transactions of the American Institute of Electrical Engineers, vol. 67, no. 1, pp. 47-57, Jan. 1948.

[24] E. A. Goldberg, "Stabilization of Wideband Direct-Current Amplifiers for Zero and Gain", RCA Review, pp. 296-300, June, 1950.

[25] A. J. Williams, Jr. "Recorder and Control Circuits", US Patent 2,113,164, April 5, 1938.

[26] G. Wegmann, E. A. Vittoz and F. Rahali, "Charge injection in analog MOS switches," in IEEE Journal of Solid-State Circuits, vol. 22, no. 6, pp. 1091-1097, Dec. 1987.

[27] R. Burt and J. Zhang, "A Micropower Chopper-Stabilized Operational Amplifier using a SC Notch Filter with Synchronous Integration inside the Continuous Time Signal Path," 2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers, 2006, pp. 1388-1397.

[28] R. G. H. Eschauzier, L. P. T. Kerklaan and J. H. Huijsing, "A 100 MHz 100 dB operational amplifier with multipath nested Miller compensation structure," 1992 IEEE International Solid-State Circuits Conference Digest of Technical Papers, 1992, pp. 196-197.

[29] J. H. Huijsing, "Multi-stage amplifier with capacitive nesting for frequency compensation", US Patent 4,559,502, December 17, 1985.

[30] G. F. Luff, "Chopper Stabilized Amplifier", US Patent 7,724,080 B2, May 25, 2010.

[31] Y. Kusuda, "Auto Correction Feedback for ripple suppression in a chopper amplifier," 2009 IEEE Custom Integrated Circuits Conference, 2009, pp. 573-576.

[32] Y. Kusuda, "Auto Correction Feedback for Ripple Suppression in a Chopper Amplifier," in IEEE Journal of Solid-State Circuits, vol. 45, no. 8, pp. 1436-1445, Aug. 2010.

[33] V. Ivanov and M. Shaik, "5.1 A 10MHz-bandwidth 4μs-large-signal-settling 6.5nV/√Hz-noise 2μV-offset chopper operational amplifier," 2016 IEEE International Solid-State Circuits Conference (ISSCC), 2016, pp. 88-89.

[34] C. G. Yu and R. L. Geiger, "Precision offset compensated op-amp with ping-pong control," GOMAC-92 Dig., pp. 189-190, 1992.

[35] M. A. P. Pertijs and W. J. Kindt, "A 140 dB-CMRR Current-Feedback Instrumentation Amplifier Employing Ping-Pong Auto-Zeroing and Chopping," in IEEE Journal of Solid-State Circuits, vol. 45, no. 10, pp. 2044-2056, Oct. 2010.

[36] J. F. Witte, J. H. Huijsing and K. A. A. Makinwa, "A chopper and auto-zero offset-stabilized CMOS instrumentation amplifier," 2009 Symposium on VLSI Circuits, pp. 210-211, August 2009.

[37] M. Belloni, E. Bonizzoni, F. Maloberti and A. Fornasari, "Low-power ripple-free chopper amplifier with correlated double sampling de-chopping," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, 2010, pp. 765-768.

[38] M. Belloni, E. Bonizzoni, A. Fornasari and F. Maloberti, "A Micropower Chopper—CDS Operational Amplifier," in IEEE Journal of Solid-State Circuits, vol. 45, no. 12, pp. 2521-2529, Dec. 2010.

[39] I. Akita and M. Ishida, "A 0.06mm2 14nV/√Hz chopper instrumentation amplifier with automatic differential-pair matching," 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2013, pp. 178-179.

[40] T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "A Quiet Digitally Assisted Auto-Zero-Stabilized Voltage Buffer with 0.6pA Input Current and 0.6μV Offset," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), 2018, pp. 50-52.

[41] T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "An Auto-Zero Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Input Current," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), 2019, pp. 298-299.

[42] T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "An Auto-Zero-Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Sub-pA Input Current," in IEEE Journal of Solid-State Circuits, 2021.