Are CMOS Operational Transconductance Amplifiers Old Fashioned? A Systematic Review

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***Abstract*— Operational Transconductance Amplifiers (OTAs) are essential building blocks in analog circuits. Since the early years of integrated circuit science, OTAs have been used in industry and researched in academia. Over the years, a number of techniques and approaches to OTA design have been observed in the literature. With this systematic review, we aim to provide an overview of top journal papers published from 2017 to 2021 containing OTA design. In our investigation we initially found 128 manuscripts and 24 primary studies of OTA design. A set of 10 different techniques have been found. Furthermore, we also evaluated used technology, inversion level and characterization process. With this study we contribute to highlight recent OTA design innovations.**

***Index Terms*— CMOS; Operational Transconductance Amplifiers; OTA; Systematic Review.**

I. Introduction

Integrated circuits (IC) are miniaturized circuits capable of boosting new research and advances in a myriad of applications such as medical, aerospace and education. Moreover, since the MOS transistor patent in the 1920s by Lilienfeld [1], we have seen an astonishing evolution in circuit design, process and automation to fabricate ICs. Passing through William Shockley, Jack Kilby, John Atalla and Dawon Kahng and other remarkable researchers [2], today the IC industry commercially produces the Apple M1, an ARM-based 5-nm process chip with 16 billion transistors in a single chip [3].

In spite of these huge advances in IC, some basic building blocks are still needed. Most analog projects require voltage regulators, reference sources, analog filters, analog-to-digital converters, etc. Among this basic circuits, the operational transcondutance amplifier (OTA) has a wide range of analog applications.

One of the basic building block of an OTA is the differential pair. It was invented to be used with vacuum tubes in the decade of the 1930s [4]. Originally, the differential pair was built with the cathodes connected together but in more recent technologies we frequently see these structures using either bipolar or MOS transistors sharing their emitters or sources, respectively.

A common OTA symbol can be seen in Fig. 1a. In this symbol, the OTA has a balanced/differential voltage input and a single current output. Note that the output current depends on the input voltage difference and it is proportional to the device's transconductance (G_m).

One of the first OTA schematic that was integrated, can be seen in Fig. 1b [5]. At the time this structure was named as differential voltage controlled current source (DVCCS) and

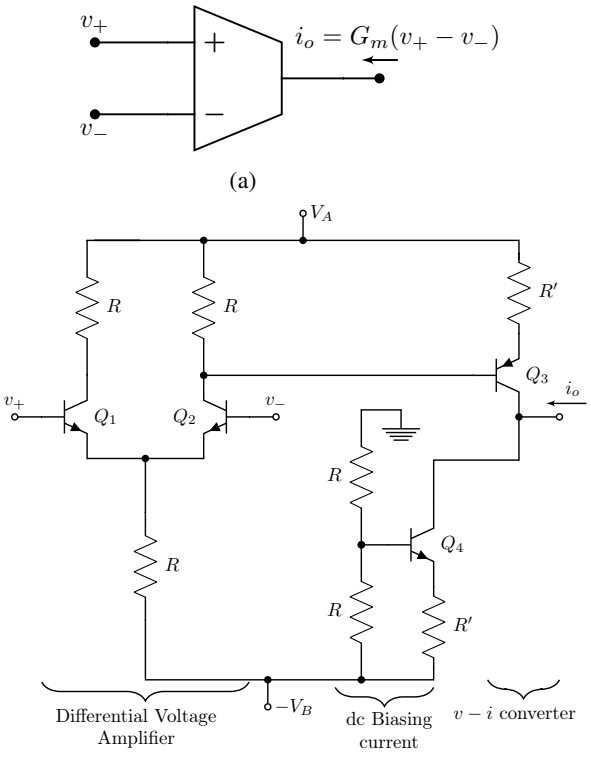

Fig. 1: An OTA symbol for balanced input/single output (a) and one of the first on-chip OTA that can be seen in [5] (b).

the amplifier was composed by two stages. The first stage contains a differential pair and is a differential voltage amplifier. Transistor Q_3 is responsible to convert the output voltage of the first stage into current and Q_4 is configured to set the DC current of Q_3. At the time the device's G_m was controlled by adjusting V_B biasing voltage. More recently, it is common to see the 'Miller OTA' as a standard CMOS amplifier [6]. It is a simple two-stage OTA that can be integrated with MOS transistors and has a frequency compensation by means of a capacitance. After its invention, we have seen OTAs being used in a wide range of applications. Classic works such as [7, 8] and [9] illustrate applications of OTAs in filters and voltage references, respectively.

Inside this context, our objective is to answer the following research question: "Are CMOS Operational Transconductance Amplifiers Old Fashioned?". Through a systematic literature review, we are going to investigate the works published in indexed journals in the last 5 years. We aim to identify the proposed innovations of OTAs design techniques and topologies, used technology, operation region and character-

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ization process. During this research we walk through 128 papers that cite OTAs.

After selecting only the top rated journals in the Scopus CiteScore Index and apply the inclusion and exclusion criteria, we came up with 24 papers. We evaluated these 24 papers in detail to understand the innovations proposed in each of them.

The rest of this work is structured as follows. Section II presents the methods used to conduct this systematic review. In Section III we perform the data tabulation, individual studies and results synthesis. Finally, Section IV presents the conclusion.

II. Methods

A systematic review process should be conducted under some protocol to ensure that it can be reproduced, and later appended, in a standardized way. In this work we use PRISMA [10], which is majorly divided into following these steps:

i. Information sources and search strategy;
ii. Eligibility criteria and selection process;
iii. Data collection process and data items;
iv. Results and Discussions.

A. Information sources and search strategy

We establish the criteria from [11] to select the journals. Thus, the CiteScore index, obtained from the Scopus Documents Search [12] is used to select works stratified from 100th to 80th top journals.

Therefore, we search within Article Title, Abstract and Keywords the terms: CMOS, transconductance and amplifier. This strategy can cover and found all related OTA publications. We also limit our results for English articles published only in high quality journals (CiteScore 100th to 80th) from years 2017 to 2021. The resultant search string is:

TITLE-ABS-KEY (CMOS AND TRANSCONDUCTANCE AND AMPLIFIER) AND LIMIT-TO (PUBYEAR , 2021, 2017) AND LIMIT-TO (SRCTYPE , "j")

B. Eligibility criteria and selection process

To ensure that only relevant OTA manuscript have been selected to conduct the review, we impose inclusion (InC) and exclusion (ExC) criteria:

- InC1. Paper that an innovation in the OTA topology was identified;
- InC2. Paper that an improvement in OTA performance was identified;
- ExC1. Work that a traditional OTA topology is used to demonstrate device improvement;
- ExC2. Work that an OTA is a building block of a system.

Each author of this paper worked independently and read the title and abstract of the selected papers. This first step allowed to identify the works that uses an OTA topology. Then each researcher evaluated the entire journal paper for its relevance and apply the InC and ExC criteria. The last step consisted in confirming if select works are relevant to this paper.

Table I.: Retrieved articles.

Initially Scanned	1st Filtered	2nd Filtered	Final Selection
603	128	36	24

C. Data collection process and data items

The data presented in this manuscript has been summarized in Table I. The search string introduced in Section A. applied in Scopus database returned 603 papers. After reading the abstract we found 128 manuscripts that have OTAs circuits involved. By using the CiteScore chosen range, 36 works have been fully read. Finally, we apply the InC and ExC defined in Section B. and 24 papers fulfilled the requirements to help to answer the main question of this study.

Table II shows the selected articles for the research question. By using Table II, we refine the study focusing to elucidate design techniques, methods and technology data.

III. Results and Discussions

As a first step in this section, we will summarize the main ideas and innovations in the OTAs found in the works listed in Table II. Next, we will group the works with common characteristics, namely: design technique (Table III), technology (Table IV), inversion level (Table V) and characterization process (Table VI). Finally, we will carry out an evaluation of our findings and answer the research question.

A. Design Techniques

During our research process we found ten different design techniques. Some articles use more than one technique to achieve a desired OTA performance. Table III summarizes the design techniques with the respective papers.

In [13] the authors present a novel two-stage OTA that improves the dynamic response of an adaptively biased low-dropout regulator (AB-LDO). The proposed novelty was achieved by combining the structures of a conventional current-mode OTA and a conventional differential-mode OTA. The proposed OTA is named as hybrid-mode OTA (HM-OTA) and its performance such as DC gain, bandwidth, slew rate and loop stability can be controlled by the aspect ratio of the transistors of the first stage of the OTA.

Modifications on a conventional class-AB OTA are presented in [19]. The authors increase the output impedance of the OTA by reducing the output stage and using a cascade topology. In addition to this, it is proposed the use of transistors in the first stage to generate a large drain-source voltage drop during the large-signal transient period to increase the OTA's slew rate (SR) performance. The proposed OTA is tested in a switched capacitor filter.

In [22] the authors propose a wideband differential two stage low-noise transconductance amplifier (LNTA). This LNTA is a transconductance amplifier, it does not use differential pairs and it is designed to be used in a receiver front-end operating from 0.1 to 3.1 GHz.

[23] designed a three-stage OTA with the aid of derived equations to estimate the dynamic response of the amplifier.

Topologies based on Current Recycling/Reuse also represent a large part of the works found. Based on the recycling folded cascode OTA (RFC OTA), [15] presents an improved

Table II.: Selected research articles.

Ref.	Authors	Title	Year	Percentile
[13]	Maity A., Patra A.	A hybrid-mode operational transconductance amplifier for an adaptively biased low dropout regulator	2017	96
[14]	Shen L., Lu N., Sun N.	A 1-V 0.25-μW Inverter Stacking Amplifier with 1.07 Noise Efficiency Factor	2018	92
[15]	Garde M.P., Lopez-Martin A., Carvajal R.G., Ramírez-Angulo J.	Super Class-AB Recycling Folded Cascode OTA	2018	92
[16]	Luo D., Zhang M., Wang Z.	A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition	2019	92
[17]	Yosefi G.	A special technique for Recycling Folded Cascode OTA to improve DC gain, bandwidth, CMRR and PSRR in 90 nm CMOS process	2020	92
[18]	Lee S.-Y., Wang C.-P., Chu Y.-S.	Low-Voltage OTA-C Filter with an Area- and Power-Efficient OTA for Biosignal Sensor Applications	2019	89
[19]	Kim J., Song S., Roh J.	A High Slew-Rate Enhancement Class-AB Operational Transconductance Amplifier (OTA) for Switched-Capacitor (SC) Applications	2020	87
[20]	Khateb F., Kulej T., Akbari M., Kumngern M.	0.5-V High Linear and Wide Tunable OTA for Biomedical Applications	2021	87
[21]	Grasso A.D., Pennisi S., Scotti G., Trifiletti A.	0.9-V Class-AB Miller OTA in 0.35-μm CMOS with Threshold-Lowered Non-Tailed Differential Pair	2017	84
[22]	Guo B., Gong J., Wang Y.	A Wideband Differential Linear Low-Noise Transconductance Amplifier with Active-Combiner Feedback in Complementary MGTR Configurations	2021	84
[23]	Giustolisi G., Palumbo G.	Design of Three-Stage OTA Based on Settling-Time Requirements including Large and Small Signal Behavior	2021	84
[24]	Toledo P., Crovetti P., Aiello O., Alioto M.	Design of digital OTA's with operation down to 0.3 V and NW power for direct harvesting	2021	84
[25]	Beloso-Legarra J., de la Cruz-Blas C.A., Lopez-Martin A.J., Ramirez-Angulo J.	Gain-boosted super class AB OTA's based on nested local feedback	2021	84
[26]	Zhang Q., Zhao X., Zhang X., Zhang Q.	Multipath recycling method for transconductance enhancement of folded cascade amplifier	2017	83
[27]	Shirazi M., Hassanzadeh A.	Design of a low voltage low power self-biased OTA using independent gate FinFET and PTM models	2017	83
[28]	Veldandi H., Shaik R.A.	Low-voltage PVT-insensitive bulk-driven OTA with enhanced DC gain in 65-nm CMOS process	2018	83
[29]	Dubey T., Bhadauria V.	A low-voltage highly linear OTA using bulk-driven floating gate MOSFETs	2019	83
[30]	Başak M.E.	Realization of DTMOS based CFTA and multiple input single output biquadratic filter application	2019	83
[31]	Khade A.S., Vyas V., Sutaone M.	A technique to enhance the transconductance of micro-power improved recycling folded cascode operational transconductance amplifier with reasonable phase margin	2019	83
[32]	Banagozar S., Yargholi M.	Ultra-low power two-stage class-AB recycling double folded cascode OTA	2019	83
[33]	Kumngern M., Kulej T., Khateb F., Stopjakova V., Ranjan R.K.	Nanopower multiple-input DTMOS OTA and its applications to high-order filters for biomedical systems	2021	83
[34]	Wang Y., Zhang Q., Zhao X., Dong L.	An enhanced bulk-driven OTA with high transconductance against CMOS scaling	2021	83
[35]	Zhao G., Ye M., Hu K., Zhao Y.	A ROIC for diode uncooled IRFPA with hybrid non-uniformity compensation technique	2018	81
[36]	Jakusz J., Jendernalik W., Blakiewicz G., Kłosowski M., Szczepański S.	A 1-nS 1-V sub-1-µW linear CMOS OTA with rail-to-rail input for Hz-band sensory interfaces	2020	80

RFC OTA able to increase its current efficiency, dynamic and small-signal performances. The authors achieve this performance boost by replacing the RFC OTA's fixed tail current by an adaptive current biasing circuit.

Table III.: Identified design techniques.

Design techniques	Ref.
Multistage	[13, 19, 23, 26, 14, 19, 22, 27, 28, 29, 32, 36]
Current Recycling/Reuse	[15, 26, 14, 17, 31, 32]
Bulk-driven	[20, 28, 29, 33, 34, 36]
Dynamic Threshold Voltage MOSFET (DTMOS)	[30, 33, 34]
Very Low Transconductance (VLT)	[16, 18, 20, 36]
Multiple-input MOS Transistors	[20, 27]
Non-tailed Current	[21, 29]
Flipped Voltage Follower (FVF)	[25, 29]
Double Gate FinFet	[27]
CMOS Standard Cells	[24]

Manuscript [26] revised the improved recycling folded cascode amplifier (IRFC). The modified circuit uses a second input pair to create three paths to conduct the small signal current into a different path of the DC current. As result, this improves the transconductance of the original IRFC and creates the multipath recycling folded cascode (MRFC). The MRFC increases the transconductance, almost at no expense of power dissipation.

In [14] is proposed a new two-stage OTA structure based on stacking inverters. Due to the stacking inverters and hence current reuse, the amplifiers present a better noise efficiency factor (NEF) compared to other OTAs.

In [17] the author proposes modifications of a RFC OTA proposed in [37] to fix the common mode output voltage in the middle ranges of V_{DD}. The main modification consists of adding a common mode feedback circuit to change the OTA's transistors biasing.

The work in [31] is also based on FC/RFC and its variations. A subthreshold fixed-g_m low-voltage low-power IRFC OTA is designed with an asymmetrical current split input stage. The unbalanced inner differential pair conducts different DC current for the same input voltage. The author calls this structure as a modified improved recycling folded cascode (MIRFC) since this topology enhances the transconductance, DC gain, GBW and phase margin when compared to its IRFC counterpart.

Paper [32] presents an ultra-low power multiple stage OTA also based on RFC topology. The first stage is a recycling double folded cascode (RDFC) and the second stage is a class AB. Since the topology use two transconductance elements it improves the linearity and enhances the open loop gain at cost of the following additional blocks: current control circuit and RC Miller compensation. The performance of the circuit shows a better output signal swing when compared against the other FC/RFC based topologies.

Paper [28] presents a high DC gain bulk-driven OTA for low voltage applications. A cross-coupled active load is employed at the bulk-driven input stage to enhance the gain of the OTA and a cross-forward (CF) gain stage was placed between the input and output stages of the OTA. This stage helps to enhance the output stage transconductance and also allows large capacitive loads (up to 50 pF) keeping the OTA stable. The bulk terminals of some of the MOSFETs are biased at common-mode voltage to reduce their threshold voltage (V_{TH}) that makes easier to operate at low voltages.

The work from [30] used a Current Follower Transconductance Amplifier (CFTA) and a transistor with tied body and gate called Dynamic Threshold Voltage MOSFET (DTMOS). The use of DTMOS guarantees a higher transconductance than a normal MOS transistor even in weak inversion operation. The manuscript [33] also uses the DTMOS technique with multiple input bulk driven (MIBD) MOS to build the multiple input dynamic threshold (MIDT) MOS. The OTA designed with MIDT has enhanced linear range (as compared to DTMOS) and transconductance (as compared to MIBD). The proposed OTA has 4 inputs and takes advantages from DTMOS decreasing the threshold voltage property and it has a better linearity by using the MIDT solution.

The paper in [34] proposes a subthreshold bulk driven OTA where the input (bulk) is connected to the gate of the transistor through a robust transconductance enhancement (RTE) control block. Although [34] does not make this relationship, this connection characterizes a DTMOS. This arrangement allows the input voltage V_{in} to be applied through the feedforward as kV_{in} to the gate terminal. This strategy improves the transconductance of bulk-driven OTAs working in weak inversion and benefits from CMOS scaling as the g_{mb}/g_m decreases, the transconductance increases.

The works [16, 18, 20, 36] propose an interesting design choice: Very Low Transconductance (VLT). They use VTL to obtain OTAs with transconductance at pS or nS, ideal for biomedical applications.

In [16] the authors show an application of neural signal amplifier where a very low transconductance is required (order of 65 pS). The presented VLT OTA uses a current mirror with a series-parallel current division to decrease transconductance and the authors propose the use of a complementary input stage with source degeneration to increase the linearity of the amplifier.

A similar idea is found in [18], it proposes a VLT OTA for biosignal sensor applications. The OTA has a local-feedback linearized technique and a transconductance booster. The proposed OTA combines current division with source degeneration to enhance linearity and implement low transconductance.

In [36] is presented a two-stage, bulk-driven and VLT OTA for biomedical applications. The deviation of the first stage current (the one that is converted from the input voltage variation) is based on the channel length modulation of the input MOS transistors.

Multiple-input MOS transistors are used by [20]. This paper presents a low-voltage and a low-power OTA operating in subthreshold region and using the bulk-driven multiple-input MOS transistors as differential pairs. The differential stage includes source degeneration transistors. The circuit shown is aimed for biomedical applications and these modifications improve the linearity. To increase the DC gain, the authors

also use self-cascode transistors and positive feedback.

The work in [25] describes an approach to the super class AB OTAs using an adaptive biasing and Local CMFB (LCMFB) by two nested local feedback loops (positive and negative) at the active load. Two cross-coupled floating batteries implemented by Flipped Voltage Follower (FVF) are used to build the adaptive-tail-current-biasing block, while a network combining resistors (negative feedback) and transistors (positive feedback) implements the LCMFB. As a result, both settling time and settling accuracy are improved under high power efficiency provided by subthreshold operation.

A Flipped Voltage Follower is also found in [29]. This work proposes an OTA using three different techniques: bulk-driven, floating gate-transistors and FVF. This combination creates the BDFG-FVF OTA, by removing the conventional biasing tail current the voltage follower makes the circuit self biased. Bulk-driven and floating-gate transistors are used together: first gate is used for a bias input voltage and the second gate is directly connected to the bulk where the input signal is applied. The proposed BDFG-FVF OTA achieves better FoMs than the conventional FG-OTA. Like [29], the authors from [21] also propose a non-tailed with threshold-lowered differential pair OTA. The proposed circuit is designed to increase the common-mode input range of the OTA.

In [27] we find a combination of multistage and multiple input transistors. The first stage of the proposed subthreshold OTA is a pseudo differential, the second stage is a common source amplifier using an active load and the third one has a high resistance to increase the amplifier gain. A double gate IGFinFET is used to obtain multiple input transistors. Since double gate transistors are independent, the full circuit demands some biasing voltage for each transistor gate. The paper implements a Damping Factor Control as a compensation method used to adjust the frequency behavior. The double gate transistors allow the advantage of bulk-driven technique for low-voltage analog designs without bulk-driven limitations since the IGFinFET threshold voltage of the front gate in linearly dependent on back gate voltage twin well or triple well technology is needed.

Manuscript [24] proposes a subthreshold digital OTA (DIGOTA) designed with digital CMOS standard cells. By using fully digital circuits the result block behaves like an OTA.

The authors of [35] propose an OTA with DC offset calibration designed to reduce its input offset voltage and it is used in a CMOS readout IC for diode uncooled infrared focal plane array.

B. Fabrication technology

Table IV presents the fabrication technology used in each paper. Fabrication technologies used before the 2000s are still very popular in OTA design. The 180 nm process represents 66% of the researched works and the 500 nm and 350 nm processes are still found in 13% of the manuscripts. Thus together they correspond to 79% of the researched works. The 90 and 65 nm processes are each seen with one and two manuscripts, respectively and they represent 12.5% of the total researched papers.

Table IV.: Identified fabrication technology.

Technology	**Ref.**
500 nm	[15]
350 nm	[21, 35]
180 nm	[13, 14, 16, 18, 19, 22, 20, 24, 25, 26, 29, 31, 32, 33, 34, 36]
90 nm	[17]
65 nm	[23, 28]
45 nm	[30]
20 nm	[27]

The manuscripts containing MOS transistors with the narrowest channels have 45 and 20 nm of channel length. We mention that these works use the Predictive Technology Model (PTM) [38] that allows only schematic simulation, since it is not provided by a foundry.

C. Inversion level

The effort to reduce power consumption and decrease the supply voltage has motivated the design of OTAs since the early 2000s. This trend still persists today and is reflected in the researched papers. The weak inversion/subthreshold designs corresponds to 54% (13) of the researched works.

However, designs operating at strong inversion are still representative in applications that demand high transconductance values. They represent 46% of the total researched works.

Table V presents the inversion levels of each work.

Table V.: Identified inversion levels.

Region	**Ref.**
Weak inversion/ Subthreshold	[16, 17, 18, 20, 23, 24, 27, 28, 30, 31, 32, 33, 34]
Strong inversion	[13, 14, 15, 19, 21, 22, 25, 26, 29, 35, 36]

D. Characterization process

Finally, we grouped the works by the characterization process: measurements or simulation. Table VI shows a summary of this grouping. Only 54% of the researched papers were manufactured and measured. The remaining OTAs, 46%, were characterized only through computer simulation.

Table VI.: Identified characterization process.

Characterization	**Ref.**
Measurement	[13, 14, 15, 16, 18, 19, 22, 21, 24, 25, 34, 35, 36]
Simulation	[17, 20, 23, 26, 28, 27, 29, 30, 31, 32, 33]

E. Evaluation and challenges

Analyzing the papers we noted that current recycling/reuse OTAs represent a large amount of papers. In

the scenario where low power consumption is relevant, these kind of techniques are of interest. In low voltage applications, where the power supply is lower than 1 V (but close to 1 V, e.g. 0.9 V), we may expect that current reuse with stacking transistors is not an option. However, works such as [14] proves otherwise.

When the supply voltage is decreased further away from 1 V, we noticed that multiple stages and not stacked OTAs are used. Also input stages using bulk-driven transistors are getting common. The authors use these techniques in order to mainly maintain the OTA's gain when the power supply is decreased.

In spite of many integrated digital circuits being fabricated with transistors with channel lengths narrower than 10 nm, such as the Apple M1, in the design and research of OTAs it is possible to note that the planar MOS technology is still dominant. Only one manuscript was using FinFets. We also note that clever analog designs can still be seen with 500-nm channel length transistors [15].

Considering the quality of the journals and the review process that these articles underwent, the authors of the present study believed that most OTAs should be manufactured and measured. However, this did not happen. A relevant percentage of works were simulated, only a few at post layout level. This may indicate that accessing the foundry process has been difficult. However, the authors of the present study believe that a deeper investigation should be carried out to prove this claim.

IV. Conclusion

In IC design, some initial conditions guides its building process. Considering the OTAs, the techniques/topologies, fabrication technology and regions of operation guides the design rules. Hence, efficient OTAs have to address many conditions to achieve the characteristics for which they were designed. Therefore, we conduct a systematic literature review trough 128 papers and apply inclusion and exclusion criteria. A critical review was done on 24 papers.

After analyzing the obtained data, it was possible to address the research question: "Are CMOS Operational Transconductance Amplifiers Old Fashioned?". The answer is: NO! There are still researches that present innovations in the design of OTAs. The OTAs that use current recycling/reuse almost represents a family among the 10 different design techniques identified. And multi-stage also have relevant share in the papers researched. Planar CMOS technologies are still very popular among researchers. However, there is room for OTA projects addressing the challenges of non-planar technologies.

As future work, this systematic review can expand the number of papers evaluated. This would allow a deeper investigation of other questions that can not be answered with the collected samples, such as "how has the industry handled the OTA design?". Furthermore, this work may inspire the choice of an OTA topology by IC designers.

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