Properties and Design of CMOS Thyristor Delay Elements

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***Abstract*— The CMOS thyristor delay element and its basic operation are presented in this paper. Six variations of the thyristor design developed over the years to extend the delay length, to improve the consistency of the delay, or to control the sensitivities of the delay are also discussed. This includes the complementary thyristor, the thyristor without the current source, the thyristor with threshold elevation, the thyristor with opposing current source, the single-ended thyristor, and the thyristor-type feedback delay element. Design considerations common to all CMOS thyristors are also discussed to provide insights on topology selection, capacitive loading, and transistor sizing.**

***Index Terms*— CMOS Thyristors; Delay Elements; Sensitivity.**

I. Introduction

The CMOS thyristor is a current-controlled delay element first proposed as a low-voltage, low-power delay element with a wide delay range and lower voltage and temperature sensitivity compared to other RC-based or CMOS inverter-based delay elements [1]. Although the original design already had a wide range of possible delay lengths, improvements made on the CMOS thyristor design over the years focused on the controllability and tunability of its delay [2][3]. Current CMOS thyristors have extremely high sensitivity to temperature and are even more sensitive than current starved CMOS inverters [4].

With the amount of flexibility in its delay length and temperature sensitivity, new designs of CMOS thyristors have emerged for various applications. There are CMOS thyristors specifically designed for temperature sensors[5][6][7], long delay elements for burst pulses[2], and continuous-time digital signal processors (CTDSP) [8]. Aside from these, CMOS thyristors are still commonly used as delay elements in delay-locked loops, phase-locked loops, and oscillators [2].

To delve deeper into the properties and design of CMOS thyristor delay elements, this paper is organized as follows: section II discusses its operation by looking at a simple thyristor circuit, section III presents six classifications of CMOS thyristor designs found in literature that vary its operation, section IV highlights some design considerations applicable to all CMOS thyristors, and section V provides our conclusions into the use of CMOS thyristors as delay elements.

II. Basic CMOS Thyristor Operation

The basic operation of the CMOS thyristor can be exhibited by the idealized circuit shown in figure 1. In its inactive state, the current source is not connected and the switches S_1 and S_2 are closed, strongly pulling Q to ground and $\overline{Q}$ to the supply, thereby turning off the two transistors. To start the delay, the switches are opened. As Q and $\overline{Q}$ are now undriven with the two transistors continuing to be OFF, the voltages stored in these two nodes through the gate capacitances of the transistors are retained. In this configuration, nothing will happen and the delay is essentially infinite. To start the delay, the current source I_{ctrl} must also be connected. $\overline{Q}$ is then drained at the rate dictated by the current source. Once $\overline{Q}$ drops to the threshold voltage of M_2, the thyristor's positive feedback mechanism is activated. M_2 turns ON, pulling Q up and subsequently turning ON M_1. $\overline{Q}$ is then pulled down stronger with the additional current through M_1 turning ON M_2 more. The delay ends when the voltage of $\overline{Q}$ is at ground and Q is at supply. To use the delay element again, the positive feedback is broken by turning OFF the transistors by closing the two switches.

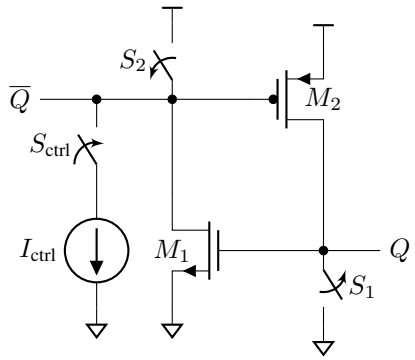

Fig. 1 A basic CMOS thyristor with an ideal current source [1]

The delay of this element then is the sum of two phases: the current source phase and the positive feedback phase. In the current source phase, the delay is simply how long it takes for the current source I_{ctrl} to drain the capacitance $C_{g,2}$ at the gate of M_2 to the threshold voltage $V_{th,p}$ of M_2. Equation 1 shows the relationship.

$$t_{\text{d,lin}} = \frac{C_{g,2} V_{th,p}}{I_{\text{ctrl}}} \tag{1}$$

This is the phase that makes the CMOS thyristor insensitive to the supply voltage and to temperature. The delay is only dependent on the threshold voltage, the gate capacitance, and the current source.

Assuming that the current source is kept connected after M_2 turns ON, the positive feedback phase has a delay length as shown in equation 2. This is the result after solving how long it takes M_1 to reach saturation after M_2 reaches saturation using the square-law model [9]. In this equation, $C_{g,1}$ is

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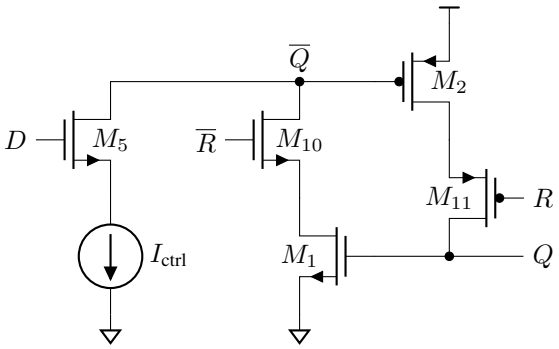
the capacitance at the gate of M_1, $V_{th,n}$ is the threshold voltage of M_1, and k_p is the process transconductance parameter of M_2.

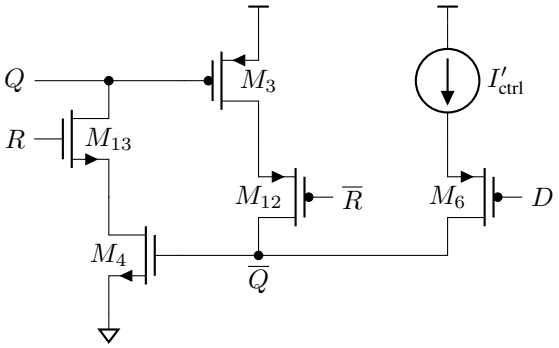
$$t_{\text{d,sat}} = \sqrt[3]{\frac{6C_{g,2}^2 C_{g,1}}{k_p I_{\text{ctrl}}^2} V_{th,n}} \tag{2}$$

As the transistors are OFF and the nodes are undriven during the current source phase, the only instances that the thyristor consumes power are during the resetting and during the positive feedback phase. Again, with the current source phase dominating the total delay, this property is what leads to the CMOS thyristor's low power consumption. Unlike the CMOS inverter where the delay is dependent on how long transistors in saturation would charge the load, the CMOS thyristor's delay is based on how long it takes current sources to discharge the pre-charged capacitance at the transistors' gates. Instead of dynamic power supporting the delay, it is static power supporting it. The lower the static power, the longer is the delay acquired.

Another advantage of CMOS thyristors to CMOS inverters is that the delays can be longer. For applications requiring long delays, fewer CMOS thyristor stages are needed compared with CMOS inverter stages. The footprint of the CMOS thyristor implementation is then generally smaller and has fewer switching events than the CMOS inverter-based implementation.



(a) The half delaying the rising of Q



(b) The half delaying the falling of Q

Fig. 2: The two halves of the original CMOS thyristor proposal [1]. Labeled nodes of the same name are connected together.

III. Review of CMOS Thyristor Circuits

This section presents the properties and designs of CMOS thyristors found in literature. We have classified them into six designs: (1) *complementary transistors*, which implements the thyristor discussed in section II using double the number of transistors to improve the fall time of the output; (2) *thyristor without current sources*, which is designed to make the effects of the current source smaller to the point that it allows no current; (3) *thyristor with threshold elevation*, which deals with increasing the threshold voltage of the thyristor to lengthen the linear part of the delay; (4) *thyristor with operating current source*, which minimizes the weak positive feedback present at the very start of the delay; (5) *single-ended thyristor*, which combines CMOS inverters and CMOS thyristors in delay chains to make the inherently complementary thyristor into a single-ended delay element; and (6) *thyristor-type feedback delay element*, which provides a different perspective in thyristor operation, where adding a positive feedback path to current-starved CMOS inverters can have a similar behavior to that of CMOS thyristors.

A. Complementary Thyristors

The original proposal [1] for the CMOS thyristor delay element is two thyristors connected together, as shown in figure 2. Since the basic thyristor discussed earlier can delay the rising of Q but not of its falling (as the reset is fairly instantaneous), two thyristors, one of which is inverted, are used to delay both edges. The thyristors being inverses of each other removes the need for the switches that pull the nodes to the rails; the end of one thyristor's delay pulls the other to reset. This reset, however, does not break the positive feedback like with the basic thyristor, hindering the delay phase of the other thyristor. Transistors $M_{10\text{-}13}$ are then added to break the feedback by splitting the loop.

The addition of another thyristor does change the equation for the delay a bit. But not in form, only in the values involved. The total capacitance in the nodes are higher as there are now two gates to charge for each operation. It is now the gates of M_2 and M_4 together that are charged or discharged by the current source. On the other side, both gates of M_1 and M_3 are charged or discharged together, but the end of the delay is still dependent on the one transistor in the enabled thyristor reaching saturation. The load is heavier, but the threshold voltages are still the same.

B. Thyristor without Current Sources

The CMOS thyristor made with ideal components has infinite delay when the current source is removed. With real transistors, however, the subthreshold currents of the transistors would slowly discharge the gate capacitors and eventually trigger the positive feedback. The circuit shown in figure 3 uses this effect.

In terms of supply voltage sensitivity, this version of the CMOS thyristor is more sensitive than the complementary thyristor while still less sensitive than CMOS inverters and current-starved CMOS inverters [4]. Raising or lowering the supply does not change the condition to end the delay, in which either M_1 or M_2 reaches saturation or their respective threshold voltage. It does, however, change the currents observed with the change in drain-to-source voltages experienced.

As for its temperature sensitivity, the CMOS thyristor has significantly higher sensitivity than current-starved inverters [4]. A temperature sensor [10] made with this thyristor has a

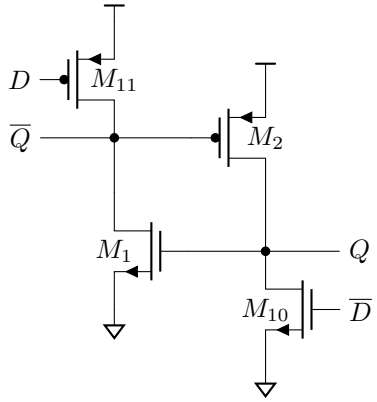


Fig. 3 A thyristor without current sources [4]

temperature coefficient ranging from $20\,000\,\mathrm{ppm/°C}$ at low temperatures to $40\,000\,\mathrm{ppm/°C}$ at high temperatures when a thyristor with a current source made with the same technology only reported $2000\,\mathrm{ppm/°C}$ over the same range.

While using this design produces long delays, i.e., the limit as I_{ctrl} approaches zero, the value of that delay is difficult to calculate. An approximation can be made, where only the subthreshold current of one of the main transistors is considered and the other is assumed to be completely OFF [11]. The weak positive feedback that is ignored shortens the delay of this design, and so that approximation merely gives an upper bound.

Using the exponential model for the subthreshold currents of the transistors, an equation that considers the weak positive feedback can be solved [5]. The result of that is as shown in equation 3, along with supporting equations 4-5. Here, ηV_T is the subthreshold swing, W_p/L_p is the sizing of M_2, and W_n/L_n is the sizing of M_1. As for V_{tp} and V_{tn}, these are the respective gate-to-source voltage where the drain current is $100\,\mathrm{nA}$ for PMOS and NMOS transistors.

$$t_d = \frac{\eta V_T}{K_p - K_n} \ln\left(\frac{K_p}{K_n}\right) \tag{3}$$

$$K_p = \frac{100\,\mathrm{nA}}{C_{g,1}} \cdot \frac{W_p}{L_p} \cdot \exp\left(\frac{-V_{\text{tp}}}{\eta V_T}\right) \tag{4}$$

$$K_n = \frac{100\,\mathrm{nA}}{C_{g,2}} \cdot \frac{W_n}{L_n} \cdot \exp\left(\frac{-V_{\text{tn}}}{\eta V_T}\right) \tag{5}$$

It is certainly a more involved equation, but it still does not capture the delay of this version of the thyristor completely. The exponential model severely underestimates the currents when the gate-to-source voltage is near zero, and so the result here is again higher than the real value. Adding the missing currents as a constant current based on simulations does not resolve into a simple, closed-form solution, so further approximations are needed for a model outlining the delay of the CMOS thyristor without a current source.

Relying on simulations may also not be advisable. It has been shown that physical measurement of the frequency of a thyristor-based oscillator is around half of what simulations give [11]. In addition, it has also been shown that the delay of a thyristor-based delay chain from the layout simulations is 1.8 times higher than that of the schematic simulations [10]. The promise of generating a lot of delay for a minuscule amount of capacitance, current, power, energy, and area has the disadvantage of being easily swayed by any disturbance.

C. *Thyristor with Threshold Elevation*

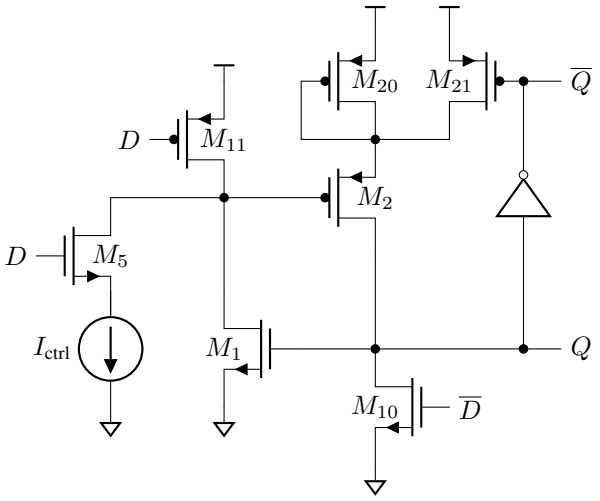


Fig. 4 A thyristor with its threshold voltage elevated [12]

To further lengthen the delay of the CMOS thyristor, the effective threshold voltage can be increased by adding transistors to the stack [12]. In the case of the circuit shown in figure 4, the addition of M_{20} increases the voltage that must be reached to the threshold voltage of M_2 *plus* the threshold voltage of M_{20}. This effectively doubles the delay of the thyristor.

The addition of M_{20} also lowers the final voltage of Q to the drain voltage of M_{20}, so M_{21} is also added to fully pull Q to supply when Q is already high enough to toggle the inverter.

Adding more diode-connected transistors to the stack can further amplify the delay. It is limited by supply voltage, however, as eventually the voltage of Q will be too low to turn ON M_1 or to toggle the inverter such that positive feedback is no longer possible.

D. *Thyristor with Opposing Current Source*

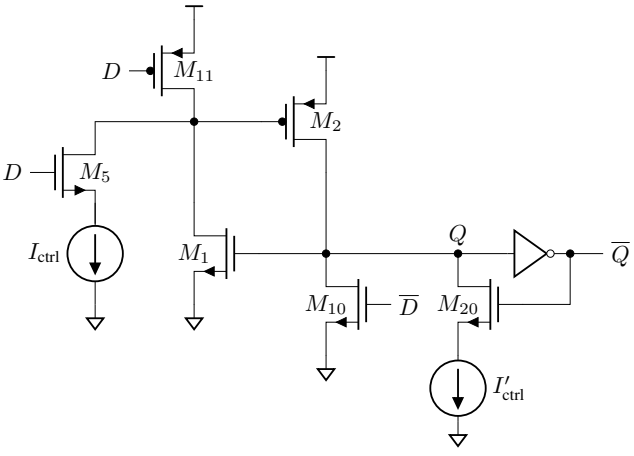


Fig. 5 A thyristor with opposing current source [12]

Another way to lengthen the delay, as shown in figure 5, is to sink the subthreshold currents on the other side of the thyristor [12]. As long as the current through M_2 is weaker than that of I'_{ctrl}, Q will remain low and M_1 will remain off. By preventing the opposite node from slowly rising up until the threshold voltage is reached, the contribution of M_1 in pulling M_2 is minimized up until the trigger point.

The higher I'_{ctrl} is, the longer the resulting delay would be. Simply adding the opposing current has a large effect, from 30% to 1800%, as seen in figure 6. As I'_{ctrl} is further increased, the change in delay is marginal. Taken to the extreme, however, the thyristor can stop working as M_2 can no longer pull M_1 up, even when it is fully ON. Very long delays can then be achieved just with this design by making I'_{ctrl} very close to the saturation current of M_2. It just becomes asymptotically difficult to control.

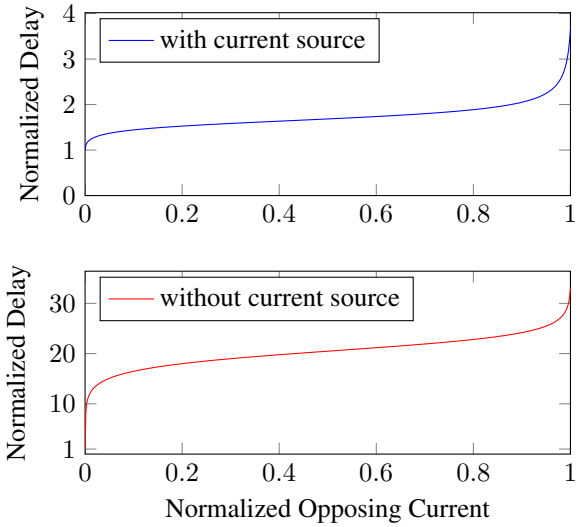


Fig. 6: Delay normalized to delay without opposing current vs opposing current normalized to infinite delay opposing current of a thyristor with current source (top) and without current source (below). These results are from our simulations with 32nm PTM LP transistors.

For the case of the thyristor without the current source, the opposing current multiplies the length of the delay a few times, more pronounced than that of thyristors with current sources, in which the delay only increases by a fraction of the original delay. Keeping M_1 from increasing its current exponentially drastically lengthens the time M_2 needs to turn ON.

E. *Single-ended Thyristor*

CMOS thyristors can be chained together to make ring oscillators or delay chains like the CMOS inverter by directly connecting the complementary outputs of one thyristor to the complementary inputs of the other. By crossing the inputs or not, one can select whether the next stage delays or resets, effectively configuring the falling and rising delay or duty cycle of a chain or a ring. Figure 7 shows the two extremes, one which acts like a thyristor with four times the delay and the other in which both the rising and falling is delayed by two thyristor delay lengths.

A single-ended version of the thyristor can also be made by adding CMOS inverters in between stages as shown in figure 8. For one, adding these inverters separate each stage's

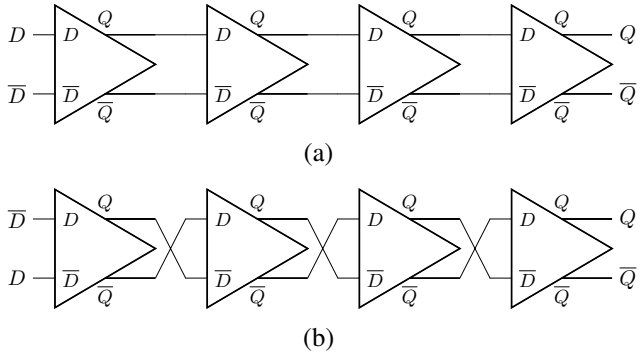


Fig. 7: With each triangle being a thyristor, chain (a) has a long rising delay and a short falling delay while chain (b) has about equal rising and falling delays [10]

capacitances, making the delay equation simpler. Another is that the input signal of each stage is sharp. Connecting the thyristors directly would lead to each stage already partially discharging even before the positive feedback of the previous stage activating, producing shorter delays. That said, the CMOS inverters are then the ones partially on, leading to additional dynamic power consumption.

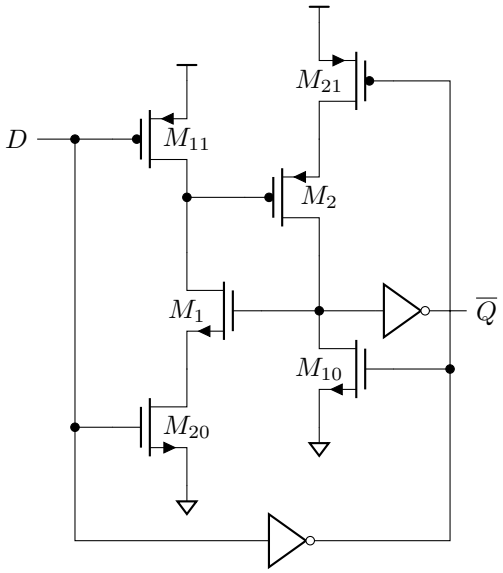


Fig. 8 A single-ended thyristor [11]

F. *Thyristor-type Feedback Delay Element*

Another possible design is with thyristor-like feedback. Instead of using the basic thyristor circuit, this uses CMOS inverters with the input driven by a current source. Once the inverter triggers, the current source input is helped by additional transistors and so starts a positive feedback loop.

In the design shown in figure 9, the first stage (the two current sources, M_5, and M_6) is treated like a current-starved inverter which slowly drives the second stage (M_2, M_4, M_{11}, and M_{13}) with a small current. Once that second stage triggers, transistors M_1 and M_3 are activated, and the current-starved inverter is no longer starved. The unstarved inverter now drives the second stage strongly. Like with the thyristor, positive feedback happens after some trigger point ending the delay.

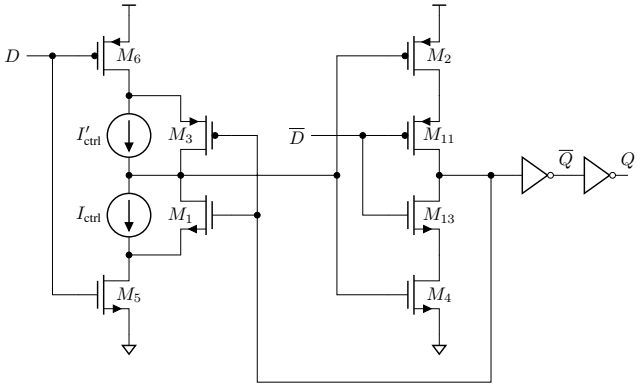


Fig. 9 A delay element with thyristor-like feedback [3]

Upon further inspection, the circuit in figure 9 is similar to that of the complementary thyristor of figure 2. Corresponding transistors and current sources in both circuits have the same names to show the connection. The only differences are that M_{10} and M_{12} are missing and the locations of the current sources and transistors M_5 and M_6 are swapped. Transistors M_5 and M_6 are made to carry the roles of M_{10} and M_{12} in breaking the positive feedback by breaking the connections to the supply rails as opposed to M_{10} and M_{12}'s breaking of the connections to the outputs. Figure 10 shows one-half of the circuit redrawn to resemble more the complementary thyristor.

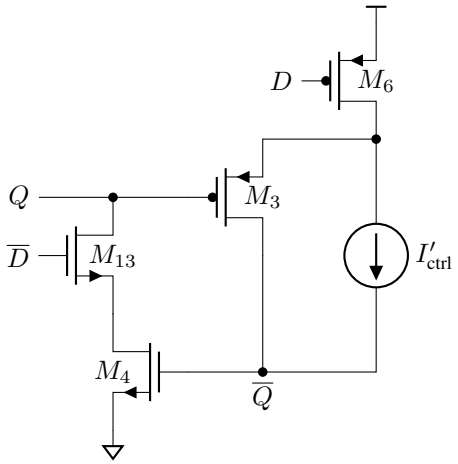


Fig. 10: One half of figure 9 [3] redrawn to resemble the complementary thyristor.

While this is still a design with hidden thyristors, this design does reduce the number of transistors needed by two and gives a different perspective on how the thyristor works. An earlier work [13] has M_2 swapped with M_{11} and M_{13} swapped with M_4, following the design of power-gated inverters to select which positive feedback to enable to prevent the inverter from having large crowbar currents. Another work [14] has M_{11} and M_{13} missing as well. The first thyristor-like circuit [2] is like a basic thyristor with the current source replaced with a current-starved inverter but there are already hints of all of it being inverters. These papers recognize that the mechanism is based on thyristors (hence thyristor-like circuits), but their reasoning leans more on inverters with positive feedback. That thinking led to variations common to that of inverters, allowing new improvements in the design of these thyristor-based delay elements.

IV. Design Considerations

With the variations in design presented in section III, there are still some properties that are common to all thyristors. This section discusses a few points to consider when designing a CMOS thyristor-based delay element.

A. Selection of Topology

The first step in the design process is selecting the thyristor variation to use. Each one has their own strengths and weaknesses. The original thyristor or the basic thyristor is stable to supply voltage and temperature, beneficial for references. The thyristor without the current source produces long delays for minimal area and power, but very sensitive to temperature. That would be good for very-low-power applications or for temperature sensing. Adding inverters between stages makes the per-stage delays consistent, which may be useful for delay-locked loops or for time-to-digital converters. If the required delay is long, using threshold elevation and/or opposing current sources before resorting to increasing the number of stages or adding more capacitance may be beneficial in terms of area.

A thing that is common to all the thyristors is their sensitivity to capacitance. As these thyristors produce a large amount of delay using only small capacitances, adding capacitance, explicit or through parasitics, has a significant effect. The amount of delay thyristors produce per unit capacitance is high. While that may be beneficial if the thyristor is to be used for measuring capacitance, but for other applications, this may require some additional planning in the layout.

B. Main Transistor Sizing

The main transistors have two functions: the storage capacitance and the output drive strength. The larger the transistors, the longer the delay as the gate capacitance increases. The larger the width-to-length ratio, the stronger the output load is driven. This also governs how strong the positive feedback would be.

For the thyristor without the current source, sizing of the main transistors also vary the currents that determine the delay of the thyristor. Scaling the length decreases the current and increases the capacitance, so the delay is expected to lengthen. Scaling the width increases both the current and the capacitance, so the delay is expected to be about the same. When both are scaled, the capacitance increases quadratically while the current stays the same, so the delay is expected to increase quadratically as well. Figure 11 shows the effect of scaling on a 1x1μm 32nm LP PTM thyristor with 1:2 NMOS to PMOS ratio that we have simulated.

C. Capacitive Loading

To extend the delay, additional capacitance can be added at the gates of the main transistors. Invariant of thyristor design, the added delay is linear to the added capacitance. As such, the high sensitivity to capacitance of thyristors can be alleviated by explicitly loading the circuit with capacitors. The delay per unit capacitance is still the same, but the normalized delay per unit capacitance would be lower because

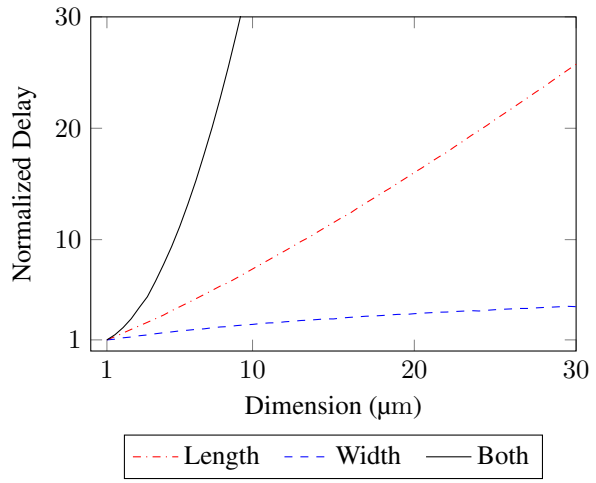


Fig. 11: Effect of scaling the main transistors's length, width, or both to the delay of a thyristor without current sources.

the delay element now has a higher delay. It may be beneficial to load the thyristors with capacitors first before increasing the number of stages if sensitivity to capacitance is important.

D. *Reset Transistor Sizing*

The reset transistors control the output drive strength, though at the opposite edge as that of the main transistors. Also, the reset transistors must be able to break the positive feedback of the main transistors. Failing to do so leaves the nodes hanging in between the rails, leading to high static power consumption and the circuit not working as a delay element. Using wider reset transistors, however, increases the reset transistor's off current and capacitance at the gates of the main transistors leading to increased delay.

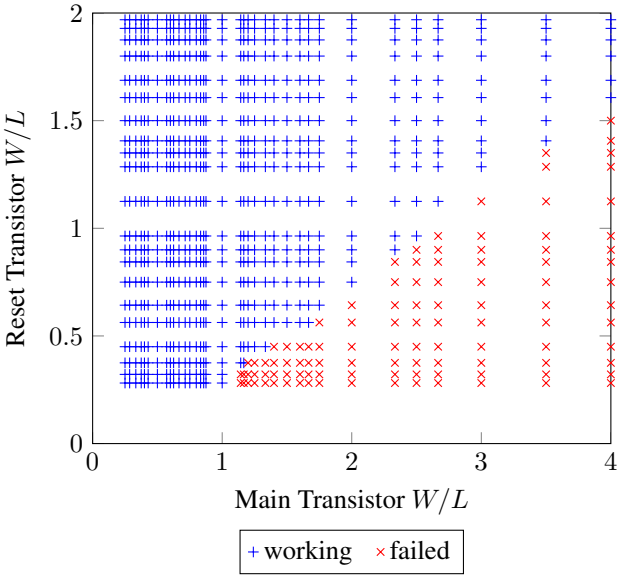


Fig. 12: Thyristors of various sizes in a 65nm process. Note that there are combinations of main and reset transistor sizes that result in a non-working delay element.

From our simulations on a 65nm process, thyristors (without current sources) can properly reset if the ratio of the reset transistors is some proportion of the main transistors. The main NMOS transistor's width and length were both swept from $1\,\mu m$ to $4\,\mu m$. The reset NMOS transistor's width is swept in multiples of the minimum width and length. As for the PMOS counterparts of these transistors, their width are 2.3 times that of the NMOS and the length are the same as the NMOS, since CMOS inverters are balanced with that PMOS/NMOS ratio in that process. Whether each combination of reset transistor size and main transistor size works as a delay element is shown in figure 12. A clear dividing line can be seen between the working and failed ratio combinations, showing that the reset transistor must be of at least some size. Getting the equation of that line gives a result that the reset transistor ratio must be at least 0.6 times that of the main transistor ratio.

V. Conclusion

The CMOS thyristor delay element was presented in this paper – from its basic operation to six other circuits that showed improvements from the original design. The CMOS thyristor has been shown to have a wide delay range, can be sensitive or insensitive to temperature, and sensitive to capacitance while consuming a low amount of power and energy.

In terms of designing these delay elements, there are a few things to consider. Aside from selecting or creating a design to use, the sizing of the main and reset transistors determine the delay range available to the circuit. Additional explicit capacitors can further slow the thyristor, but it could get extremely slow due to its high sensitivity to capacitance. There also exists conditions where the thyristor fails as a delay element, like when the reset transistors are too weak or the opposing currents are too strong. All in all, we see a lot of possibilities for the use of CMOS thyristors as delay elements for sensing temperature or capacitance, for massively delaying short pulses, tap delays for CTDSPs, and tunable delays for DLLs.

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