Analysis and Design Procedures of CMOS OTAs Based on Settling Time

Hamed Aminzadeh[1], and Dalton Martini Colombo[2]

[1] Department of Electrical Engineering, Payame Noor University (PNU), 19395–4697, Tehran, Iran
[2]Electrical Engineering Department, Federal University of Minas Gerais, 31270-901, Belo Horizonte, Brazil,
E-mail: h.aminzadeh@ieee.org

***Abstract*—Analysis of generic single-pole, two-pole, and three-pole operational transconductance amplifiers (OTAs) is carried out based on settling time. The most important design metrics of the open-loop frequency response, such as the stability margins and the gain-bandwidth product (GBW) are related to the settling time of single-, two- and three-stage OTAs in closed-loop configuration, enabling to present a design procedure for each OTA based on the settling time specifications. Transistor-level design examples are provided for each case to validate the described settling-based design strategies.**

***Index Terms*—Design procedures, frequency compensation, Miller compensation, operational transconductance amplifier, opamp, OTA, settling time.**

I. Introduction

The settling time of an amplifier is defined as the time interval by which its output step response enters and remains within an error band around the final steady-state value by applying a step voltage to the input [1-5]. Setting this parameter is a primary task in designing the switched-capacitor (SC) circuits used in discrete-time filters and data converters. Moreover, it is also an important design metric in the case of the continuous-time G_m-C filters, low-dropout regulators (LDOs), voltage and current references, and power amplifiers [6-12]. Depending on the application of concern, a fast-settling response with sufficient accuracy is demanded with minimal power consumption from the OTA embedded in the core of analog or mixed-signal circuits. Despite the great efforts made to characterize the settling response of an OTA and improvise proper optimization strategies from this perspective, designers still face challenges to address the settling requirements of an OTA in advanced CMOS technologies. One of the design factors which is challenging to fulfill despite the reduced intrinsic gain of scaled MOS devices is the accuracy requirement of the settling response. As such, the DC gain of the closed-loop single-stage OTAs is found to be insufficient for many applications, while increasing the number of cascaded stages leads to bandwidth degradation [13]. Frequency compensation is another requirement to keep multistage OTAs stable in a feedback configuration, although making the settling response more complicated than a single-pole system [14].

Regardless of the topology, the implementation of an OTA should be such that the desired settling time is unconditionally met, given that the power consumption should be optimized with minimum silicon resources. Many analytical strategies are thus provided to relate settling time to the sizing of an OTA. The settling time can be evaluated within this framework by assuming that the step response is a purely stochastic process [15]. Another strategy is to assume that the OTA is a purely linear system and to measure the settling time based on an iterative process [16]. Correspondingly, many solutions have been proposed to analyze the settling response of a linear system [4, 5, 15]. However, these methodologies do not account for the large-signal operation of the transistor-level OTAs in the presence of process, voltage, and temperature (PVT) variations. Many design rules and optimization procedures have thus been addressed to also account for the limitations of a transistor-level implementation, including those solutions relying on the location of the poles and zeros of transfer function [17], variations of the slew-rate (SR) [18], and the role of damping factor in closed-loop settling response [3, 19]. Depending on the desired settling time, a robust design approach has been formulated in [20] despite the statistical process variations. Another method estimates the settling time given the symbolic transfer function of an OTA for an arbitrary number of poles and zeros [21]. Likewise, the settling response has been modeled using the generalized relationship between the settling time and frequency response specifications of an OTA having multiple pole-zero pairs [22]. In addition to professional design strategies, new frequency compensation solutions have been also proposed to improve the settling response of an OTA by pushing further the frequency of the non-dominant poles to high frequencies [23].

Efficient design techniques have been addressed given the schematic of the OTA with a predetermined number of the gain stages. Within this framework, the settling response of single-stage OTAs has been analyzed based on the optimized settling model [24, 25], and by taking into account the large-signal operation besides the small-signal constraints. Extension of the corresponding methodology to multistage OTAs leads to efficient design procedures for two-stage Miller-compensated OTAs [26-28], two-stage Miller-compensated OTAs with current buffers [29], and three-stage nested-Miller compensated (NMC) amplifiers [30]. Similar strategies enabled the evaluation of the settling error of the two-stage Miller-compensated OTAs used in SC applications [17, 31]. Settling-time-oriented design techniques were also proposed to realize two-stage OTAs with Miller compensation and current buffers [32], through which an optimized settling response was achieved without any time-consuming trial-and-error on the devices' dimensions. In the case of folded-cascode OTAs, the power-efficient design strategies reported in [33] can be additionally used for further optimizing the settling response of the scheme.

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A robust optimization procedure of the settling time for three-stage CMOS OTAs is discussed in [34]. Another technique shapes the settling response of an OTA with three poles using the open-loop damping factor of non-dominant poles despite the PVT variations [35]. The design and optimization of an NMC three-stage OTA are addressed in [36] for SC applications. Another strategy targeting near-to-minimum settling time is discussed in [37]. Similar design procedures originally helped optimize the settling performance of NMC three-stage OTAs [38, 39]. Optimization of small-signal settling time is made possible based on the analytical approach discussed in [40], which also includes the SR limitation of the OTA. This approach is eventually applied to three-stage OTAs with reversed nested-Miller compensation (RNMC).

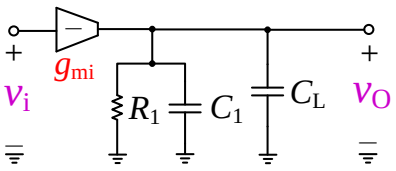
In this paper, we attempt to relate the settling time of a closed-loop OTA to the well-known open-loop specifications such as GBW, phase margin (PM), and damping factor through an approach discussed in [24, 26, 29, 30]. At first, the key settling response expressions are presented in Section II for the case of a single-stage OTA. The derived expressions are eventually generalized to analyze the most important two- and three-stage OTA topologies in Sections III and IV. The transfer function, stability criteria, and design considerations are elaborated on along with design examples in each section. Finally, conclusions are drawn in Section V.

II. Single-Stage OTAs

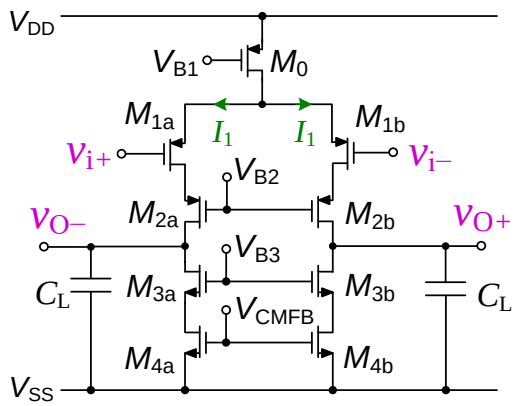
Fig. 1(a) shows the small-signal diagram of a single-stage OTA, where $v_\mathrm{i} = (v_\mathrm{i}^+ - v_\mathrm{i}^-)$ and $v_\mathrm{O} = (v_\mathrm{O}^+ - v_\mathrm{O}^-)$ are the differential input voltage and the single-ended (fully-differential) output voltage, respectively. g_mi is the equivalent OTA transconductance, and R_1 and C_1 are the output resistor and capacitor, respectively. The load capacitor is shown by C_L, whose value is typically much larger than C_1. With a single left-half plane (LHP) pole at the output node, the open-loop voltage-gain transfer function of this OTA is given as [13]:

$$A_\mathrm{V}(s) = \frac{v_\mathrm{O}}{v_\mathrm{i}} = \frac{A_0}{1 + s/|p_{-3\mathrm{dB}}|}, \qquad (1)$$

where $A_0 \approx g_\mathrm{mi}R_1$ and $p_{-3\mathrm{dB}} \approx -1/R_1C_\mathrm{L}$ are the open-loop DC gain and the dominant pole frequency, respectively. Regarding the application, different implementations of this circuit diagram are possible in CMOS technology, including the telescopic-cascode fully-differential scheme with *p*MOS input pair in Fig. 1(b), and the folded-cascode single-ended topology with *n*MOS input pair in Fig. 1(c). In both instances, g_mi is made by $M_{1a} - M_{1b}$ while the bias current is supplied by M_0. The cascode devices, i.e. $M_{2a} - M_{2b}$ and $M_{3a} - M_{3b}$, are also meant for increasing the output resistance of the topology. More immunity against the power supply (V_DD) fluctuations is an advantage of the fully-differential topology over the single-ended configuration.



(a)



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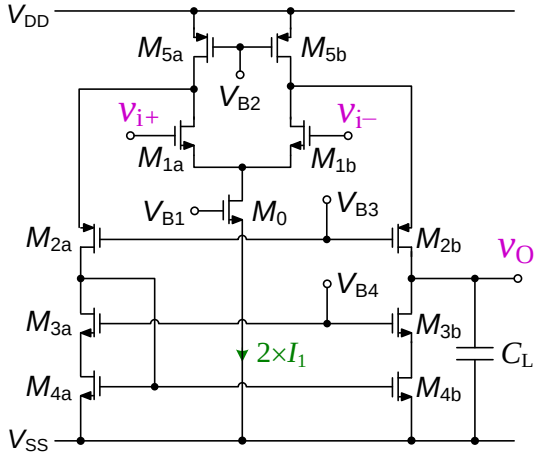
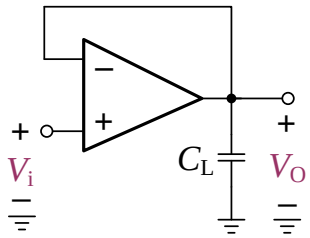


(c)

Fig. 1 (a) Small-signal amplifier diagram of a single-pole OTA;(b) Folded-cascode implementation; (c) Telescopic-cascode implementation.



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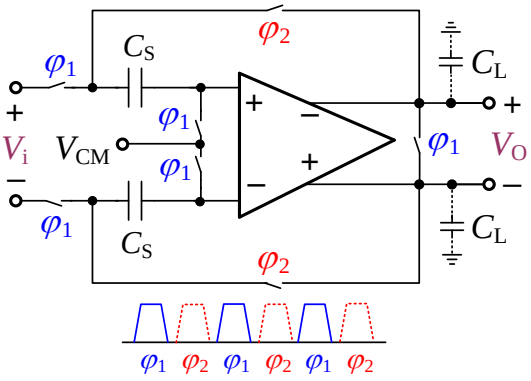


(b)

Fig. 2 (a) Single-ended and (b) fully-differential OTA topologies in closed-loop configuration for a feedback factor of unity.

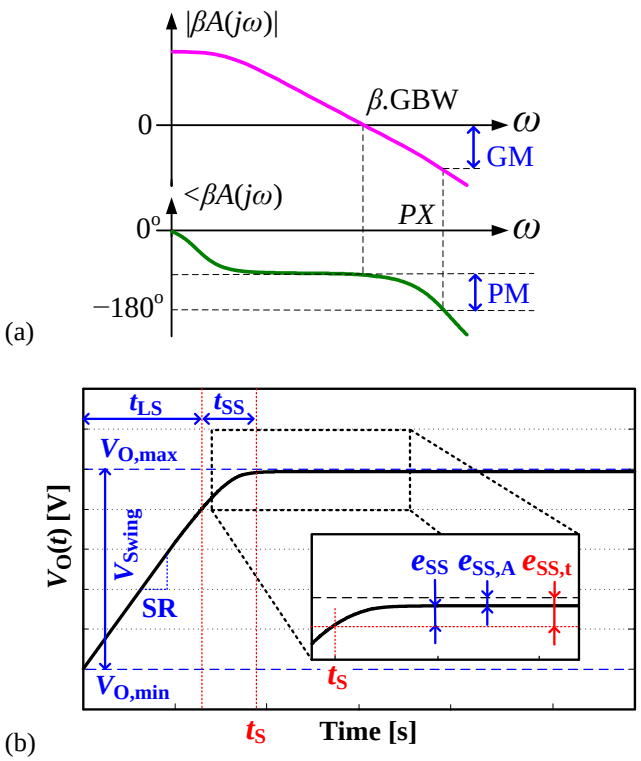


Fig. 3 (a) Loop-gain and (b) step response of an OTA in closed-loop configurations.

Nonetheless, common-mode feedback (CMFB) is required to stabilize the common-mode output voltage (V_{CM}) of the fully-differential OTA in Fig. 1(b). For this purpose, V_{CM} can be at first sensed and then compared with a voltage reference for the error signal (V_{CMFB}) to be subsequently applied to the gate of $M_{4\mathrm{a}} - M_{4\mathrm{b}}$ [41]. The single-ended topology stabilizes V_{CM} at the output by simply using the current mirror devices $M_{4\mathrm{a}} - M_{4\mathrm{b}}$to convert the fully-differential input signal to a single-ended output.

For the desired feedback factor (β), both OTAs in Fig. 1 can be wired such that a prescribed gain factor is obtained with high accuracy. Fig. 2 depicts two familiar OTA configurations for the feedback factor of unity. The output terminal is simply shorted to the inverting v_{i}^{-} input in the case of the single-ended topology in Fig. 2(a). The SC flip-around sample-and-hold amplifier (SHA) in Fig. 2(b), however, requires non-overlapping clock phases to buffer the fully-differential input at the output [31]. Other SC implementations are also available in reference textbooks for alternative feedback factors [41]. For both cases of Fig. 2, Fig. 3(a) illustrates the loop-gain frequency response for arbitrary feedback factor, where:

$$\mathrm{GBW} = A_0 \times |p_{-3\mathrm{dB}}| \approx \frac{g_{\mathrm{mi}}}{C_{\mathrm{L}}}, \tag{2}$$

is the open-loop gain-bandwidth product frequency where $|A_{\mathrm{V}}(j\mathrm{GBW})| \approx 1$, and PX is the phase crossover frequency where $\angle A_{\mathrm{V}}(jPX) \approx -180^{\mathrm{o}}$. The well-known stability margins, i.e. PM and GM, are additionally indicated according to their definitions [41]. Fig. 3(b) shows the settling response of the OTA in closed-loop configurations after a large-signal differential step voltage is applied to input terminals. Depending on the required total settling error ($e_{\mathrm{SS,t}}$), the output voltage $V_{\mathrm{O}}(t)$ initially at $V_{\mathrm{O,min}}$ settles down to the steady-stage $V_{\mathrm{O,max}}$ after a measurable settling time (t_{S}), which can be defined as the first moment the condition $|V_{\mathrm{O,max}} - V_{\mathrm{O}}(t)| < e_{\mathrm{SS,t}}$ is satisfied [24]. The total settling error is composed of two separate sections as graphically specified in Fig. 3(b): $e_{\mathrm{SS,A}}$ due to limited DC gain and e_{SS} due to finite bandwidth of the OTA, which can be formulated as $e_{\mathrm{SS,t}} = e_{\mathrm{SS,A}} + e_{\mathrm{SS}}$. The error caused by the finite DC gain is a function of A_0 and β [41]:

$$e_{\mathrm{SS,A}} = \frac{1}{1 + A_0\beta} \simeq \frac{1}{A_0\beta}. \tag{3}$$

The maximum tolerable settling error due to the bandwidth should be therefore smaller than:

$$e_{\mathrm{SS}} \le e_{\mathrm{SS,t}} - \frac{1}{A_0\beta}, \tag{4}$$

Starting from the open-loop transfer function in (1) and after a few manipulations, the small-signal settling response and e_{SS} of a single-pole closed-loop OTA can be expressed as:

$$V_{\mathrm{O}}(t_{\mathrm{SS}}) \approx V_{\mathrm{Swing}}(1 - e_{\mathrm{SS}}), \tag{5}$$

$$e_{\mathrm{SS}} = \exp\left(\frac{-t_{\mathrm{SS}}}{\tau}\right) = \exp(-\beta\mathrm{GBW} \cdot t_{\mathrm{SS}}), \tag{6}$$

where $V_{\mathrm{Swing}} = V_{\mathrm{O,max}} - V_{\mathrm{O,min}}$ is the peak-to-peak output voltage swing whilet_{SS} is the small-signal settling time. It is defined as the time interval during which the settling response is governed by the small-signal GBW and PM rather than the large-signal SR specifications (see Fig. 3(b)). The closed-loop time-constant is:

$$\tau = \frac{1}{\beta.\mathrm{GBW}}. \tag{7}$$

Equation (6) shows that the relation $\mathrm{GBW} - t_{\mathrm{SS}}$, which can be rearranged as (8):

$$t_{\mathrm{SS}} = n\tau = n\frac{1}{\beta.\mathrm{GBW}}, \tag{8}$$

where n is the number of necessary time constants for the error caused by finite bandwidth to become smaller than e_{SS}. It is a function of e_{SS} and can be expressed as:

$$n = \frac{t_{\mathrm{SS}}}{1/(\beta.\mathrm{GBW})} = \ln\left(\frac{1}{e_{\mathrm{SS}}}\right) = f(e_{\mathrm{SS}}). \tag{9}$$

As shown graphically in Fig. 3(b), the settling time of an OTA consisting of nonlinear MOSFETs can be divided into large-signal settling time (t_{LS}) and small-signal settling time t_{SS} sub-regions. Hence:

$$t_{\mathrm{S}} = t_{\mathrm{LS}} + t_{\mathrm{SS}}. \tag{10}$$

As a conservative approach to evaluate t_{LS}, we assume that the SR-limited region covers the entire V_{Swing}on the vertical axis in Fig. 3(b). Consequently, the conventional definition of the SR can be applied to either topology in Fig. 1 to approximate t_{LS} as:

$$t_{\mathrm{LS}} \approx \frac{V_{\mathrm{Swing}}}{\mathrm{SR}} = C_{\mathrm{L}}\frac{V_{\mathrm{Swing}}}{2I_1}, \tag{11}$$

where I_1 is the quiescent current of $M_{1a} - M_{1b}$.When the input devices are operating at strong-inversion saturation, the conventional square-law model can then be used to relate I_1 to g_{mi} as below:

$$I_1 = \frac{g_{mi} V_{eff,i}}{2}. \quad (12)$$

where $V_{eff,i}$ is the overdrive voltage of the input $M_{1a} - M_{1b}$ pair. Combining (11) and (12), and substituting the GBW product from (2) into the result, the total settling time can be expressed by:

$$t_S = t_{SS} + t_{LS} = \left(\frac{n}{\beta} + \frac{V_{Swing}}{V_{eff,i}}\right)\frac{1}{GBW}. \quad (13)$$

Taking into account both small- and large-signal regions, the relationship between GBW and t_S thus becomes [26]

$$GBW = \left(\frac{n}{\beta} + \frac{V_{Swing}}{V_{eff,i}}\right)\frac{1}{t_S}, \quad (14)$$

where V_{Swing} is considered as the maximum possible output voltage swing to ensure that the resulted GBW satisfies t_S unconditionally. Variable n is referred to as time–constant coefficient, which depends on e_{SS} according to (9). Eq. (14) reveals that the GBW is inversely proportional to t_S, and increases for a particular $t_S$when the expected voltage swing is enlarged for higher accuracy requirement. Besides, the SR can be determined based on t_S according to the GBW–SR expression indicated below:

$$SR = \frac{2I_1}{C_L} = \frac{2I_1}{V_{eff,i} C_L} V_{eff,i} = \frac{g_{mi}}{C_L} V_{eff,i} = V_{eff,i}.GBW. \quad (15)$$

At this stage, we can present a settling-based design procedure for any of the single-stage OTAs shown in Fig. 1 based on the desired V_{Swing}, t_S and $e_{SS,t}$, when the nominal C_L and β are specified a priori. The design flow starts by defining the required DC gain regarding the derived error factor in (3). The OTA topology should also be capable of providing such a DC gain factor. The transconductance of the input devices can be determined by combining (2) with (14) which gives:

$$g_{mi} = C_L\left[\frac{1}{\beta}\ln\left(\frac{1}{e_{SS,t} - 1/A_0\beta}\right) + \frac{V_{Swing}}{V_{eff,i}}\right]\frac{1}{t_S}. \quad (16)$$

The DC current of the input devices which satisfies both large-signal and small-signal operations is subsequently measured by:

$$I_1 = \frac{g_{mi} V_{eff,i}}{2} = C_L\left[\frac{n}{\beta} V_{eff,i} + V_{Swing}\right]\frac{1}{t_S}, \quad (17)$$

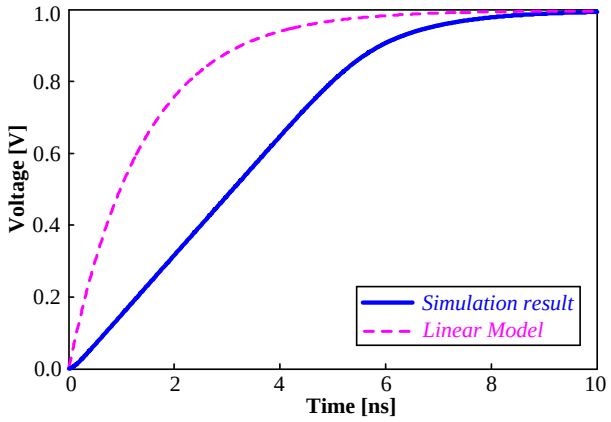
The rest of our design flow is to fulfill the desired performance metrics concerning noise, DC gain, output voltage swing, CMFB, and the location of parasitic poles and zeros.

Circuit-level simulations were conducted in a standard 0.25μm CMOS technology to configure the fully-differential and single-ended topologies in Fig. 1(b) and (c) for inclusion in the unity-gain topologies illustrated in Fig. 2. Table I compares the simulation results with the hand analysis in the case of an SHA driving 5-pF C_L. The 0.5% settling time from simulation results is relatively close to the expected value (9.31 vs. 10.00 ns).

The single-ended OTA is also designed according to the described methodology, and $V_{eff,i} = 135$ mV, $A_0 = 50$ dB, $V_{Swing} = 1Vp - p$ and $g_{mi} = 8.5$ mA/V were obtained from the simulation results. Fig. 4(a) shows the step response for the load capacitor of 10pF. The small-signal step response model is also added for comparison, indicating that the real step response is practically different from the small-signal model because of SR limitations. Fig. 4(b) compares the simulated relation between 0.5% settling time and GBW with Eq. (14). The GBW product is varied by indirectly changing the load capacitor according to (2), revealing that (14) overestimates the required GBW for any settling time. As stated earlier, this is an important property to confirm that the required t_S is fulfilled unconditionally.

Table I. Comparison between simulation and calculations of the SHA.

Parameter	Simulation	Calculation
Overdrive Voltage of Input devices	0.29V	0.3V
Output Voltage Swing	0.9Vp-p	
Load Capacitor (C_L)	5pF	
Feedback Factor (β)	1	
DC Gain	~50dB	50 dB
Total Settling Error	0.5%	
Settling Time	9.31ns	10ns
OTA Transconductance	4.16mA/V	4.15mA/V



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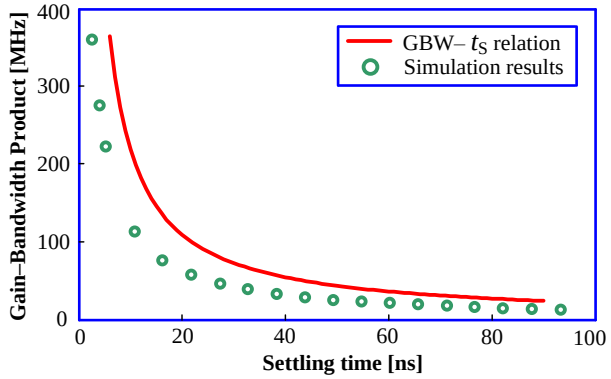

(b)

Fig. 4 Simulation results of the single-ended OTA: (a) Comparison between small-signal and simulated step response for $C_L = 10$ pFC_L; (b) Relationship of GBW and t_S.

III. TWO-STAGE OTAS

A. Miller Compensation

Two-stage OTA is a good candidate for balancing DC gain and bandwidth when both parameters are equally important. In this section, we shall analyze the classical Miller-compensated OTA to be sized according to the settling time. Fig. 5(a) depicts the circuit diagram of this OTA. The first and the second gain stages are modeled by an equivalent transconductance (g_{mi}, g_{mL}), a parasitic output capacitor (C_1, C_2), and an output resistor (R_1, R_2). The compensation capacitor (C_{C}) dominates the pole at the second-stage input and pushes the output pole to higher frequencies. A nulling resistor (R_{C}) is also added to eliminate the right-half–plane (RHP) zero generated by C_{C} [13, 41]. Fig. 5(b) illustrates a possible implementation of this OTA, where the transconductance stages are realized by MOS devices. The single-pole settling model discussed in the previous section is not accurate in modeling the output response of this OTA. Hence, the open-loop voltage gain is derived at first to eventually obtain the settling response of closed-loop OTA [27]:

$$A_{\mathrm{V}}(s)=\frac{v_{\mathrm{O}}}{v_{\mathrm{i}}}=\frac{A_0(1+s/|z_1|)}{(1+s/|p_{-3\mathrm{dB}}|)(1+s/|p_2|)}, \quad (18)$$

where $A_0 \approx g_{\mathrm{mi}}g_{\mathrm{mL}}R_1R_2$and $p_{-3\mathrm{dB}} \approx 1/g_{\mathrm{mi}}g_{\mathrm{mL}}R_1R_2C_{\mathrm{C}}$ are the DC gain and the dominant pole frequency, respectively, and $z_1 = 1/(1/g_{\mathrm{mL}} - R_{\mathrm{C}})C_{\mathrm{C}}$ and $p_2 \approx -1/g_{\mathrm{mL}}C_{\mathrm{L}}$ are the magnitude of the zero and the non-dominant poles, respectively. The GBW is given as:

$$\mathrm{GBW} = A_0 \times |p_{-3\mathrm{dB}}| \approx \frac{g_{\mathrm{mi}}}{C_{\mathrm{C}}}. \quad (19)$$

The zero z_1 moves to infinity when

$$R_{\mathrm{C}}=\frac{1}{g_{\mathrm{mL}}}. \quad (20)$$

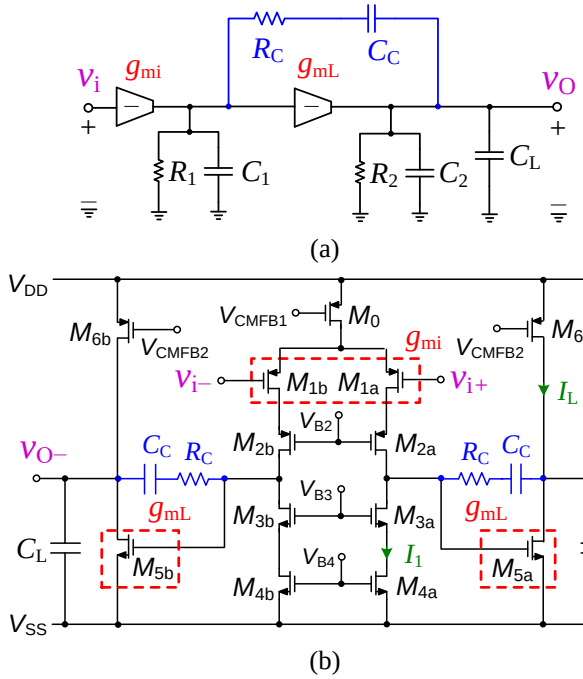

Fig. 5 (a) Amplifier diagram of a two-pole OTA; (b) Circuit-level implementation in the form of a two-stage OTA with Miller compensation.

As such, the transfer function contains two poles only and the PM can be evaluated as:

$$\mathrm{PM} = 90^{\mathrm{o}} - \tan^{-1}\left(\frac{\beta\mathrm{GBW}}{|p_2|}\right) \Rightarrow \tan \mathrm{PM} = \frac{|p_2|}{\beta\mathrm{GBW}}. \quad (21)$$

Calculating the closed-loop voltage gain using (18) and (21), two LHP poles are subsequently obtained:

$$s_{1,2}=\frac{-\beta\mathrm{GBW}\times\tan\mathrm{PM}}{2}\left(1\pm\sqrt{1-\frac{4}{\tan\mathrm{PM}}}\right). \quad (22)$$

To evaluate e_{SS} of the closed-loop system similar to that of (6), $V_{\mathrm{O}}(t)$can be estimated by assuming zero initial conditions ($V_{\mathrm{O}}(0) = 0$ and $dV_{\mathrm{O}}(0)/dt = 0$). When the poles are separated (PM $> 76^{\mathrm{o}}$according to (21)), the result would be:

$$e_{\mathrm{SS}} = \frac{1}{2}\left[1-\frac{1}{\sqrt{1-(4/\tan\mathrm{PM})}}\right]\exp\left[-\frac{W}{2}\left(1+\sqrt{1-\frac{4}{\tan\mathrm{PM}}}\right)\right] + \frac{1}{2}\left[1+\frac{1}{\sqrt{1-4/\tan\mathrm{PM}}}\right]\exp\left[-\frac{W}{2}\left(1-\sqrt{1-\frac{4}{\tan\mathrm{PM}}}\right)\right] \quad (23)$$

while for complex poles (PM $< 76^{\mathrm{o}}$):

$$e_{\mathrm{SS}} = 2\frac{\exp(-W/2)}{\sqrt{4-\tan\mathrm{PM}}}\sin\left[\frac{W}{2}\sqrt{\frac{4}{\tan\mathrm{PM}}-1}-\tan^{-1}\left(-\sqrt{\frac{4}{\tan\mathrm{PM}}-1}\right)\right]. \quad (24)$$

where $W = |p_2|t_{\mathrm{SS}}$. The e_{SS} derived from either (23) or (24) is based on the conservative zero initial conditions. As such, the required t_{SS} will be overestimated, ensuring that the required settling time is unconditionally guaranteed.

An analysis similar to the case of single-stage OTAs yields an expression similar to (14) for the two-pole OTA analyzed in this section. Nonetheless, it is essential to find the equivalent time-constant coefficient with a similar definition of (9). The result, in the form of (25), is a nonlinear function of e_{SS} and PM:

$$n=\frac{t_{\mathrm{SS}}}{1/\beta\mathrm{GBW}}=\frac{W}{\tan\mathrm{PM}}=f(e_{\mathrm{SS}},\mathrm{PM}). \quad (25)$$

It is not straightforward to find a closed-form expression similar to (9). Nonetheless, given that e_{SS} and PM should be specified a priori, a computational program can solve (25) using (23) and (24). Table II presents the result, together with the 3-D waveform in Fig. 6, which presents the n values as a function of the error percentage and PM. As expected, the derived time-constant coefficients for higher PM values tend to be the results from (9) for single-stage OTAs with PM $\approx 90^{\mathrm{o}}$. The time-constant coefficient has also fewer PVT variations for higher PMs. However, the price is the extra current required for pushing the parasitic poles to higher frequencies. From another perspective, higher settling error decreases n and, eventually, the required GBW for unchanged settling time (Eq. (14)), yielding lower power consumption in less silicon area.

Table II. Time-constant coefficient vs. phase margin and settling error

	e_{SS} (%)							
PM (°)	0.005	0.01	0.02	0.05	0.10	0.20	0.50	1.00
10.0	111.31	103.48	95.661	87.304	79.451	71.565	57.020	49.197
20.0	55.574	50.925	45.898	40.495	38.77	34.337	28.965	23.938
30.0	33.269	32.389	28.683	24.504	23.845	19.918	18.787	15.142
40.0	24.064	21.111	20.515	17.247	16.619	13.509	12.755	9.6133
50.0	15.645	15.268	14.671	12.064	11.623	10.807	8.4823	7.9482
55.0	14.200	11.781	11.529	10.933	8.5137	8.2624	7.6655	5.2465
60.0	11.215	10.838	10.273	8.1996	7.9168	7.4770	5.1522	4.9323
65.0	8.4195	8.2310	7.9796	7.4456	6.8487	5.1836	4.8695	4.5239
70.0	7.7283	7.0686	5.7491	5.4978	5.2465	4.9009	4.3354	3.5814
75.0	4.8695	4.7438	4.5867	4.3040	4.0841	3.8013	3.4243	3.1102
80.0	7.8226	7.2885	6.7544	6.0633	5.5292	4.9951	4.3040	3.7699
85.0	8.9850	8.3566	7.7283	6.9115	6.2832	5.6549	4.8381	4.2097
89.5	9.8332	9.1420	8.4509	7.5398	6.8487	6.1575	5.2465	4.5553

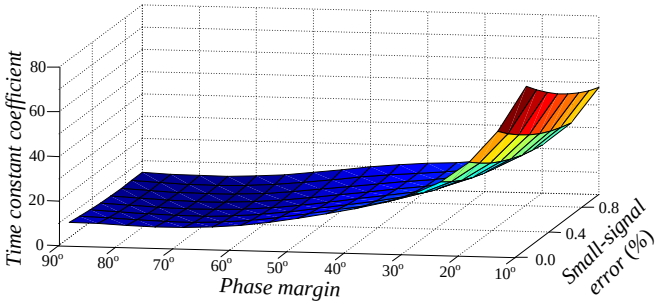

Fig. 6: Time-constant coefficient as a function of phase margin and small-signal settling error.

The analysis presented above helps to determine the trans-conductances of the Miller-compensated OTA in Fig. 5(b) based on settling time. At first, combining (14) and (19) gives the following g_{mi} as a function of t_{S}:

$$g_{\mathrm{mi}} = C_{\mathrm{C}}\left(\frac{n}{\beta}+\frac{V_{\mathrm{Swing}}}{V_{\mathrm{eff,i}}}\right)\frac{1}{t_{\mathrm{S}}}. \tag{26}$$

From (21), g_{mL} is measured as:

$$g_{\mathrm{mL}} = \frac{C_{\mathrm{L}}}{C_{\mathrm{C}}} g_{\mathrm{mi}} \times \beta \times \tan \mathrm{PM}. \tag{27}$$

Resistor R_{C} is then set in line with (20) for the RHP zero to be moved to infinity. Its value changes across the different process and temperature corners. This is not, however, a problem for the OTA operation since R_{C} is not meant for generating an LHP zero for pole-zero cancellation. The current of the input devices is finally determined from (12).

The effectiveness of the derived expressions is validated through simulations in a standard 0.18-µm CMOS process. The unity-gain flip-around SHA shown in Fig. 2(b) was realized based on the OTA configuration in Fig. 5(b) as the core. Table III compares the calculations with simulation results.

Table III. Comparison of simulated results and calculation

Parameter	Simulated	Calculated
C_{L} , C_{C}	1.0pF,1.8pF	1.0pF,1.8pF
R_{C}	80Ω	80Ω
DC gain	92 dB	90dB
GBW	157MHz	159MHz
PM	73°	71°
0.05% Settling Time	6.34ns	6.50ns
Power	6.80mW	6.81mW

B. Miller Compensation Employing Current Buffers

Fig. 7 shows the circuit diagram and schematic of a two-stage OTA with Miller compensation and current buffers. Referred to as cascode-compensated OTA, it comprises a telescopic-cascode first stage and a common-source second stage. The purpose of the g_{mC} stages with input resistance $1/g_{\mathrm{mC}}$ in the small-signal equivalent circuit is to reduce the direct capacitive loading of C_{C} on the OTA output, thereby, non-dominant poles are located at higher frequencies concerning classical Miller compensation. Solving the small-signal expressions after compensation, the open-loop transfer function can be derived as[29]:

$$A_{\mathrm{V}}(s) = \frac{v_{\mathrm{O}}}{v_{\mathrm{i}}} \approx \frac{\mathrm{A}_0\left(1-\frac{s^2}{|z_{1,2}|^2}\right)}{\left(1+\frac{s}{|p_{-3\mathrm{dB}}|}\right)\left[1+\left(\frac{2\xi_0}{\omega_{\mathrm{n0}}}\right)s+\frac{s^2}{\omega_{n0}^2}\right]}, \tag{28}$$

where $A_0 \approx g_{\mathrm{mi}} g_{\mathrm{mL}} R_1 R_2$ and $p_{-3\mathrm{dB}} \approx 1/g_{\mathrm{mi}} g_{\mathrm{mL}} R_1 R_2 C_{\mathrm{C}}$ are the dc gain and the frequency of the dominant pole, respectively, and the GBW relation is similar to (19). The above open-loop transfer function has one dominant and two non-dominant poles. Non-dominant poles become complex for a damping factor (ξ_0) smaller than unity. The transfer function also contains two zeros, one at the RHP and the other one at the LHP.

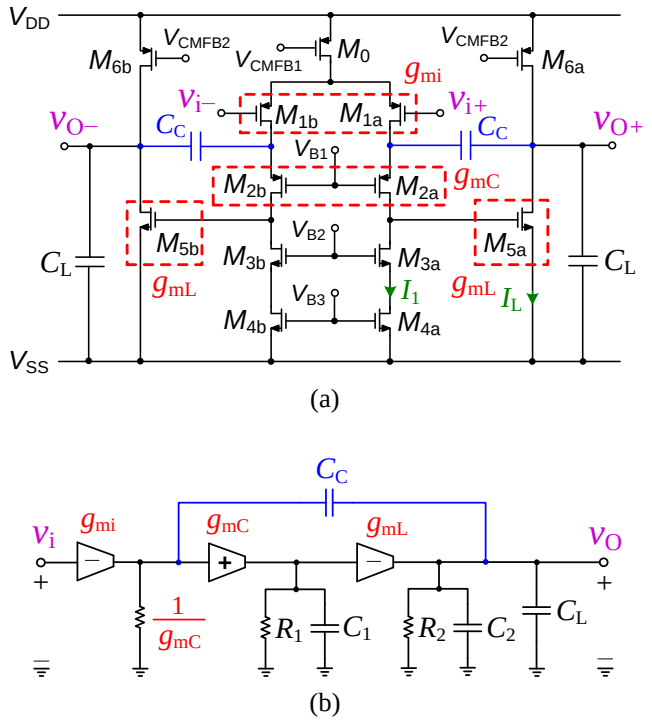

Fig. 7 (a) A fully-differential two-stage OTA with Miller compensation and current buffers; (b) Small-signal equivalent circuit.

The frequency of zeros is given as:

$$z_{1,2} = \pm j\sqrt{\frac{g_{mC}g_{mL}}{C_2 C_C}} \tag{29}$$

The damping factor (ξ_0) and the natural frequency (ω_{n0}) are additionally expressed by:

$$\omega_{n0} = \sqrt{\frac{g_{mC}g_{mL}}{C_2 C_L}}, \tag{30}$$

$$\xi_0 = \frac{1}{2}\left(1+\frac{C_L}{C_C}\right)\sqrt{\frac{g_{mC}}{g_{mL}}\cdot\frac{C_2}{C_L}}. \tag{31}$$

It is relatively challenging to include the effect of the zeros in (29) when analyzing (28). An elegant way of making the analysis more accurate is to consider their impact on the generic second-order polynomial of $A_V(s)$. Coined as effective damping factor (ξ'_0) and effective natural frequency (ω'_{n0}), the original damping factor and natural frequency can thus be modified such that the effects of zeros are accounted for as well:

$$\frac{1-s^2/|z_{1,2}|^2}{1+(2\xi_0/\omega_{n0})s+s^2/\omega_{n0}^2} = \frac{1}{1+(2\xi'_0/\omega'_{n0})s+s^2/\omega'^2_{n0}}$$

$$\Rightarrow 1+\left(\frac{2\xi'_0}{\omega'_{n0}}\right)s+\frac{s^2}{\omega'^2_{n0}} \approx 1+\left(\frac{2\xi_0}{\omega_{n0}}\right)s+s^2\left(\frac{1}{\omega_{n0}^2}+\frac{1}{|z_{1,2}|^2}\right). \tag{32}$$

ξ'_0 and ω'_{n0} are consequently given by:

$$\omega'_{n0} = \sqrt{\frac{g_{mC}g_{mL}}{C_2(C_L+C_C)}}, \tag{32}$$

$$\xi'_0 = \frac{1}{2}\sqrt{\frac{g_{mC}}{g_{mL}}\cdot\frac{C_2(C_L+C_C)}{C_C^2}}. \tag{33}$$

The original transfer function can be approximated as:

$$A_V(s) = \frac{A_0}{(1+s/|p_{-3dB}|)[1+(2\xi'_0/\omega'_{n0})s+s^2/\omega'^2_{n0}]}. \tag{34}$$

From this expression, the relationship between PM and GBW can be evaluated as:

$$\tan(\mathrm{PM}) = \frac{1-(\beta\mathrm{GBW}/\omega'_{n0})^2}{2\xi'_0(\beta\mathrm{GBW}/\omega'_{n0})}. \tag{35}$$

Equation (35) has been derived based on the assumption that the effect of non-dominant parasitic poles and zeros is negligible on the loop-gain transient frequency (where $|\beta A_V(j\mathrm{GBW})| \approx 1$). As such, this parameter is approximated as βGBW similar to the case of single-pole OTAs. This approximation is valid for typical PM values. From (35), GBW can be expressed in terms of PM as:

$$\mathrm{GBW} = \frac{1}{\beta}\frac{\omega'_{n0}}{\xi'_0\tan(\mathrm{PM})+\sqrt{1+\xi'^2_0\tan^2(\mathrm{PM})}}. \tag{36}$$

The lower the effective damping factor, the higher the GBW, according to (36). However, this is not essentially helpful since the relative distance between ω'_{n0} and the GBW reduces for identical PM, finally inducing a peak in the closed-loop frequency spectrum and degrading the stability. Hence, keeping unchanged $\xi'_0\tan(\mathrm{PM})$ is essential for proper operation and a lower ξ'_0 must be compensated by a higher PM. Similar steps to the case of single-stage OTAs can be followed to derive a GBW $- t_S$ expression similar to (14) for the two-stage OTA in this section. It is, however, essential to determine the modified *n* formula with the same definition as (9). The equivalent formula for the third-pole system presented in Fig. 7 is a nonlinear function of e_{SS}, ξ'_0 and PM:

$$n = \frac{t_{SS}}{1/\beta\mathrm{GBW}} = f(e_{SS}, \xi'_0, \mathrm{PM}). \tag{37}$$

The analysis for extracting the exact n expressions starts by evaluating at first the e_{SS} of a three-pole system [5]:

$$e_{SS} = \frac{1}{1-2\alpha\xi^2+\alpha^2\xi^2}\exp(-\alpha.\xi.W) + \frac{\alpha\xi\exp(-\xi.W)}{1-2\alpha\xi^2+\alpha^2\xi^2}\left[(-2\xi+\alpha\xi)\cos\left(W\sqrt{1-\xi^2}\right) + \frac{1-2\alpha\xi^2+\alpha^2\xi^2}{\sqrt{1-\xi^2}}\sin(W\sqrt{1-\xi^2})\right], \tag{38}$$

where ξ and ω_n are the damping factor and natural frequency of the closed-loop OTA, and $W = \omega_n t_{SS}$ and $\alpha \approx \beta\mathrm{GBW}/\xi\omega_n$. These variables are related to the open-loop parameters:

Table IV. Time-constant coefficient vs. PM and ξ'_0 for an e_{SS} of 0.05%.

ξ'_0 / PM	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**	**1.0**
10°	295.30	90.630	59.812	49.348	42.507	40.573
20°	130.06	58.240	40.293	33.145	31.340	29.613
30°	74.584	40.149	28.578	24.329	22.581	20.889
40°	44.963	26.911	18.919	16.956	15.410	15.832
50°	27.573	17.466	12.284	10.870	11.218	9.8727
55°	21.612	12.689	9.4958	8.2693	8.7534	9.1247
60°	16.201	9.7662	7.0011	7.2211	6.5070	6.8769
65°	11.427	7.1280	4.8382	5.2276	5.6526	6.0463
70°	7.2782	5.6927	4.7437	4.1885	4.1078	4.7600
75°	6.1976	5.8045	5.6007	5.4397	5.2231	5.1993
80°	6.4961	6.3998	6.3373	6.2932	6.2622	6.2398
85°	7.0286	7.0103	6.9987	6.9917	6.9868	6.9837
89°	7.4857	7.4851	7.4848	7.4845	7.4844	7.4843

$$\xi'_0 = \frac{\xi + 0.5.\alpha.\xi}{\sqrt{1 + 2.\alpha.\xi^2}}, \tag{39}$$

$$\omega'_{n0} = \omega_n\sqrt{1 + 2.\alpha.\xi^2}. \tag{40}$$

The modified time-constant coefficient derived from (38) is nonlinear and cannot be expressed using conventional mathematical functions. A computational program was consequently written to numerically estimate n for the prescribed PM, ξ'_0 and e_{SS}. The 3D surface in Fig. 8 has been drawn based on the results for $e_{SS} = 0.05\%$. The values are also tabulated in Table IV for future reference, revealing that the results for PM $\approx 89^o$ are almost identical to those derived from (9) (PM $= 90^o$).

It is now possible to present a well-defined design methodology for two-stage cascode-compensated OTAs based on the derived equations. The design procedure starts by choosing the transconductance of input transistors according to (26) for the required settling time to be satisfied. Substituting ω'_{n0} and ξ'_0 by their corresponding values from (32) and (33) into (36), and after some routine algebra, g_{mC} and g_{mL} are then related to g_{mi} and, in turn, t_S by:

$$g_{mC} = 2.\beta.\xi'_0.(\xi'_0\tan(\mathrm{PM}) + \sqrt{1 + \xi'^2_0\tan^2(\mathrm{PM})})g_{mi}, \tag{41}$$

$$g_{mL} = \frac{\beta}{2\xi'_0}\left[\frac{C_2(C_L + C_C)}{C_C^2}\right] \times \left(\xi'_0\tan(\mathrm{PM}) + \sqrt{1 + \xi'^2_0\tan^2(\mathrm{PM})}\right)g_{mi}. \tag{42}$$

The current of the input devices can then be obtained from (12). The time-constant coefficients are reported in Table V for different small-signal settling errors to facilitate using the methodology for the case of PM $= 65^o$ and $\xi'_0 = 0.7$.

Circuit-level simulations were performed in a standard 0.18μm CMOS technology. An OTA in the form of Fig. 7(a) was embedded in the unity-gain flip-around SHA illustrated in Fig. 2(b). During the sampling phase (φ_1), sampling capacitors (C_S) are charged by the input differential voltage.

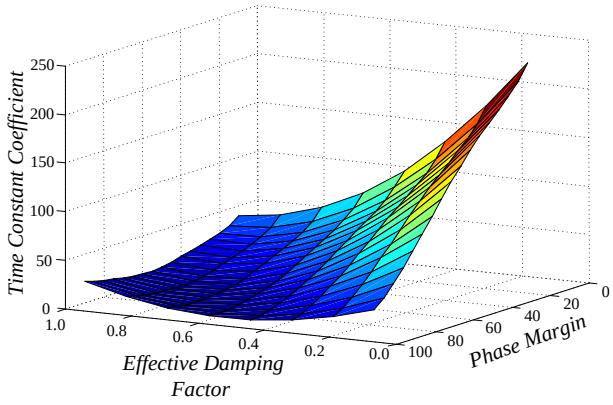

Fig. 8 Time-constant coefficient vs. PM and ξ'_0 for the small-signal settling error of 0.05%.

Table V. Time-constant coefficient vs. e_{SS} for PM and ξ'_0 of 65° and 0.7.

Small-Signal Error (e_{SS})	**Time-Constant Coefficient (n)**
0.005 %	7.3804
0.01 %	6.2825
0.025 %	6.0279
0.05 %	4.8382
0.1 %	4.7171
0.25 %	4.45
0.5 %	4.0659
1 %	2.943

The output voltage then settles down to the sampled voltage when the capacitors are connected to the output in the holding phase (φ_2). The compensation capacitors were chosen to 3pF following the noise constraints. The required dynamic range also enforces choosing a peak-to-peak output voltage swing of $1.5V_{p\text{-}p}$. The overdrive voltage of the input transistors is chosen to be 0.3 V. Regarding the needed accuracy for the 50MS/s sampling frequency, the required small-signal settling error was calculated to be smaller than 0.05% at 10ns settling time. The phase margin and the effective damping factor were chosen as 65° and 0.7 respectively. From Table V, the required time-constant coefficient (n) was obtained as 4.83. Using (14), the transconductance of input

devices was obtained as 2.95 mA/V. The transconductance of the cascode and load transistors were calculated from (41) and (42) as 13.64 mA/V and 6.18 mA/V, respectively. The nominal settling time illustrated in Table VI is for a full-swing differential voltage and 0.1% total settling error (corresponding to 0.05% small-signal settling error). The SHA settling behavior and the settling time match very well with the calculated results.

Table VI. Comparison of simulated and calculated results

Parameter	Simulation	Calculation
Feedback Factor	0.99	1.00
Peak-to-peak Swing (Vp-p)	1.5	1.5
DC Gain (dB)	67	66
Effective Damping Factor	0.648	0.7
Phase margin (deg.)	64.62	65
Nominal GBW (MHz)	147.44	156
Total Settling Error (%)	0.1	
Nominal Settling Time (ns)	9.676	10

IV. Three-Stage OTAs

Frequency compensation is mandatory to stabilize closed-loop three-stage OTAs similar to the case of two-stage OTAs. Nested-Miller compensation (NMC) is the original solution proposed, while several other solutions are subsequently discussed in the literature [13, 30, 38, 42]. Fig. 9 (a) depicts the circuit diagram of an NMC three-stage OTA, which is composed of a differential 1st stage, a non-inverting 2nd stage, and an inverting 3rd stage with equivalent transconductances g_{mi}, g_{m2} and g_{mL}, respectively. The output resistors and capacitors are also modeled by R_i and C_i, where $i = 1, 2, 3$. The load capacitor is shown by C_L, whose value is normally much higher than C_3. For frequency compensation purposes, NMC utilizes two negative capacitive feedbacks according to the circuit diagram in Fig. 9(a), one through C_{C1} for pole-splitting and the other through C_{C2} for damping factor control of non-dominant poles. Fig. 9(b) shows a transistor-level implementation of the NMC OTA in CMOS technology, where the transconductance stages are realized using MOS devices. The poles of the closed-loop OTA can be placed according to the arrangement of the poles of a third-order Butterworth filter with a maximally flat band. This will not, however, guarantee the minimum power consumption for the applications based on settling time.

The original transfer function of the NMC diagram in Fig. 9 (a) is rather complicated. Under the assumptions that:

1. The load and compensation capacitors (C_{C1}, C_{C2} and C_L) are much larger than the capacitors in the output of different stages (C_1, C_2 and C_3);
2. The DC gain of the first, second and third stage is much higher larger than unity;
3. g_{mL} is significantly larger than $g_{mi}$and g_{m2};

The methodology described in [42] can be applied to evaluate the open-loop transfer function as:

$$A_V(s) = \frac{A_0}{(1 + s/|p_{-3dB}|)[1 + (2\xi_0/\omega_{n0})s + s^2/\omega_{n0}^2]} \quad (43)$$

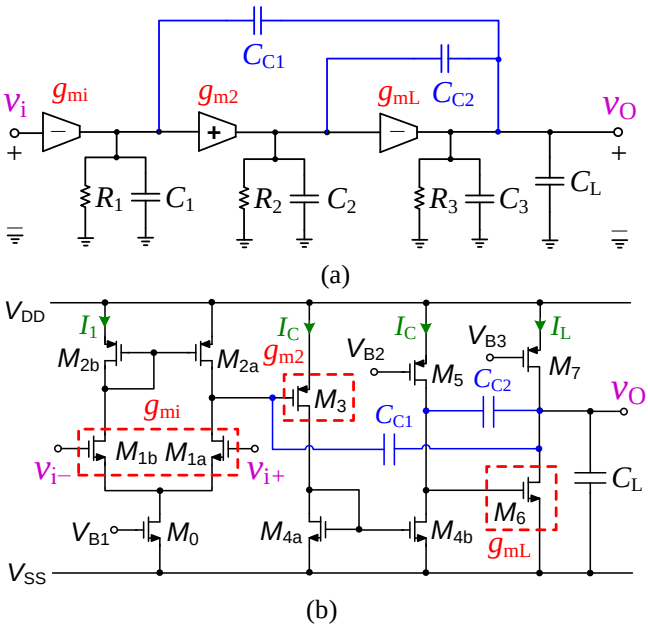

Fig. 9 A three-stage nested-Miller-compensated OTA; (a) small-signal equivalent circuit, (b)Transistor-level scheme.

where $A_0 \approx g_{mi}g_{m2}g_{mL}R_1R_2R_3$ is the DC gain, and

$$p_{-3dB} \approx \frac{-1}{g_{m2}g_{mL}R_1R_2R_3C_C}, \quad (44)$$

is the dominant pole frequency. The GBW is given by:

$$GBW = A_0 \times |p_{-3dB}| \approx \frac{g_{mi}}{C_{C1}}. \quad (45)$$

The damping factor ξ_0 and natural frequency ω_{n0} are, respectively, measured as:

$$\omega_{n0} = \sqrt{\frac{g_{mC}g_{mL}}{C_{C2}C_L}}, \quad (46)$$

$$\xi_0 = \frac{1}{2}\sqrt{\frac{g_{mL}}{g_{mC}} \cdot \frac{C_{C2}}{C_L}}. \quad (47)$$

From (47), the role of C_{C2} for stabilizing the OTA is evident. Despite C_{C1} dominates the first stage output pole and moves the rest to higher frequencies, the damping factor of the non-dominant pole might become very small in the absence of C_{C2}. A large peaking then appears in the frequency response, causing ringing in the transient response of closed-loop OTA.

We refer to the PM definition, we can write:

$$\tan(PM) = \frac{1 - (\beta GBW/\omega_{n0})^2}{2\xi'_0(\beta GBW/\omega_{n0})}. \quad (48)$$

After rearranging, GBW can be expressed in terms of PM as:

$$GBW = \frac{1}{\beta}\frac{\omega_{n0}}{\xi_0\tan(PM) + \sqrt{1 + \xi_0^2\tan^2(PM)}}. \quad (49)$$

For unchanged β, ω_{n0}, and PM, a higher GBW will be obtained if the damping factor in (49) is lowered. This may not be, however, helpful for improving the settling time since the relative distance between ω_{n0} and GBW subsequently reduces. This will finally generate an undesired peaking in the

frequency spectrum and degrades the stability. Hence, keeping $\xi_0 \tan(\mathrm{PM})$ beyond a threshold value is essential for stability and a lower ξ_0 should be compensated by a higher PM.

Similar analysis as the case of single- and two-stage OTAs can be performed to extract an expression between GBW and t_S. While the result is similar to (14), it is essential to determine the modified formula of n shown by (9). Similar to the case of two-stage cascode-compensated OTA, the equivalent definition is a non-linear function of small-signal settling error, phase margin, and damping factor:

$$n = \frac{t_{SS}}{1/(\beta \mathrm{GBW})} = f(e_{SS}, \xi_0, \mathrm{PM}). \qquad (50)$$

Given the PM,ξ_0 and e_{SS}, a computational program numerically solved n using the expressions from (38) to (40). Table IV represents the results for $e_{SS} = 0.05$ % when the effective damping factor is replaced by ξ_0. The values for PM $\approx 90^o$ approach the same values as (9) for the case of single-stage OTAs. The 3D surface in Fig. 8 is plotted based on the numerical values in Table IV and depicts the typical expression between n, PM and ξ_0 for a particular e_{SS}. Greater PM and $\xi_0$values increase the robustness of n against the variations due to local mismatches. This is, however, at the cost of more power consumption necessary to move non-dominant poles to higher frequencies. Table VII reports n for different values of e_{SS} when PM $= 70^o$ and $\xi_0 = 0.6$, which can be considered as a reference to realize an NMC OTA with proper stability margins.

A settling-based design methodology can now be presented based on settling time. In case the methodology is used as a starting point for hand analysis, the time-constant coefficient along with the damping factor and phase margin should be evaluated at first. The results are shown in Table VII for the case of PM $= 70^o$ and $\xi_0 = 0.6$ would be more convenient in this case. Combining (14) with (45), the required $g_{mi}$for a prescribed t_S would be:

$$g_{mi} = C_{C1}\left(\frac{n}{\beta} + \frac{V_{Swing}}{V_{eff,i}}\right)\frac{1}{t_S}, \qquad (51)$$

where C_{C1} can be sized according to the target thermal input-referred noise factor [30]. The equivalent transconductances of the second and the third stages in Fig. 9 can then be related to g_{mi} and subsequently to t_S. Substituting (46) and (47) into (49), we get:

$$g_{m2} = \frac{\beta C_{C2}}{2\xi_0 C_{C1}}\left(\xi_0 \tan(\mathrm{PM}) + \sqrt{1 + \xi_0^2 \tan^2 \mathrm{PM}}\right) g_{mi}, \qquad (52)$$

$$g_{mL} = 2\beta\xi_0 \frac{C_L}{C_{C1}}\left(\xi_0 \tan(\mathrm{PM}) + \sqrt{1 + \xi_0^2 \tan^2(\mathrm{PM})}\right) g_{mi}. \qquad (53)$$

The current of the input devices can be evaluated from (12), which should be later modified in the presence of the second-order effects included in the models.

The above methodology is validated through simulations in a standard 0.35μm CMOS technology. The three-stage OTA shown in Fig. 9(b) is implemented in the form of the unity-gain voltage buffer in Fig. 2(a).

Table VII. Time-constant coefficient vs.e_{SS} for PM and ξ_0 equal to 70^o and 0.6.

Small-Signal Error (e_{SS})	**Time-Constant Coefficient(n)**
0.005 %	6.4792
0.01 %	6.3192
0.025 %	6.0298
0.05 %	5.6927
0.1 %	4.2253
0.25 %	3.9973
0.5 %	3.7963
1.0 %	3.5375

Operating at 3 V supply voltage, the OTA drives a 100pF capacitive load. According to the speed/accuracy requirement, the small-signal settling error is calculated to be smaller than 0.1% for 1μs settling time. The dynamic range requirement sets the amplifiers' output voltage swing to $0.5V_{p\text{-}p}$. The overdrive voltage of all transistors is also assigned as 100 mV. The design flow was applied for PM $= 70^o$ and $\xi_0 = 0.6$. By choosing $e_{SS} = 0.1\%$, the corresponding time-constant coefficient would be 4.225. Depending on the noise and area constraints, the compensation capacitors are also considered as $C_{C1} = 30$ pF and $C_{C2} = 10$ pF. From (51), the required transconductance for the input devices was obtained as $g_{mi} = 277\ \mu A/V^2$. g_{m2} and g_{mL} were also derived from (52) and (53) as $275\ \mu A/V^2$ and $3967\ \mu A/V^2$, respectively. From (12), I_1 was calculated as 15μA. Table VIII compares the 0.1% settling time with the results obtained from hand analysis.

Table VIII. Simulation results the unity-gain OTA.

Parameter	**This work**
Load Capacitor (pF)	100
Power (μW)	700
DC Gain (dB)	108
C_{C1},C_{C2} (pF)	30,10
Gain Bandwidth (MHz)	1.40
SR+ / SR– (V/ μs)	1.16 / 1.24
Damping Factor	0.62
Phase margin (deg.)	71
Desired 0.1% t_S (μs) +0.1% t_S (μs) –0.1%t_S (μs)	1.00 0.94 0.93

V. CONCLUSIONS

Single-, two- and three-stage CMOS OTAs were analyzed based on settling time. The OTA gain-bandwidth was related to settling time by including both small- and large-signal parts of the settling response, giving the possibility to determine the OTA circuit specifications based on a settling-based design methodology. Design examples were provided to clarify the implementation details based on settling time.

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