A Review of CMOS Current References

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Abstract— A current reference is able to provide a precise and accurate current for other circuits inside the chip. This type of electronic circuit is employed as a building block in numerous analog and mixed-signal circuits. Moreover, it is a fundamental component of current-mode circuits. This work discusses the basic and essential concepts of designing CMOS integrated current references. A review of conventional topologies is presented, including current mirrors and current references. The temperature dependence is discussed, along with PTAT and CTAT topologies, and also some low-power and low-voltage implementations.

***Index Terms*— Current reference, CMOS, Review, Survey**

I. INTRODUCTION

An integrated current reference circuit is capable of providing a precise and accurate current (I_{REF}) for other circuits inside the chip. This type of circuit is a fundamental building block in almost every analog and mixed-signal circuit. For instance, the generated current reference can simply be used to bias an operational amplifier or employed in a current-controlled oscillator to compensate for its temperature coefficient [1]. Moreover, current references are also mandatory for current-mode circuits, which are important for several applications such as telecommunication systems, instrumentation, analog signal processing, and microprocessors [2]. In current mode circuits, the information is represented by a branch current rather than the nodal voltage. The main desired features for a current reference circuit are explained below.

The first important characteristic of a current reference is its robustness against the effects of the fabrication process. Ideally, the value of I_{REF} is the same for every instance of the fabricated reference circuit. However, in reality, we expect different values of I_{REF} for each instance of the fabricated circuit. These variations result from the IC manufacturing process that involves complex physical and chemical interactions. As a result, the value of I_{REF} presents finite variations centered around the targeted value. These effects can be simplified categorized into: (i) intra-die and (ii) inter-die applications [3]. The first one refers to variations in different instances inside a specific chip present, while the second relates to variations when considering different fabricated chips. To estimate these variations in the performance on the designed voltage reference, designers usually use Monte Carlo analysis and Process Corner simulations. The variability of I_{REF} caused by the impact of the fabrication process is usually expressed in percentages, and common values vary from 1 to 20% [4].

The second characteristic that almost all current references must present is a low dependency of I_{REF} on the supply voltage (V_{DD}). This feature is required because the supply voltage varies for several reasons in real electronic applications. And it is not expected that those variations affect the value of I_{REF}. For example, microprocessors usually employ a dynamic voltage and frequency scaling technique (DVFS) [5]. The supply voltage, in this case, is decreased to save battery energy when high performance is not demanded. Another situation where the supply voltage is also not fixed and well-defined is those applications whose supply voltages are extracted from the energy available in the environment. Since the amount of energy in the environment may not be constant, the amount of extracted power and the V_{DD} level is also variable over time. For instance, using a piezo-cantilever for IoT applications makes it possible to extract 1 to 500 nW according to the available vibrational energy [6]. The variation of I_{REF} as a function of supply voltage is usually expressed in percentage for each 1 volt of variation in the supply line (i.e., %/V), which is called line sensitivity (LS). Values of LS between 0.1 to 8 are found in the literature [4]. Furthermore, an important specification is also the minimum supply voltage of operation (V_{DDMIN}). This parameter limits the employability of a given current reference architecture when low voltage performance is required.

The third common feature is the low dependency of I_{REF} on the operation temperature. This specification strongly depends on the temperature range of the application. In a simplified way, one can list three standard ranges of temperature: (i) commercial (0° to 70 °C), (ii) industrial (-40° to 85 C°), and (iii) Military (-55° to 125° C). Note, however, that several applications just need to operate at specific temperature conditions. For instance, implantable biomedical integrated circuits operate at 36° to 37 °C, which is the body temperature, and therefore, there is no need for a low dependency of I_{REF} on temperature. The temperature coefficient (TC) is usually calculated by equation (1), given in ppm/°C. Common TC values reported in the literature vary between 1.5 to 700 ppm/°C [4].

$$TC = \frac{1}{I_{REF}} \cdot \frac{(I_{REF\_max} - I_{REF\_min})}{\Delta T} \cdot 10^6 \quad (1)$$

Apart from the above main specifications, the design of integrated current references also faces the traditional trade-off in analog circuits, like silicon area and power dissipation. If low power operation is needed, it is frequently necessary to increase the silicon area. It is often valid for current reference topologies that use integrated resistors. Therefore, the absence or presence of integrated resistors in the current reference architecture is also an important feature to evaluate the best current reference topology for the application. Additionally, note that integrated resistors in a circuit topology may make it more susceptible to the mentioned

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impact of the fabrication process. The accuracy of the resistance of integrated resistors varies from 10% to 40% [4].

This work is organized as follows. Section II starts with a discussion of current mirror topologies. This type of circuit is a building block in the design of current references, and therefore, its understanding is needed. Section III presents basic and widely used current reference architectures and their limitations. The temperature effects on I_{REF} are presented in Section IV. Section V discusses a few examples of temperature compensated current references. A brief discussion of some low voltage and low power current reference architectures is given in Section VI. Finally, Section VII presents the conclusions.

II. CURRENT MIRROR

Current mirrors are circuits that create a scaled copy of a reference current. This section presents a survey of the most common current mirror architectures.

A. Simple Current Mirror

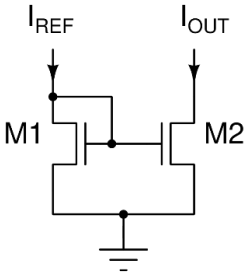

Fig. 1 Simple current mirror. M_1 and M_2 are matched.

The simplest and most common current mirror is shown in Fig. 1. The output current, I_{OUT}, is a scaled replica of the reference current, I_{REF}, as shown by the next equations:

$$I_{REF} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2(1 + \lambda V_{DS1}) \quad (2)$$

$$I_{OUT} = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH})^2(1 + \lambda V_{DS2}) \quad (3)$$

Where λ is the channel length modulation parameter, μ represents the mobility of electrons to the N channel transistor (holes to P channel transistor), and C_{ox} corresponds to oxide capacitance per unit area. Combining the equations 2 and 3, equation (4) can be written:

$$I_{OUT} = I_{REF}\frac{(W/L)_2}{(W/L)_1}(1 + \lambda V_{Out}) \quad (4)$$

By design, we can choose the same length of the channel to devices M_1 and M_2, so the equation 4 is therefore described by:

$$I_{OUT} = I_{REF}\frac{(W)_2}{(W)_1}(1 + \lambda V_{Out}) \quad (5)$$

If $\lambda = 0$, the output current, I_{OUT}, is a scaled replica of I_{REF}, by the factor W_2/W_1. Considering the effect of the channel length modulation parameter, an precise copy requires a long channel lengh and therefore more silicon area. This architecture has a low relative output resistance. On the other hand, this topology has a superior output dynamic range when compared with others [7].

B. Wilson current mirror

The Wilson current mirror structure, shown in Fig. 2, is an alternative to improve the low output impedance of the simple current mirror. The gate-to-source voltage of M_1 and M_2 are equal. The device M_3 is added to increase the output impedance [7]. Note that in Fig. 2, the drain-to-source voltage of M_1 is given by:

$$V_{DS1} = V_{GS3} + V_{DS2} \quad (6)$$

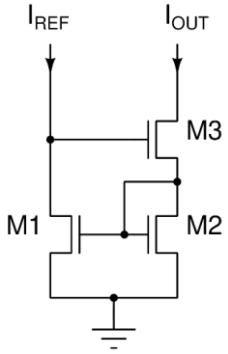

Fig. 2 Wilson current mirror.

Therefore, I_{OUT} is given by Equation (7):

$$I_{OUT} = I_{Ref}\frac{W_2}{W_1}\frac{1 + \lambda V_{DS2}}{1 + \lambda(V_{DS1} + V_{GS3})} \quad (7)$$

The output resistance is represented by Equation (8) [7], and the minimum output voltage is given by Equation (9):

$$r_{out} \simeq r_{ds3}\frac{g_{m3}}{g_{m2}}g_{m1}r_{ds1} \quad (8)$$

$$V_{OUT,min} = V_{sat3} + V_{GS1} \quad (9)$$

C. Improved Wilson current mirror

The current mismatch in the Wilson current mirror is reduced if the circuit topology is modified as shown in Fig. 3 [7]. The drain-to-source voltage of M_1 in this case is:

$$V_{DS1} = V_{GS3} + V_{DS2} - V_{GS4} \quad (10)$$

The condition to have an equal drain-to-source voltage of M_1 and M_2 is to have an equal gate-to-source voltage of M_3 and M_4. It is achievable if M_3 and M_4 are designed to be matched. Thus, the same size of transistors M_3 and M_4 is essential to make layout matching easier.

The relationship between I_{out} and I_{REF} is described by Equation (11). Moreover, the Equations for the output resistance and minimum output voltage are equal to that Wilson current mirror.

$$I_{Out} = I_{Ref}\left(\frac{W_2}{W_1}\right)\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \quad (11)$$

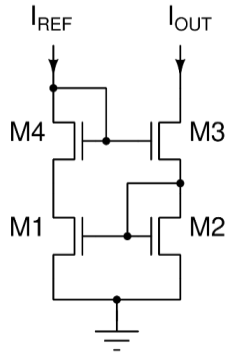

Fig. 3 Improve Wilson current mirror.

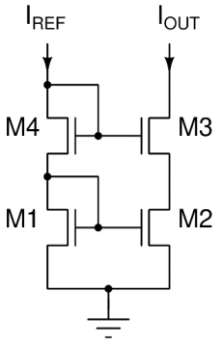

Fig. 4 Cascode current mirror

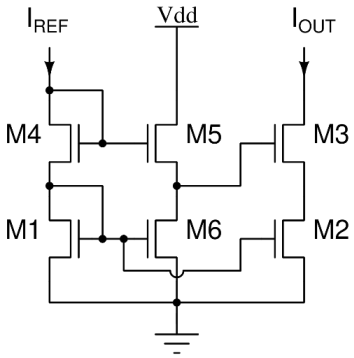

Fig. 5 Modified cascode current mirror.

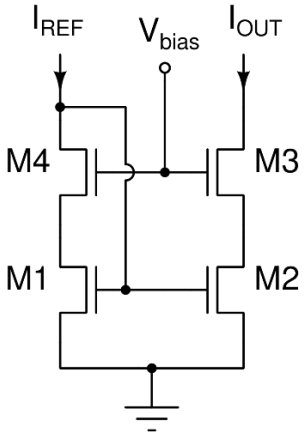

Fig. 6 High compliance current mirror.

D. Cascode current mirror

Another option to increase the output impedance is shown in Fig 4. The output stage of cascode topology is built with devices M_2 and M_3, which are biased by the diode-connected M_1 and M_4 transistors. The output resistance of this circuit is given by (12) [8], which is the product of the intrinsic gain of device M_3 ($g_{m3}r_{ds3}$) by the drain resistance of transistor M_2 (r_{ds2}). The output current as a function of I_{REF} is also given by (11).

$$r_{out} \approx g_{m3} r_{ds3} r_{ds2} \tag{12}$$

The minimum output voltage required for operation is expressed by (13) [7, 8].

$$V_{out,min} = 2V_{sat} + V_{TH} \tag{13}$$

E. Modified cascode current mirror

The Wilson, The improved Wilson, and the cascode current mirror architectures show an increase in the output resistance, but the payoff is a reduction in the output dynamic range. An alternative that allows an increase in the dynamic range is shown in fig. 5. The minimum output voltage for this configuration is given by [7]:

$$V_{out,min} = 2V_{sat} \tag{14}$$

F. High compliance current mirror

The high compliance current mirror, also called a wide-swign current mirror, is shown in Fig. 6. It has a minimum output voltage of two overdrive voltages if the value of V_{bias} is suitable to keep the saturation of transistors M_3 and M_4. The saturation of device M_1 is guaranteed if:

$$V_{bias} - V_{GS4} > V_{sat1} \tag{15}$$

The transistor M_4 is saturated if:

$$V_{bias} - V_{DS1} - V_{TH4} < V_{GS1} - V_{DS1} \tag{16}$$

Substituting the gate-to-source voltage $V_{GSx} = V_{Sat,x} + V_{TH,x}$ (where the sub-index "x" is 1 or 4) in the above equations, the following inequalities are obtained: $V_{bias} > 2V_{Sat} + V_{TH,4}$ and $V_{bias} < V_{Sat,1} + 2V_{TH}$. So, the value of V_{bias} must be kept between two threshold voltages plus one saturation voltage and two saturation voltages plus one threshold.

Equation (11) describes the behavior between I_{out} and I_{ref}. Similar to the modified cascode current mirror, this topology has two saturation voltages as minimum output voltage.

G. Enhanced output-impedance current mirror

Using feedback is possible to increase the output resistance of a current mirror [7].

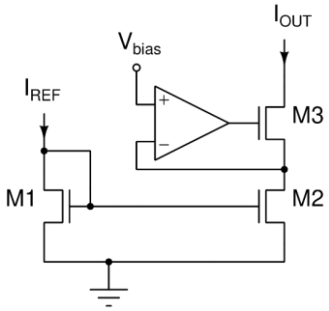

Fig. 7 Enhanced output-impedance current mirror.

Fig. 7 illustrates the use of feedback. The gate voltage of transistor M_3 is the product of the amplifier's gain (A) by the difference between a bias voltage (V_{bias}) and the drain voltage of device M_2 (V_{DS2}).

To obtain electrical matching between the reference current and the output current, the V_{bias} voltage must be equal to the V_{GS1} voltage of transistor M_1, which is diode-connected.

The output resistance of this circuit topology is approximately [7]:

$$r_{out} \simeq A r_{ds2} g_{m3} r_{ds3} \tag{17}$$

The minimum output voltage is given by (18), and I_{OUT} is also given by (11).

$$V_{out,min} = V_{bias} + V_{sat3} \tag{18}$$

Table 1 summarizes the main specifications of the presented current mirrors. Note that the lowest $V_{out,\ min}$ is archived by simple current mirror topology, and the largest output resistance is achieved by the enhanced output-impedance current mirror.

III. CURRENT REFERENCES

The current mirror architecture reviewed in the last section can be employed as a building block to design current reference circuits. This section presents three widely used and traditional ways to design a simple current reference.

A. Simple Current Reference

The simplest way to implement a current reference I_{REF} is shown in Fig. 8. Note that the ideal current source of Figure 1 (i.e., the simple current mirror) was replaced by a resistor.

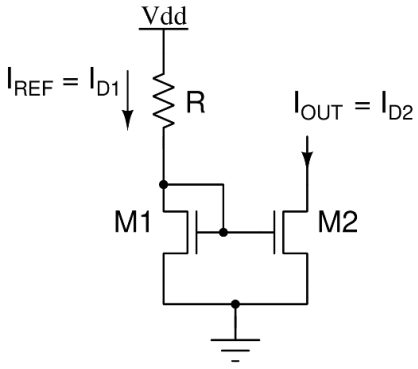

Fig. 8 Simple current reference.

Therefore, the current reference I_{REF} is produced by the difference between the power supply, V_{DD}, and gate-source voltage of transistor M_1, V_{GS1}, divided by resistor R. Therefore, I_{REF} can be modeled as (19):

$$I_{REF} = \frac{V_{DD} - V_{GS1}}{R} \tag{19}$$

In Equation 19, I_{REF} is directly and inversely proportional to the supply voltage and the integrated resistor, respectively. Therefore, the accuracy of the current reference will be significantly affected by the resistor's tolerance and variations (DC or AC) in the supply voltage.

B. Widlar Current Reference

Another method to generate a current reference is illustrated in Fig. 9.

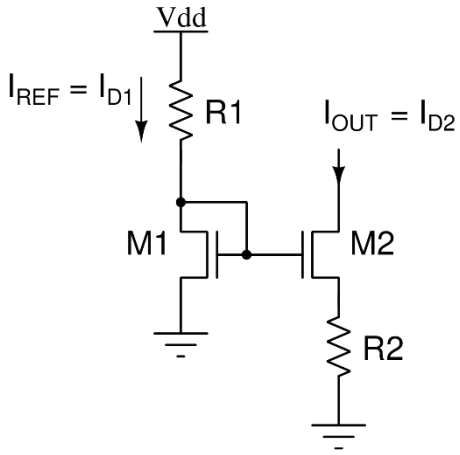

Fig. 9 Widlar current reference.

Note that this circuit is equal to the last case, except by the resistor R_2, which is connected to the source of device M_2 for limiting its drain current I_{D2}. The gate-source voltage value of transistor M_1 is $V_{GS1} = V_{GS2}+I_{OUT}*R2$. Therefore, the reference current I_{REF} is given by Equation (20):

$$I_{REF} = \frac{V_{DD} - V_{GS2} - I_{OUT} R_2}{R_1} \tag{20}$$

C. V_{REF}-based current reference

Another current reference architecture that is widely presented in the literature [8], is the circuit shown in Fig. 10. Assuming an ideal operational amplifier, Op-Amp, the reference current is represented by (21):

Table I. A performance comparison between current mirror topologies.

Architecture	N° of Transistor	$V_{out,min}$	r_{out}
Simple	2	$V_{sat2} = V_{GS2} - V_{TH2}$	r_{ds2}
Wilson	3	$V_{sat3} + V_{GS1}$	$r_{out} \simeq r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} r_{ds1}$
I. Wilson	4	$V_{sat3} + V_{GS1}$	$r_{out} \simeq r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} r_{ds1}$
Cascode	4	$2V_{sat} + V_{TH}$	$r_{out} \simeq g_{m3} r_{ds3} r_{ds2}$
M. Cascode	6	$2V_{sat}$	$r_{out} \simeq g_{m3} r_{ds3} r_{ds2}$
H. Compliance	4	$2V_{sat}$	$r_{out} \simeq g_{m3} r_{ds3} r_{ds2}$
Enhanced	3 plus 1 OpAmp	$V_{bias} + V_{sat3}$	$r_{out} \simeq A g_{m3} r_{ds3} r_{ds2}$

$$I_{REF} = \frac{V_{REF}}{R} \quad (21)$$

To reduce the dependence of the current mirror performance on variations in the IC process, supply voltage, and temperature, the voltage V_{REF} should be generated by a voltage reference circuit and a highly precise and accurate integrated resistor. Alternatively, resistor "R" can be carefully chosen if placed outside the chip, at the cost of lower integration.

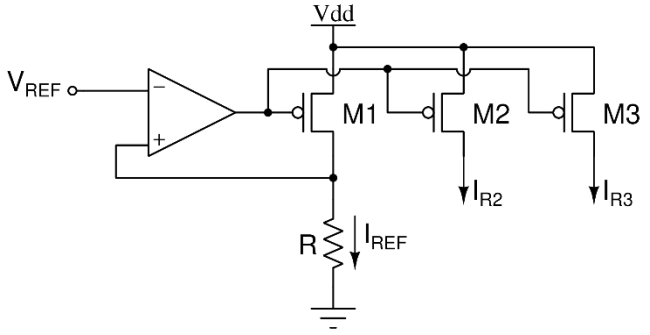

Fig. 10 Current reference using Op.-Amp.

The above three methods to generate a current reference are simple and useful. However, the first two circuits suffer from supply variations or resistor tolerance, which may make them an invalid option for products that must rely on accurate current references. Moreover, the output provided by these two circuits also varies with temperature, which is a limiting factor for its employment. Finally, although the third architecture is robust against V_{DD} and temperature variations, it depends directly on a voltage reference circuit.

IV. TEMPERATURE DEPENDENCY

As is widely known, several electric parameters used in electronic circuits depend on the operating temperature, such as the resistance of resistors. Typically, but not always, their resistance increases linearly with an intense increase in the temperature. Not unlike resistors, other devices such as bipolar junction transistors, BJTs, MOS transistors, and diodes also suffer variations in their operation caused by temperature variations. In literature, we usually use the following terms to represent the dependency regarding the temperature. When a voltage or a current increases linearly with the temperature, it is called Proportional to Absolute Temperature (PTAT) [9-12]. When it decreases linearly with the temperature, it is called Complementary Proportional to the Absolute temperature (CTAT). In this chapter, some PTAT and CTAT current reference topologies will be discussed.

A. PTAT Current Reference

The most traditional method to generate a PTAT current reference is using the V_{BE} difference (ΔV_{BE}) of two transistors with different areas or collector currents. Fig. 8 shows two circuit topologies for the PTAT current reference used in the literature [11].

The first topology, Fig. 11 (a) uses bipolar junction transistors to generate the PTAT component [13]. The voltage V_{BE} of a bipolar transistor BJT is given by Equation (22):

$$V_{BE} = U_T \cdot ln\left(\frac{I_0}{I_S}\right) \quad (22)$$

where I_0 is the current passing through the transistor, I_S the saturation current and U_T is the thermal voltage, defined as KT/q, where K is the Boltzmann constant and q is the charge of an electron. As a consequence, Equation (23) described the current across resistor R3. The emitter area of Q1 is assumed to be N times larger than Q2.

$$I_{R3} = \frac{V_{BEQ1} - V_{BEQ2}}{R_3} \quad (23)$$

Substituting Equation (22) in (23), Equation (24) is obtained:

$$I_{R3} = \frac{U_T \cdot ln\left(\frac{NI_0}{I_S}\right) - U_T \cdot ln\left(\frac{I_0}{I_S}\right)}{R_3} \quad (24)$$

Equation (24) can be simplified as (25). Note that current I_{R3} is directly proportional to the temperature, as U_T varies positively with increasing temperature.

$$I_{R3} = \frac{U_T}{R_3} \cdot ln(N) \quad (25)$$

The topology in Fig. 11 (b) generates a similar PTAT current by only using MOS transistors. N1 and N2 transistors should operate in a weak inversion region [14]. The weak inversion current flowing through the transistor terminals is given by Equation (26):

$$I_{DS} = I_0 \cdot exp\left(\frac{V_{GS}-V_{TH}}{n \cdot U_T}\right)\left(1 - exp\left(-\frac{V_{DS}}{U_T}\right)\right) \quad (26)$$

Here, I_0 is given by Equation (27), where n *is* the slope factor in weak inversion. Considering the voltage V_{DS} greater than or equal to three times the size of the thermal voltage U_T, the second portion of the multiplication of Equation (26) can be ignored, thus resulting in (27):

$$I_0 = \mu_0 \cdot C_{OX} \cdot \frac{W}{L}(n-1)U_T^2 \quad (27)$$

Fig. 8 (b) illustrates a topology consisting of a PMOS current mirror, an NMOS degenerate current mirror, and a resistor. For correct functioning, transistors N_1 and N_2 must operate in the inversion region. The PTAT voltage depends on the current I_1, which in turn depends on the resistor R_1 and the gate-source voltages V_{GSN1} and V_{GSN2}, given by (28):

$$I_1 = \frac{V_{GSN1} - V_{GSN2}}{R_1} \quad (28)$$

Isolating Equation (26) as a function of V_{GS}, and substituting it in equation (28), obtains (29), where S is the aspect ratio of the transistor.

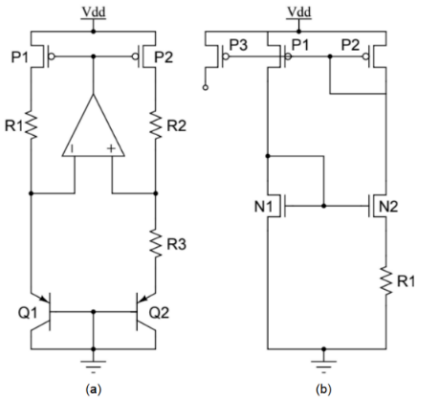

Fig.11 PTAT current reference

$$I_1 = \frac{1}{R_1} n \cdot U_T \cdot ln\left(\frac{S_{N2}}{S_{N1}}\right) \quad (29)$$

One way to reduce the channel length modulation effects, and, as a consequence, improve the line regulation of the circuit of Fig. 11 (b), is utilizing the inclusion of an OpAmp in the circuit. In this case, the differential inputs are connected at the drains of P_1 and P_2, and output at the gates of the same transistors.

B. CTAT Current Reference

The most traditional way to generate a CTAT voltage is using a BJT transistor, because its base-emitter voltage, V_{BE}, decreases approximately linearly with the increase in temperature. An alternative method is employing the V_{GS} voltage of the MOS transistor, which in weak inversion, is defined by Equations (30) and (31):

$$|V_{GS}| \approx |V_{GS}|(T_0) + K_G\left[\left(\frac{T}{T_0}\right) - 1\right] \quad (30)$$

$$K_G \cong K_{T1} + |V_{GS}|(T_0) - |V_{TH}|(T_0) - V_{OFF} \quad (31)$$

where the variables K_{T1} and V_{OFF} are BSIM4V4 parameters (MOS transistor model family) for the thermal coefficient (TC) of V_{TH} and the displacement voltage in the subthreshold region, considering the very large length (L) and width (W), respectively [15]:. (TC) of V_{TH} and the displacement voltage in the subthreshold region, considering the very large length (L) and width (W), respectively [15]. With typical values of K_{T1}, V_{OFF}, $V_{GS}(T_0)$, and $V_{TH}(T_0)$, the constant K_G becomes negative, and the gate-source voltage is a CTAT voltage.

In [16], a different way to generate a CTAT voltage is presented. It is used two MOS transistors with different channel lengths with different threshold voltages, V_{TH}, which in turn also has a CTAT behavior.

Fig. 12 shows two circuit topologies able to generate a CTAT current. The first one, shown in (a), uses the V_{GS}, while the second one in (b), uses a bipolar device.

Considering the circuit in Fig 12, (a), the voltage across resistor R_1 is the V_{GS} voltage of transistor M_4, which makes the current I_{R1} to be given by Equation (32) [15]:

$$I_{R1} = \frac{V_{GSM4}}{R_1} \quad (32)$$

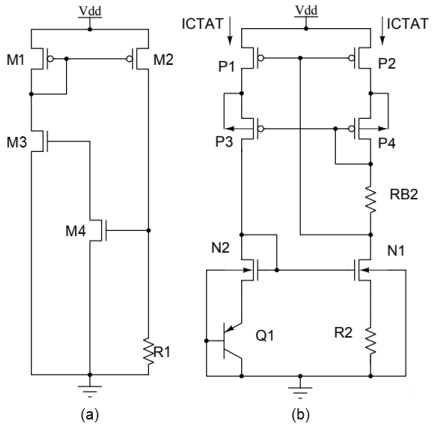

Fig.12 CTAT Topology.

The circuit topology of Fig. 12 (a) is very interesting for applications that require low silicon area occupation where the silicon area can be a problem.

The current generated by the circuit topology of Fig. 12 (b) is given by (33):

$$I_{R2} = \frac{V_{BEQ1}}{R_2} \quad (33)$$

V. TEMPERATURE-COMPENSATED CURRENT REFERENCES

A concept widely used in the various typologies found in the literature would be the sum of an I_{PTAT} current with another I_{CTAT} through a current mirror as shown in Fig. 13:

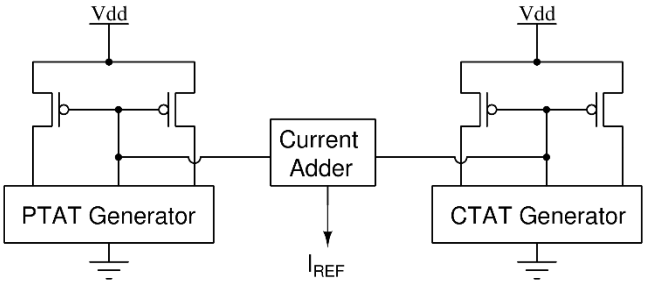

Fig. 13 Generic current reference circuit

One of the first references listed in the literature was proposed by Lee and Park [18]. Its topology uses only MOS transistors and weak inversion resistors. The topology is shown in Fig. 14 and the current I_0 is given by Equation (34):

$$I_0 = \frac{1-\sqrt{m_3}}{1+2\sqrt{m_2}} \sqrt{m_1 m_4}\left(\frac{V_{DD}-3V_{TH3}}{R}\right) \quad (34)$$

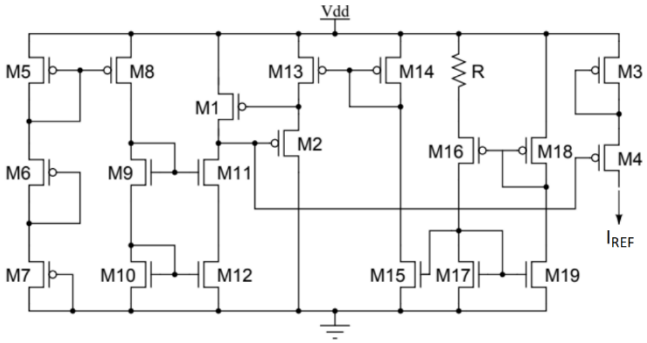

Fig.14 Current reference proposed by [18].

Where the constants m_1, m_2, m_3, and m_4 are parameters that depend on process variables such as dimensioning, mobility of carriers, and oxide capacitance.

Almost ten years after the publication of [18], work [19] was published. The compact circuit topology of [19] is shown in Fig. 15. The circuit has a good PSRR as it is based on a Widlar current source.

The current mirror M_3 - M_4 sets the aspect ratio m between the currents through the two branches, while the Widlar current source M_1 - M_2 - R_1 defines the value of the reference current I. Using Kirchhoff's law in the circuit (a), equation (35) is obtained:

$$\boldsymbol{V_{GS1} + V_{GS5} - V_{GS2} - mR_1 I = 0} \qquad (\mathbf{35})$$

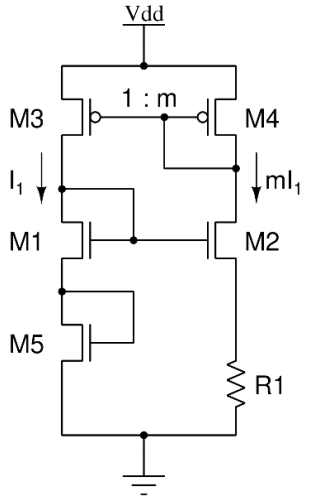

Fig.15 Current reference proposed by [19].

Isolating V_{GS} from the I_D equation in strong inversion, and substituting in (35), Equation (36) is achieved:

$$\sqrt{\frac{\mathbf{I}}{\boldsymbol{\beta}_{\mathbf{n0}}}}\left(\frac{\mathbf{1}}{\sqrt{\mathbf{S_1}}}+\frac{\mathbf{1}}{\sqrt{\mathbf{S_5}}}-\sqrt{\frac{\mathbf{m}}{\mathbf{S_2}}}\right)+\mathbf{V_{TH}}-\mathbf{mR_1 I}=\mathbf{0} \quad (\mathbf{36})$$

Where $\beta_{n0} = \mu_n C_{OX}/2$ and S_i is the m_i transistor aspect ratio. The voltage drop across resistor R_1 is given by the sum of two terms with opposite temperature coefficients. The first one is related to the overdrive voltage of transistors M_1, M_2, and M_5, and has a positive temperature variation, which is due to the negative variation of the μ_n mobility.

The second term is the threshold voltage V_{TH} whose temperature dependency is negative, as mentioned before. A current with a low-temperature coefficient can be obtained if the ratio of these terms is properly chosen. Simply, the value of R1 must be designed accordingly to (37) [19], where $K_{\mu n}$, KV_{TH}, and K_{R1}, represent the temperature coefficient (K) of the electron mobility, threshold voltage, and resistance of R_1.

$$R_1 = \frac{V_{TH}}{mI}\frac{K_{\mu n} + 2K_{VTH}}{K_{\mu n} + 2K_{R1}} \qquad (37)$$

Figure 16 shows a current reference topology [20] that works as illustrated by figure 13. Its temperature compensation depends on a sum of a PTAT current with a CTAT current, and a calibration circuit.

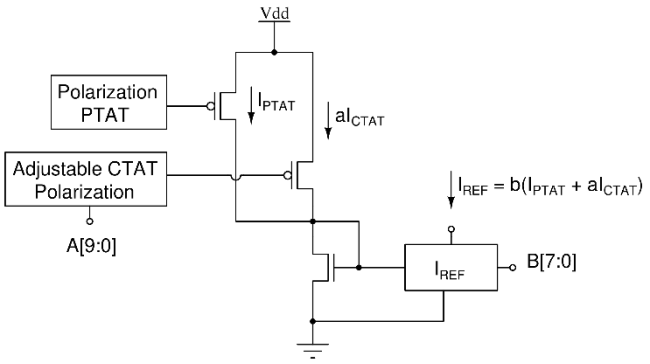

Fig. 16 Current reference proposed by [20].

Another circuit reference that also operates using the balanced summing of oppositive temperature coefficients is shown in figure 17 [17]. The compensated current I_{REF} is given by Equation (40), where α_1 and α_2 are parameters that depend on the aspect ratios of the transistors.

$$I_{REF}(T) = \alpha_1 I_{PTAT}(T) + \alpha_2 I_{CTAT}(T) \qquad (38)$$

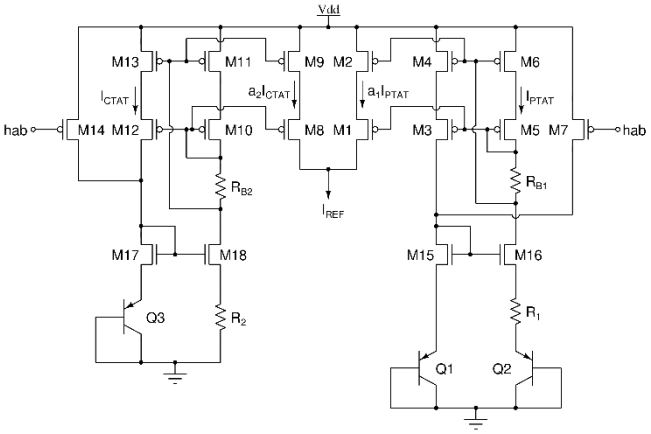

Fig. 17 Compensated I_{REF} proposed by [17].

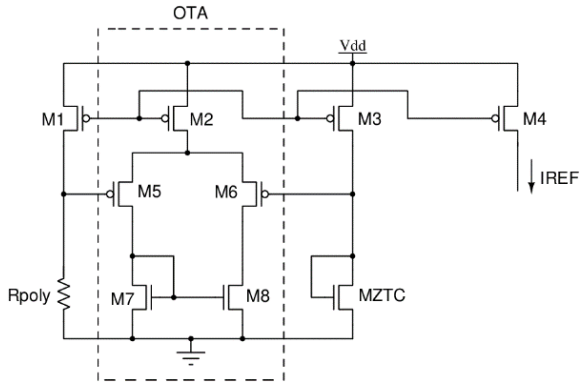

Fig. 18 Compensated I_{REF} proposed by [21].

A different approach to generating a temperature-compensated current reference is proposed by [21]. In this circuit topology, shown in figure 18, the MOSFET (MZTC) that generates I_{REF} is biased at a zero-temperature coefficient (ZTC) condition.

To achieve such biasing, a certain voltage must be applied between the gate and the bulk terminals of the transistor, V_{GB}. The gate voltage and the drain current at these conditions are named V_{GZ} e I_{DZ}, respectively.

The condition causes a mutual cancellation effect of the channel carrier mobility and the threshold voltage dependence on temperature, forcing the drain current to present low dependency on the temperature operation.

VI. LOW VOLTAGE/LOW POWER IMPLEMENTATIONS

The demand for low supply voltage and low power operation is very important for several applications, for instance, portable equipment (e.g., watches and smartphones), implantable devices (e.g., pacemakers and hearing aids), autonomic systems enabled to communicate to the internet-of-things infrastructure, and wireless-sensors (e.g., temperature or pressure sensors). To assure lifelong autonomous operations of some of these devices, their power sub-system often has to harvest energy from natural energy sources such as ambient light, motion, heat, and pressure variations. In some cases, just 500 nW is extracted from the environment in the best operations cases [23]. In the above scenario, low voltage and low power constraints are also needed for current reference topologies.

An example of topology that presents a V_{DDMIN} lower than 1 V is proposed by [12]. The proposed circuit generates simultaneously voltage and current references. The topology is shown in Fig. 19 and I_{REF} is given by Equation 39.

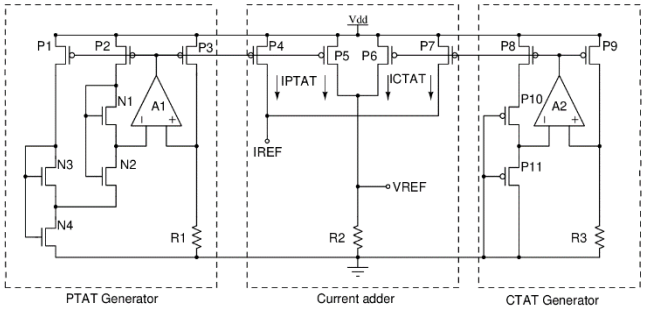

Fig. 19 Compensated I_{REF} proposed by [12].

$$I_{REF} = \frac{V_{DSN2} + V_{DSN4}}{R_1}\left(\frac{S_{P4}}{S_{P3}}\right) + \frac{V_{SGP10} - V_{SDP11}}{R_3}\left(\frac{S_{P7}}{S_{P8}}\right) \quad (39)$$

For applications requiring ultra-low power consumption, the circuit proposed by [22], shown in Fig. 20, is recommended. The output current is generated by a MOSFET operating in weak inversion mode. Accordingly, to equation (27), it is possible to see that the current depends on U_T^2, V_{TH}, and also μo. Since these three parameters depend on the temperature operation, the temperature dependence of I_{REF} can be modeled by an equation with many variables. The proposed topology achieves the temperature compensation by the generation of gate-source voltages with a specific temperature coefficient (i.e., CTAT) that cancels the effects of temperature in the above three parameters. The approach to force a biasing condition that results in a low TC output current is similar to that of [21].

Finally, Table II provides a summary of all discussed works at a glance. As expected, different performance parameters are achieved by each work, which illustrates that the right selection of the current reference topology is mandatory for achieving the product specification.

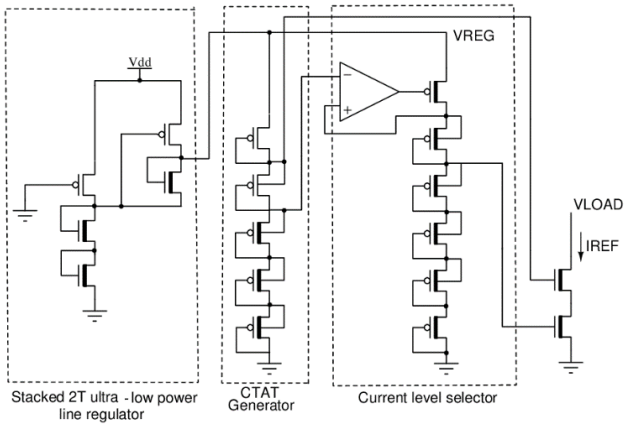

Fig. 20 Compensated I_{REF} proposed by [22].

VII. CONCLUSION

This work presents key concepts of CMOS current reference circuits. Basic and some state-of-art circuits were discussed. In summary, this paper aims to be used as a guideline for students and integrated circuit designers.

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Table II. Summary of current reference topologies discussed in this work.

The basic current references	
[7-8]	Simple Current Reference
[7-8]	Widlar Current Reference
[7-8]	V_{REF} Based Current Reference
I_{PTAT} Current Reference	
[13]	I_{PTAT} current generated by the difference in V_{BE} from the BJT transistor
[14]	I_{PTAT} current generated by the difference in V_{GS} from the MOS transistor
I_{CTAT} Current Reference	
[15]	I_{CTAT} current generated by the V_{GS} of the MOS transistor
[17]	I_{CTAT} current generated by the V_{BE} of the MOS transistor

Temperature-compensated References					
	[17]	**[18]**	**[19]**	**[20]**	**[21]**
I_{REF}(µA)	20	0.25	15.15	16,5	5
Supply voltage	2.6	5	2.5	2	1.4
Supply current (µA)	120	N/D	N/D	N/D	244
TC of I_{REF} (ppm/°C)	62.5	227	130	280	15
Line regulation	N/D	N/D	N/D	N/D	N/D
Area (mm^2)	0.1394	N/D	0,0042	0.0576	0.01
CMOS Process (nm)	350	350	350	350	180
Temperature range (°C)	-40 to 80	0 to 75	-30 to 100	-20 to 100	-40 to 85
Measured samples	26	12	None	None	None

	Sub 1-V supply Temperature Compensated	**Ultra-low-power for battery-less systems**
	[12]	**[22]**
I_{REF}(µA)	1.317	0.02
Supply voltage	0.85	1.2
Supply current (µA)	7.89	0.02
TC of I_{REF} (ppm/°C)	77	780
Line regulation	0.008 µA/V	0.58 %/V
Area (mm^2)	0.175	0.0382
CMOS Process (nm)	180	180
Temperature range (°C)	-30 to 100	0 to 80
Measured samples	4	None

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