A Novel Topology of Nonisolated DC-DC High Step up Converters for Solar PV Power Plants

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Abstract—The present study proposes a new nonisolated DC-DC high step-up converter for solar PV power plant applications using the voltage boosting technique. The output voltage gain of this converter is high and the voltage stress on the switch and diodes is acceptable. The proposed converter has a switch for easier control. Moreover, to achieve higher reliability, the converter uses a common ground between the load and source. Voltage stress analysis, proper component selection, and converter evaluation are performed in continuous conduction mode (CCM). Simulation results verify the theoretical concept.

Index Terms—DC-DC converter; nonisolated; CCM; photovoltaic; power plants.

I. INTRODUCTION

Today, DC-DC converters are extensively being utilized in medical equipment, hybrid vehicles, computer systems, motor servers, portable equipment, communication systems, power factor correction, LED lighting systems, and electrical equipment, including uninterruptible power supplies, portable computers, and cell phones as well as green energy systems, including photovoltaic (PV) and fuel cell systems [1]. The switching frequency and pulse width modulation (PWM) technique are used to control these kinds of electronic power converters.

DC-DC converters fall into two types, i.e., isolated and nonisolated. Isolated DC-DC converters, including fullbridge, half-bridge, and flyback, require a high-frequency transformer, and this leads to high voltage gain. Moreover, voltage level is varied for different numbers of turns of windings. Nevertheless, in addition to high costs, high-frequency transformers impose significant losses and high switching voltages, which is attributed to the transformer leakage inductance [2-23]. Non-waste snubber circuits are utilized to prevent such issues. However, using these circuits increases the costs and dimensions of the converters as well as complicating the control process [3, 8].

High-frequency transformers are not used in nonisolated DC-DC converters, including Sepic, Cuk, boost, buck-boost, and buck converters, so they are less expensive. Moreover, these converters have higher efficiency and lower switching losses [4].

High step-up converters as a type of nonisolated DC-DC converters are extensively used in lighting applications [4-5], hybrid vehicle equipment [6], and solar energy systems, [7] including fuel cells and PV units. The wide usage of high step-up converters is because of their power density, higher efficiency, higher transient response ratio, lower power stress on components, protecting based on switches against electromagnetic interference and overvoltage, high voltage gain, smaller filter size, and direct inductor connection at the input.

In [9]-[10], a new topology was proposed for nonisolated DC-DC step-up converters. The voltage gain is appropriately increased in this technique. However, at higher voltages, the voltage stress on switches increases and more components are required, so a more complicated control system is required. Moreover, in [11], a similar technique was presented for voltage stress reduction in switches. Coupling inductors were used in [12, 13] for voltage gain improvement. Different numbers of turns in this technique allow improving the efficiency and voltage gain. The only problem with this method is that it increases the input current ripple [14].

In [15] and [16], serially connected nonisolated DC-DC converters were examined. This technique was aimed for high efficiency and improved voltage gain by implementing the fewest active switches. High cost, large size, and complicated control are some of the disadvantages of this technique, which is widely used for renewable energy sources. Switches and semiconductor components are used to reduce high stress [17].

The capacitor-switching technique [18], in which the minimum number of inductors is used, is based on the utilization of capacitors. Capacitor-switching technique was proposed in [19]. The large number of switches and capacitors in this approach allows higher voltage gain and efficiency as well as increasing current ripple.

In [20], the voltage lift (VL) method was presented. This method was also developed in [21, 22] and widely used to boost the output voltage level in DC-DC converters. The capacitor is charged up in this approach to obtain the appropriate input voltage level. Subsequently, by charging and discharging the inductor and capacitor, the output voltage is increased. Furthermore, additional capacitors can be employed to achieve the battery voltage level at the converter output by repeating this procedure. Several types of DC-DC step-up converters, such as Zeta, Sepic, and Cuk converters, were presented by Leo (Leo VL converters) and the voltage lifting technique was applied to them.

The present study proposes a novel single-switch transformerless DC-DC boost converter. The proposed converter...
is advantageous for several aspects, such as high voltage gain, low voltage stress on semiconductor devices, common ground, and low input current.

The remainder of this article consists of six sections: Section 2 presents the design and operation principles of the proposed dc-dc converter along with a CCM analysis. The equations of output voltage gain are given in Section 3. Section 4 compares the presented converter with some state-of-the-art converters. In Section 5, the voltage stress and components current are determined. Section 6 is dedicated to the calculations for selecting the converter components. Section VII presents the simulation results to confirm the theory of the proposed converter.

II. PROPOSED CONVERTER TOPOLOGY

The structure of the proposed converter is shown in Fig. 1. This converter consists of three diodes (D1, D2, and D3), five capacitors (C1, C2, C3, C4, and Co), three inductors (L1, L2, and L3), a MOSFET switch (S), and a resistance load (R). Moreover, this converter can reduce the voltage stress on the power switch and increase the output voltage gain.

A. Analysis of switching mode

Based on the operating modes of semiconductor components, the proposed converter has two switching modes in CCM. In this design, iC is the capacitor current, iL the inductor current, VC the capacitor voltage, Vin the input voltage, and VL the inductor voltage. To facilitate the analysis, some assumptions are made as follows:

- Inductors and capacitors are sufficiently large
- The equation of series resistors for capacitors and inductors is equal to zero
- Diodes and switches are ideal

B. Switching mode I

In switching mode I, the gate voltage Vgs level is high since the switch is on. During this time interval: the diodes are off, the inductors are charged; C3, C4, and Co are discharged; C1 and C2 are charged. The current path in switching mode I is shown in Fig. 2(a). Using Kirchhoff’s voltage law (KVL) and Kirchhoff’s current law (KCL) for the circuit equations, the following relations are obtained:

\[ V_{L1} = V_{in} \]  
\[ V_{L2} = V_{C3} - V_{C1} \]  
\[ V_{L3} = V_{C3} + V_{C4} - V_{C1} \]  
\[ i_{C1} = i_{L2} + i_{L3} \]  
\[ i_{C2} = i_{L3} \]  
\[ i_{C3} = i_{L2} + i_{L3} \]  
\[ i_{C4} = i_{L3} \]  
\[ i_{Co} = i_{o} \]  

C. Switching mode II

In mode II, the switch is off and Vgs level is low. During this time interval: diodes are on, the inductors are discharged; C3, C4, and Co are charged; C1 and C2 are discharged. Figure 2(b) illustrated the current path in this mode. Using KVL and KCL for the circuit equations, the following relations are obtained:

\[ V_{L1} = V_{in} - V_{C3} \]  
\[ V_{L2} = -V_{C1} = -V_{C4} \]  
\[ V_{L3} = -V_{C2} \]  
\[ i_{C1} = i_{C2} + i_{L3} + i_{C4} - i_{L2} \]  
\[ i_{C3} = i_{L1} - i_{C1} - i_{L2} + i_{C4} \]  
\[ i_{Co} = i_{C2} + i_{L3} - i_{o} \]
III. OUTPUT VOLTAGE GAIN

From KVL for $L_1$, $L_2$ and $L_3$, by applying the voltage relations for the inductors in both switching modes, Eqs. (15)-(22) are obtained as follows and $D$ is duty cycle and $M$ is voltage gain.

\[
\int_0^{DT} V_a dt + \int_D^{DT} (V_m - V_{C3}) dt = 0
\]

(15)

\[
\int_0^{DT} (V_{C3} - V_{C1}) dt + \int_D^{DT} (-V_{C1}) dt = 0
\]

(16)

\[
\int_0^{DT} (V_{C3} + V_{C4} - V_{C2} - V_{C1}) dt + \int_D^{DT} (-V_{C2}) dt = 0
\]

(17)

\[
V_{C1} = \frac{DV_m}{1-D}
\]

(18)

\[
V_{C2} = \frac{DV_m}{1-D}
\]

(19)

\[
V_{C3} = \frac{V_m}{1-D}
\]

(20)

\[
V_{C4} = \frac{DV_m}{1-D}
\]

(21)

\[
M = \frac{V_m}{V_m} = \frac{1 + 2D}{1-D}
\]

(22)

IV. COMPONENTS CURRENT AND VOLTAGE STRESS ANALYSIS

Current stresses of diode and switch occur when the switch is on. Furthermore, in each switching mode, when a component is connected, the current equation is the same as the current stress equation of the component. Additionally, the voltage stresses of the diodes and switch are determined when the switch is off. Hence, in each switching mode with the switch or diodes disconnected, the voltage across the component is expressed by the voltage stress equation.

According to Fig. 2(b), the maximum voltage across the switch is obtained as follows:

\[
V_s = V_{C3} = \frac{V_m}{1-D}
\]

(23)

From Fig. 2(a), the maximum voltage across diode $D_1$ is obtained as:

\[
V_D = V_{C3} = \frac{V_m}{1-D}
\]

(24)

As illustrated in Figs. 2(a) and 2(b), the current diode $D_1$ and the current stress of single-switch is achieved from (25) and (26), respectively:

\[
i_{D1} = i_{D2} = i_{D3} = \left(\frac{M_{CCM}}{3} + 2\right)I_o
\]

(25)

\[
i_s = (M_{CCM} + 2)I_o
\]

(26)

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V. LOSS ANALYSIS COMPONENT DESIGN/SELECTION CONSIDERATION

Assuming that $\Delta I_{L1}$, $\Delta I_{L2}$, and $\Delta I_{L3}$ are the maximum current ripples of the inductors, the minimum required inductances can be determined using Eqs. (27)-(29):

\[
L_1 = \frac{DV_m}{f_s \Delta I_{L1}}
\]

(27)

\[
L_2 = \frac{DV_m}{f_s \Delta I_{L2}}
\]

(28)

\[
L_3 = \frac{DV_m}{f_s \Delta I_{L3}}
\]

(29)

Assuming that the maximum voltage ripples of the capacitors are $\Delta V_{C1}$, $\Delta V_{C2}$, and $\Delta V_{C3}$, the minimum values of corresponding capacitors can be obtained using Eqs. (30)-(34):

\[
C_1 = \frac{2DI_m}{f_s \Delta V_{C1}}
\]

(30)

\[
C_2 = \frac{2DI_m}{f_s \Delta V_{C2}}
\]

(31)

\[
C_3 = \frac{2DI_m}{f_s \Delta V_{C3}}
\]

(32)

\[
C_4 = \frac{2DI_m}{f_s \Delta V_{C4}}
\]

(33)

\[
C_o = \frac{2DI_m}{f_s \Delta V_{Co}}
\]

(34)

Loss analysis is one of the most important tools that can significantly help to improve the operation of a converter. In general, losses of a converter depend on the type and the number of the components. Therefore, in this section, a loss analysis is performed to calculate the efficiency of the presented converter. Moreover, Table 1 compares the efficiencies of the presented converter and some recent designs.

The power losses of the inductors, diodes, capacitors, and switch are given in Eqs. (35), (36), (37), and (38), respectively.

\[
P_{Ls} = \sum_{n=1}^{s} \left[ r_{Ls} I_{Ls}^2 + \left(Kf^{\alpha}B_{m}W_{o}\right)(10^{-3}) \right]
\]

(35)

\[
P_{D(s)} = \sum_{n=1}^{s} \left[ V_f I_{D(s),o}\right] + r_{D} I_{D(s)}^2 + \frac{Q_{V_o}}{4} I_{D(s)}^2
\]

(36)

\[
P_{Cn} = \sum_{n=1}^{s} \left[ r_{Cn} I_{Cn}\right] + \frac{Q_{V_o}}{4} I_{Cn}\]

(37)

\[
P_{Sn} = \sum_{n=1}^{s} \left[ r_{Sn} V_{Sn} + r_{Sn} \right] V_{Sn} I_{Sn} + \frac{C_{Sn}}{2} V_{Sn}^2
\]

(38)

Where $P_L$, $P_D$, $P_S$, and $P_V$ are the power loss of inductors, diodes, switch, and capacitors respectively. Also, $r_{Ls}$, $r_{D}$, $r_{Sn}$, and $r_{V}$ are the resistance of inductors, diodes, switch,
and capacitors respectively. $V_f$ is voltage forward of diodes and $I_L$, $I_D$, $I_S$, and $I_C$ are the current of inductors, diodes, switch, and capacitors respectively.

Furthermore, the total loss and efficiency of the converter are obtained from Eqs. (39) and (40).

$$ P_{loss} = P_{L1} + P_{S1} + P_{C1} + P_{D1} \quad (39) $$

$$ \eta = \frac{P_{out}}{P_{out} + P_{loss}} \times 100 \quad (40) $$

VI. SIMULATION RESULTS

The value of inductors and capacitors are obtained from the inductors current ripple and capacitor voltage ripple, we have as below for the value of inductance and switching frequency.

$$ v_{L1} = V_f \frac{di_L}{dt} = L_1 \frac{\Delta i_L}{T_{on}} \Rightarrow L_1 = \frac{DV_f}{\Delta i_L} f \quad (41) $$

$$ \Rightarrow f_s = \frac{DV_f}{\Delta i_L i_1} \quad (42) $$

$$ i_{C1} = I_{L2} + I_{L3} = C_1 \frac{dv_{C1}}{dt} = C_1 \frac{\Delta v_{C1}}{T_{on}} \Rightarrow $$

$$ C_1 = \frac{D(I_{L2} + I_{L3})}{\Delta v_{C1} f} \quad (42) $$

By using MATLAB/Simulink and table I, the simulation results of a small 1.6 kW example of the presented converter are provided to examine the theoretical basis of the paper. An adjustable DC power supply is utilized to provide the input voltage of the proposed circuit. The values of capacitors and inductors are as follows: $C_1 = C_2 = 40 \mu F$, $C_3 = C_4 = 220 \mu F$, $C_5 = 240 \mu F$, $L_1 = L_2 = L_3 = 250 \mu H$, $R = 100 \Omega$, $f_s = 100 kHz$, $V_{in} = 50 V$, and $D = 0.7$. Consequently, Figs. 3(a), 3(b), and 3(c) are plotted to show the currents of the inductors. Moreover, the voltages of the five capacitors are illustrated in Figs. 3(d), 3(e), 3(f), and 3(g). Figure 4 illustrates the output voltage waveform of the proposed converter. Also, the efficiency versus duty-cycle is represented in Fig. 6.

Table I. Information about parameters of simulation.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>CCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1$, $L_2$, $L_3$</td>
<td>$K = 0.00551$; $\alpha = 1.23$; $\beta = 2.12$; $W_{\phi} = 28.5$; $B_\phi = 0.0545$</td>
</tr>
<tr>
<td>Diodes</td>
<td>Type: MUR1560; $V_{FJD} = 0.8 W$; $r_{0} = 0.01 \Omega$</td>
</tr>
<tr>
<td>Switches N-channel MOSFET</td>
<td>Type: IRFP460; $r_{on-off} = 0.27 \Omega$; $r_{f} = 59 \Omega$; $t_f = 58 \Omega$</td>
</tr>
<tr>
<td>$C_{DS} = 870 \mu F$; $Q_{f} = 5.7 \mu C$; $di/dt = 100 A / \mu S$</td>
<td></td>
</tr>
</tbody>
</table>

Fig.3 Simulations for currents of (a) $L_1$, (b) $L_2$, and (c) $L_3$; voltages of (d) $C_1$, (e) $C_2$, (f) $C_3$, and (g) $C_4$. 

(a)
VII. COMPARATIVE STUDY

Here, the presented converter is compared with other recent non-isolated boost converters. Table II compares the number of parts, the static voltage gain, and the voltage stress on semiconductor elements of the converters.

Table II. Comparing the converter presented in this study and other recent designs.

<table>
<thead>
<tr>
<th>Converters</th>
<th>The number of components</th>
<th>Voltage gain</th>
<th>Switch voltage stress</th>
<th>Diode voltage stress</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic boost converter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[8]</td>
<td>1 2 3 4</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>94.5%</td>
</tr>
<tr>
<td>[9]</td>
<td>1 2 3 4</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>94.5%</td>
</tr>
<tr>
<td>[10]</td>
<td>1 2 3 4</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>95%</td>
</tr>
<tr>
<td>[11]</td>
<td>1 2 3 4</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>94%</td>
</tr>
<tr>
<td>[12]</td>
<td>1 2 3 4</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>94%</td>
</tr>
<tr>
<td>Proposed converter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 3 5 12</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>95%</td>
</tr>
</tbody>
</table>

These curves are obtained according to Table II. In fact, first figure is voltage gain versus duty cycle and other figures are normalized diode voltage stress and normalized switch voltage stress versus voltage gain, respectively. Meanwhile, the value of $D$ is 0.7.

VIII. CONCLUSION

The current study presented a novel single-switch transformerless DC-DC boost converter. The advantages of the presented converter are as follows: common ground between load and source, high voltage gain without magnetic coupling, and low voltage stress on semiconductor elements. These features make the presented converter appropriate for utilization in solar PV power plants. Moreover, a steady-state analysis was conducted in CCM, and the presented converter was compared with some state-of-the-art boost converters in terms of voltage gain, voltage stress on semiconductor elements, the number of parts, and other specifications. Finally, a simulation with an output voltage of 370 $V$ was performed, and the theoretical basis of the study was verified.

REFERENCES


