Silicon Nanowire Technologies: brief review, home-made solutions and future trends

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Abstract—The silicon nanowire (SiNW) is poised to become an industry standard on the upcoming technological nodes. It presents improved current drive and modulation, minimized footprint, stackability, and a host of different beneficial characteristics. The last few years of research have focused on solving the last remaining challenges of SiNW fabrication as they roll into commercial usage. Now, novel devices, as well as channel and device stacking for 3D VLSI applications is being studied. As well as how can the SiNW geometry can be harnessed for More Than Moore materials and applications.

In this review, we present a sample of the range of devices, techniques and applications of SiNW structures, alongside novel developments in the research carried out at University of Campinas.

Demonstrations of JLFETs fabricated using Ga⁺-FIB, e-beam lithography, silicon etching in NH₄OH solution, FinFETs fabricated using Ga⁺ lithography and strained silicon structures are shown. Promising future developments in VLSI and More Than Moore applications such as vertically stacked nanowire geometries, graphene nanoribbon devices, and MagFETs are also presented.

Index Terms—Silicon; Nanowire; SiNW; nanoelectronics; scaling.

I. INTRODUCTION

To imagine how the modern society would be without the many tools and applications afforded by the field of electronics is nearly unfathomable. From the early transistorised consumer applications, to the WiFi revolution, the Information Age and beyond, the way forward has been paved since the second half of the 20th century by advancements in micro and nano electronics.

However, there has been indications that the End of Moore might be nearing, as the miniaturization in the physical devices have been slowing for more than a decade, as problems such as quantum tunneling and confinement, short channel effects and random telegraph noise start to present increasing problems for the technology moving forward [1]. Building on updates of the traditional planar process, multigate geometries such as the omega-gate and the finFET took to the forefront of nanofabrication, becoming the main component in high-end consumer electronics. The industry is now at similar crossroads than those in the transition from planar architectures to multigate ones and as such, Gate-All-Around (GAA) technologies such as Silicon Nanowire (SiNW) and Silicon Nanosheets (SiNS) are proposed as a way to fulfill the immediate need for increased performance and continuous scaling of the supply voltage. A representation of the finFET, already in commercial usage, and the SiNW and SiNS devices can be seen in Figure 1. Single-channel SiNW and SiNS devices can only take miniaturization so far, and as latest reports by the IRDS show, the next technological nodes will require many parallel SiNWs per device or even 3D VLSI application with multiple stacked devices, as pictured in Figure 2.

II. THE SILICON NANOWIRE

The ultimate expression of miniaturization is the Silicon Nanowire (SiNW), which consists of silicon structures only a few nanometer thick with very high aspect ratios in regards to their length. In this configuration, the superficial area of the channel that is influenced by the gate stack is maximized, which brings many beneficial effects to the device while avoiding short-channel effects. A Scanning Electron Microscopy side-profile of a typical nanowire application is shown in Figure 3.
In this context, brazilian home-made solutions to obtain 3D devices based on SiNWs such as Junctionless-FETs (JLFETs) and finFET are presented. For future trends our results in strained silicon technology, SiNW stacking, Graphene Nanoribbons (GNR) and anisotropic-magnetoresistence-based (AMR) MagFETs will be presented.

III. JLFET

The JLFET is a device that operates in the depletion mode [5]. This means that an orthogonal electric field is introduced to deplete the device channel region, which modulates the current. If the electric field is high enough, there is a complete depletion of the channel, which pinches off the current and places the device into cutoff operating region. While the channel region is only partly depleted or being driven into accumulation, the device is on an active state.

For the JLFET to present positive threshold voltages for the nMOS device (negative for the pMOS), it is required that the electric field introduced by the Metal-Oxide-Semiconductor stack is high enough to induce complete depletion throughout the channel region, therefore, careful consideration of insulator thickness, channel dimensions and gate metal is paramount.

A. JLFET on Ga⁺ FIB

Ga⁺ focused ion beam (GaFIB) dual beam system is a well-known platform that can be used for micro- and nanofabrication in circuit editing, for prototype nanomachining applications [11], [12], as well as MEMS and NEMS fabrication [13]. It has been recently employed for manufacturing nanostructures for a wide range of nanomechanical applications [14]. In this comprehensive study, the state-of-art of the mechanical properties of nanostructures is reviewed. This system allows direct-write maskless fabrication processes at the nanoscale as it does not require lithographic steps, as well as deposition or etching postprocessing [15], [16]. In addition, due to its highly precise ion beam, GaFIB can also be employed for ion implantation at a controlled dose [17], [18], as one can determine the beam parameters, such as ion beam voltage and current, pitch, dwell-time, exposed area, as well as total exposure time. Therefore, such a system seems very promising for prototypes nanofabrication of devices for several applications, like sensors [19], FETs [18] and advanced probing systems [20]. Puydinger et al. [17] have used GaFIB for Si milling and p-type local doping of p⁺-type silicon nanowires (p⁺-SiNWs). The resulting p⁺-SiNWs were then used to create pMOS junctionless nanowire transistor (JNT) prototypes on silicon-on-insulator (SOI) wafer substrates [Figure 4]. The electron beam from the GaFIB dual beam system was used to deposit SiO₂ gate dielectric and Pt source/drain electrodes for JNT transistors. The electron beam was chosen in order to avoid additional Ga⁺ implantation in the junctionless active region. Width, length, and height dimensions of p⁺-SiNWs were approximately 35 nm, 6 µm, and 15 nm, respectively, and the JNT gate length was 1 µm. The pseudo-MOS structure was then used to determine the electrical characteristics of the p⁺-SiNWs.

Alternatively, electron beam lithography (EBL) is a versatile nanofabrication technique for the submicrometric scale, that can be used either for direct patterning on electron-beam-sensitive resists or for preparation of photolithography masks [21]. Its electro-optical system compares to a scanning electron microscope (SEM), thus the process resolution is closely related to the electron beam size, as well as to the resist characteristics [22]. Typically, one can achieve tens of nanometer resolution using Poly(methyl methacrylate) (PMMA) resist. Puydinger dos Santos [22] has employed EBL in conjunction with plasma assisted etching (electron cyclotron resonance, ECR) and physical vapor deposition (PVD) for the fabrication of n-type JNT. Optimized devices consisted of 1280 parallel 50 nm wide, 15 nm thick n-type silicon nanowires. This configuration permitted a reasonable fabrication yield, which has enabled increasing the transistor current by three orders of magnitude when com-
pared to a single nanowire JNT. In this sense, the realization of such devices demonstrates that GaFIB and EBL are adequate platforms for the fabrication of numerous devices at the nanometric resolution (below 50 nm), such as FETs, nanowire-based sensors, especially other niche applications. Therefore, the aforementioned results open an avenue to new processing frameworks and demonstrate that the Center for Semiconductor Components and Nanotechnologies (CC-Snano – University of Campinas, Brazil) is a key facility that offers a full processing chain for academia and industry.

![SEM images of (a) the entire n-type JNT fabricated by EBL + plasma etching + PVD, (b) parallel n-type silicon nanowires of a multi-fin JNT and (c) a single n-type silicon nanowire of a single-fin JNT.](image)

Fig. 5: SEM images of (a) the entire n-type JNT fabricated by EBL + plasma etching + PVD, (b) parallel n-type silicon nanowires of a multi-fin JNT and (c) a single n-type silicon nanowire of a single-fin JNT.

### B. JLFETs using anisotropic silicon etching

Stucchi-Zucchi et al. [23] showed a nanosheet based approach to the fabrication of JLFETs possible even on micrometer scale lithography. The devices were fabricated on 340 nm Si over 400 nm SiO$_2$ SOI wafers. In this process, the active region was defined with traditional photolithography and ICP-RIE silicon etching, an oxide hardmask was then grown in a conventional furnace, and the gate region was exposed using SiO$_2$ etching in HF solution. The exposed region was then etched using NH$_4$OH solution, this solution is common in MEMS applications and has a highly anisotropic characteristic, with much higher etching rates on (100) planes than on (111), this gives the etched region a very distinct angled sidewall.

Figure 6a shows the 3D representation of the fabricated devices, it is possible to see the raised source and drain region when compared to the gate region, as well as the angled sidewalls. This difference in height could be harnessed, for instance, to create a doping gradient that enhances device characteristics. Figures 6b and 6c show the side-cut view of the device, with the angled sidewalls and a thin, barely visible channel, pseudo-MOS characterization was used to determine the channel thickness, which stood at around 67 nm.

Figure 6d shows the electrical measurements of the device, which presents good current modulation although having poor electrical contacts, as evidenced by the non-linearity for low drain voltages. This effect is present due to the low doping concentration, chosen to accentuate the current modulation characteristics of the JLFET device.

**Fig. 6**: (a) 3D representation of the resulting device. (b) $I_{DS}$ x $V_{DS}$ characteristic of the device. (c) SEM side cut view of the channel region. (d) colored overlay on the channel region SEM images. Adapted from [23]. Copyright 2018 by IEEE.

### IV. Ga$^+$ FIB Lithography finFETs

Leonhardt et al. [18] showed the implementation of the Ga$^+$ FIB lithography. This technique relies on the formation of a thin nonvolatile mask on the silicon regions irradiated by the Ga$^+$ ions, when exposed to a fluorinated plasma such as SF$_6$ and Ar. Leonhardt et al. [18] demonstrated that the time required for multiple fin definition by combining the Ga$^+$ FIB lithography and SF$_6$/Ar plasma etch techniques is drastically reduced when compared to the traditional GaFIB milling.

They could achieve relatively high yield when fabricating finFETs with multiple parallel fins by combining GaFIB direct patterning with optical lithography [Figure 7]. Moreover, when compared to other serial lithography methods, the Ga$^+$ FIB lithography presents only slightly higher processing time per device, with the added advantage of defining the fins directly on silicon. As such, there is no need for additional process steps such as resist coating, development, and hard mask etching that can be challenging in the nanoscale. Therefore, this new lithography method is a viable alternative for initial finFET prototyping. Although the preliminary results on fin definition are wider than reports from the industry, they show interesting developments for device prototyping, especially for sensor devices. Regarding the electrical behavior of the fabricated finFET, several issues were found in this first generation device, such as high source/drain contact resistance and rough fin sidewalls can degrade the electrical characteristics of the device, thus resulting in non-linear behavior of the $I_{DS}$ vs $V_{DS}$ curve at low $V_{DS}$ (Figure 7c) and leak current, respectively. This certainly can be improved upon optimizing the fabrication parameters.

These results are valuable due to the importance of device prototyping in the development cycle of new materials and techniques. Moreover, while in this work we applied the Ga$^+$ FIB lithography technique for finFET fabrication, it could potentially be used for vertically integrated nanowire FETs or other complex devices.

### V. Strained Silicon

Silicon presents an improved carrier mobility for certain forms of mechanical strain, and therefore strain has been used for years as a way to improve current drive. Numerous methods can be used to achieve strained silicon, for instance, SiGe-Si mismatched layers [24] and the strain that
results from the interface with other materials [25].

Strained silicon devices are responsible for some of the greatest increases in performance seen in previous technological nodes, and are at the forefront of maintaining the progress predicted by Moore’s law with silicon or any other semiconductor in very large scale integration [21], [26]. Not only do most traditional ways to achieve strain in silicon apply to SiNW structures, novel techniques that harness the unique geometry of SiNWs are also being proposed. In this sense, the characterization of strain in nanostructures is important to determine the potential of these technologies, and it is typically performed using micro-Raman when investigating strained silicon.

A. Obtaining strained silicon without external actuators

Spejo et al. [27] have recently reported on the Raman shift-stress behavior from the (001) silicon surface of highly strained ultra-thin (15 nm-thick) suspended nanowires with stresses in the range of 0–6.3 GPa along the [110] direction. The work employs a strain technology that offers a precise control of stress values at large sampling while reducing variability. The stress level of the nanostructures can be accurately evaluated by the finite element method simulations and further correlated to the Raman spectra. For stresses below 4.5 GPa, the aforementioned behavior was linear and the extracted stress shift coefficient was in agreement with those reported in the literature. On the other hand, for stresses greater than 4.5 GPa, the Raman shift-stress behavior resembles a quadratic function, as already demonstrated in germanium in the work of Gassenq et al. [28]. As far as its known to the authors, Spejo et al. [27] is so far the only work in literature to achieve a stress level up to 6.3 GPa.

Most interestingly, this platform reproducibly stresses the nanowire without the use of external actuators, thus allowing it to control the stress/strain along the nanowire length [Figure 8a]. This was achieved by firstly changing the dimensions of the silicon nanobridge from a SOI wafer by means of EBL in conjunction with plasma etching. Then, a wet etching recipe was employed to remove the buried SiO2 underneath the silicon bridge, thus modulating the final stress by increasing or decreasing the suspended area. It turns out that, by modulating the nanowire dimensions, the ratio of the cross-sectional areas between the nanowire and the pads changes, thus resulting in different static equilibrium situations with different stresses at the nanowire region. Remarkably, the final suspended nanowire presents mostly uniaxial stress, as shown in Figure 8b.

Despite the obvious application in high mobility CMOS-compatible devices, the strained silicon platform presented in the work of Spejo et al, with relatively simple fabrication steps, could be employed for stressing nanowires of different materials (like magnetic or nanocomposite materials), which can open an avenue to further studies of materials science, especially to investigate fundamental properties of materials.
VI. THE FUTURE OF SiNW AND BEYOND

A. Stacking SiNWs

The latest industry roadmaps indicate that the next step in transistor miniaturization is to vertically integrate multiple channels or devices. The most common processes to achieve vertically stacked SiNWs begins by growing alternated layers of epitaxial SiGe and Si, which are then etched into a tall and thin fin, and then either the SiGe or the Si layers can be selectively etched or oxidized, leaving the remaining material as vertically stacked suspended channels [29].

Sachetto et al. [30] showed using a version of the Bosch process that is optimized in order to enhance the scalloping effect, applied to each sidewall of a finFET fabrication, a stacked SiNW structure can be achieved. This method uses a modification of the Bosch process to emphasize the scalloped profile of the sidewalls, and a long oxidation to create hanging silicon channels.

Currently in development at CCSNano is a novel way to stack SiNW using silicon etching in alkaline solution. The geometric characteristics of the channel will be determined by the way that two distinct methods of anisotropic etching of silicon takes place: the Inductively-Coupled-Plasma Reactive-Ion-Etching (ICP-RIE), which can create nearly vertical sidewalls, and and the wet etching in alkaline solution, which etches (110) and (100) planes rapidly, while being slowed by (111) planes. The process steps and resulting channel profile can be seen in Figure 9.

By carefully designing each of the etching steps, as well as the passivation step, it is possible to create suspended channels with a diamond shape and tuned (111) to (110) surface ratios, as well as specific width to height ratios. This is useful in mobility coupling situations, as well as being a way to create a varied array of channel structures from low H/W ratio SiNWs to high H/W ratio vertical nanosheets.

![Figure 9: Process flow of the proposed GAA fabrication method, detail of the channel region.](image)

B. Graphene nanoribbons and GFET

Graphene transistor has a two-dimensional graphene monolayer as a conduction channel, which gives it excellent carrier transport properties, such as high mobility and saturation velocity [31]. These advantages are a consequence of the physical propriety of the graphene, which presents singular band energy without an energy gap. Unlike silicon, in graphene the conduction and valence bands meet at a single point, called the Dirac point [32, 33]. However, this intermediate characteristic between a metal and a semiconductor, makes the GFETs not switched, therefore having electrons and hole conduction according to the modulation voltage [34].

The development of this type of device became possible due to the significant advances in nanotechnology, in particular, the development of synthesis and transferring of large-area graphene. The GFET operation is similar to MOSFET devices [35]. The electrical responses of GFET are modulated according to the potential applied to the gate. Furthermore, the GFET devices present two branches of the transfer. For positive gate voltages, the channel presents an electron accumulation (n-type channel), while for negative gate voltage, the channel presents a hole accumulation (p-type) channel [31].

Rufino et al. [36] showed the fabrication process and electrical measurement of a Field Effect Transistors based on graphene ribbons with the current conduction channel with 10 wires (width of 0.36 µm each) in parallel, using the photolithography and oxygen plasma ashing. Figure 10 (a,b) show the SEM images of the graphene channel region which is possible to observe that the ribbons was defined only over the gate/gate oxide structures. Figure 10 (c) shows the drain-source current ($I_{DS}$) versus drain-source voltage ($V_{DS}$) curves from several values of gate voltage where the theoretical characteristic of GFET, such as ohmic behaviour and ambipolar behaviour are observed. Figure 10 (d) presents the $I_{DS}$ and transconductance curve characteristic reaffirming the graphene properties and showing transconductance maximum value of 0.36µS by the graphene ribbon.

![Figure 10: Graphene ribbons channel defined by photolithography process and oxygen plasma etching.](image)
VII. OTHER NOVEL MATERIALS FOR NANOWIRE-BASED DEVICES

Nanowires are suitable building blocks for nanoscale devices manufacturing. Nanowire-based devices show interesting features such as ultra-low power consumption and high sensitivity to electrical, physical or chemical stimuli [37, 38, 39, 40]. The extremely high surface-to-volume ratio associated with these nanostructures makes their electrical properties significantly more sensitive to the specific molecules adsorbed selectively on its surface [41]. It turns out that binding to the surface of a nanowire can lead to depletion or accumulation of carriers in the nanometer diameter structure (versus only the surface region of a planar device), thus increasing sensitivity to the point that single-molecule detection is possible in such nanostructures [40]. In other words, organic or inorganic molecules can act as a source or a trap of surface-conducting electrons and, therefore, modulate the nanowire’s electrical conductivity.

Furthermore, magnetic nanowires exhibit an additional conductivity modulation component that is regarded to the magnetoresistance (MR) effect [42, 43, 44]. The anisotropic magnetoresistance (AMR) had an important use for digital recording in hard drive disks (HDD) in early 90’s and allowed a substantial increase in the growth rate of the HDD storage areal density [45]. Moreover, Parking et al. [46] have recently proposed a new concept of non-volatile memory based on magnetic nanowires that can overcome the traditional HDD. This spintronic device is called the ‘racetrack memory’, which is entirely a solid-state device with no moving parts. This device can surpass the current HDD technology in terms of speed and data storage capacity, as shown in the following comprehensive works [46, 47, 48, 49]. Furthermore, the biggest commercial success of spintronics so far has been the development of extraordinarily sensitive detectors of small magnetic fields capable of operating at room temperature and above [50], which can also be adequate for the implementation of high performance magnetic RAM (MRAM) memories [51].

Puydinger et al. [52] have recently built a nanowire-based magnetic field-effect transistor (MagFET, Figure 11a) based on the AMR effect. The device was built using the conventional CMOS technology in conjunction with the electrical manipulation of nickel nanowires by means of the dielectrophoresis. The nanowires were previously grown by electrodeposition on anodic alumina oxide (AAO) templates, which is a high-yield technique for the growth of nanowires of a variety of materials, including semiconductor ones [53]. This MagFET prototype can pave the way to further implementation of versatile CMOS-compatible devices based on spintronics. On the other hand, focused-electron-beam-induced deposition (FEBID) is is a well-established maskless technique that allows definition of three-dimensional micro- and nanostructures, representing an advantage over multistep conventional resist lift-off lithography [54, 52, 16]. Traditionally, FEBID has been used for the fabrication of protective coatings during transmission electron microscopy (TEM) lamella preparation, photomask repair, circuit editing, or for electrically contacting nanowires or carbon nanotubes. During the last 15 years, dedicated FEBID applications have been demonstrated, such as nanolithography, stress–strain sensors, Hall sensors, gas sensors, among others [20, 55, 56, 19, 57]. It has become increasingly relevant in recent years, with the demonstration of controlled 3D nanoscale deposition and high purity deposits [20, 58]. In addition, the multi-beam FEBID has already been demonstrated [14], which would allow boosting the process speed and make FEBID a competitive technique. Nevertheless, Puydinger et al. [44], [52], [59] have employed FEBID to obtain rather less pure carbon-rich metal deposits. Their aim was to obtain granular material from nanometric grains embedded in a carbon matrix and investigate its magnetotransport properties outperforming the ones with higher metal content. The Co-Fe-C-O ferromagnetic nanowires grown by Puydinger et al. (Figure 11b) presented one of the highest AMR values so far reported in literature for FEBID-grown materials and were in the range of 20-110% larger than the AMR of pure Co nanowires, thus opening a promising route for future applications in magnetic memories and nonvolatile storage devices.

VIII. CONCLUSION

This article presented a brief review, the home-made solutions and the future trends about nanowire technologies, mainly Si NWs. It is important to notice that our results are...
obtained using the facilities of nano and micro fabrication at University of Campinas- Brazil.

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