Low-Dropout Voltage Regulator Designed with Nanowire TFET with Different Source Composition Experimental Data

Rodrigo do Nascimento Tolêdo[1*], Joao Antonio Martino[1], *Senior Member IEEE*, Paula Ghedini Der Agopian[1, 2], *Senior Member IEEE*

[1] LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
[2] UNESP, Sao Paulo State University, Sao Joao da Boa Vista, Brazil
email*: rntoledo@usp.br

Abstract— **This paper presents the design of low-dropout voltage regulators (LDO) using nanowire tunnel field-effect transistors (TFETs) and nanowire MOSFET. The devices are modeled using lookup tables implemented with experimental measures of TFETs with different source compositions (Si, SiGe and Ge) and MOSFET. In order to compare the designs, the transistors of the differential amplifier in all LDOs is biased with g_m/I_D = 8 V^{-1} with a load of 1 µA and 10-pF. It is shown that all TFET based LDOs are stables without the need of a compensator capacitor (C_C) even for higher load capacitance. For the MOSFET LDO, a C_C of 5-pF capacitor was used. The study shows that the TFET based LDOs deliver higher efficiency due to the possibility to operate with low bias current. In the transient analysis it is shown that the TFET LDOs have lower overshoot but higher delay. The Ge-TFET LDO presented settling times for load and line transient close to the MOSFET LDO with 15 µs and 30 µs. The SiGe-TFET LDO shows the best loop gain (60 dB), while the Si-TFET LDO delivers lowest quiescent current (300 pA) and the Ge-TFET have the best GBW (70 KHz) and PSR (-52 dB). It is concluded that the TFET based LDOs can deliver specifications similar or better than the MOSFET LDO even without the need of C_C and with less power consumption.**

Index Terms— **TFET, nanowire transistors, LUT, low-dropout voltage regulators, analog circuit design.**

I. Introduction

Due to the subthreshold slope theorical limit presented in MOSFET technologies, it is not possible to decrease the supply voltage without increasing the static power consumption on digital applications [1]. Tunneling Field Effect Transistors (TFETs) became an import research topic because there is no limit on its subthreshold slope, due to its fundamental conduction mechanism based on band-to-band tunneling [2]. Tunneling transistors also demonstrated to have orders of magnitude higher output resistance than MOS transistors, resulting in a higher intrinsic gain [3]. Those characteristics are good for analog applications and for that reason, analog circuits are been designed with TFETs modeled by simulations or experimental data [4]– [9], where is shown amplifiers with high voltage gain and ultra-low power dissipation.

This paper is an extension of [10], it focuses on the analysis of nanowire MOSFET and TFET with different source composition in capacitor-less low-dropout voltage regulators design. The low-dropout voltage regulator (LDO) is a crucial block in power management systems, as it is responsible to supply a constant voltage that serves as voltage source for the functional blocks [11]. The LDO operates with negative feedback, therefore compensation techniques must be implemented. An LDO is recognized as capacitor-less when the compensation is performed inside the block i.e. not at the output node.

Section II describes the devices characteristics. The devices used in this work are modeled using experimental data arranged in lookup tables. With the use of experimental data, the circuit evaluation is more precise since it includes the devices non-idealities disregarded by simulated data models. All LDOs are designed with nanowires working in the same bias conditions and same load, their implementation is described in Section III. The LDOs DC, AC and transient characteristics are compared and analyzed based on the devices behavior, the results are detailed in Section IV. Section V concludes this paper.

II. Devices Characteristics

The devices used are silicon vertical nanowires fabricated with the same process flow, they are shown in Fig. 1, information about the devices fabrication can be found in [12], [13].

While the channel and the drain are made of silicon, three TFETs with different source compositions are available: $Si_{73}Ge_{27}$ (SiGe-TFET), Ge (Ge-TFET) and Si (Si-TFET), the use of smaller bandgap materials in the source increases the ON state current without degrading its higher intrinsic gain characteristic [14]. The TFET structure is presented in Fig. 1(a), it has a gate underlap in the drain (L_{UN} = 100 nm), a gate overlap in the source (L_{OV} = 30 nm), a gate length of L_G = 150 nm, a channel length of L_{CH} = 220 nm and diameter d = 200 nm. The underlap is used in order to mitigate the ambipolar effect [15] and the overlap improves the device performance, like its subthreshold slope and on-state current still maintaining a high intrinsic gain [16].

The MOSFET is made of silicon in the channel, drain and source, it has a channel length L_{CH} = 220 nm and diameter d = 120 nm, the gate and channel are self-aligned. All devices have a gate oxide composed by 1.8 nm of HfO_2 on top of 1 nm of SiO_2. The transistor characteristics from a device perspective can be found in [5], [17]– [20]. The devices model and validation are described in [5]. The model consists of a drain current, a gate/drain (C_{GD}) and a gate/source (C_{GS}) capacitances experimental measures, where the data is placed on a lookup table (LUT), then the model is implemented using the analog hardware description language Verilog-A, thus circuit simulation is carried out using the Virtuoso Analog Design Environment from Cadence, the use of LUTs enables the design of devices that do not have an accurate model [21].

Digital Object Identifier 10.29292/jics.v18i1.653

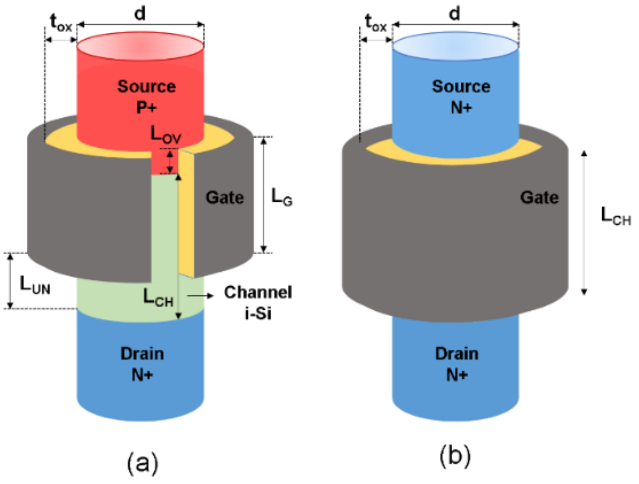

Fig. 1 Vertical nanowires transistors (a) TFET and (b) MOSFET schematics [10].

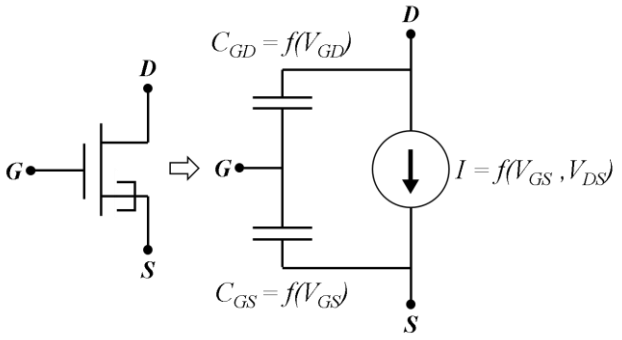

Fig. 2 Equivalent circuit schematic model for the measured nanowire transistors [10].

The Verilog-A code, implements the equivalent circuit from Fig. 2, the model consists of a current source representing the drain current, determined by V_{GS} and V_{DS} and capacitances C_{GD} and C_{GS} extracted from the LUT, determined by the V_{GD} and V_{GS} potentials, respectively. In the model, the number of nanowires in parallel can be varied to design a circuit. The experimental devices used in this work for Si-TFET had 400 nanowires while the other technologies each transistor had 100 nanowires. The experimental capacitance was extracted using devices with a large number of nanowires.

The output characteristics for the devices are shown in Fig. 3, where it should be noted that the drain current (I_{DS}) is given for only one nanowire, which was obtained by dividing the measured drain current by the number of nanowires for each device. It can be observed an increase in the drain current when more Ge is added to the source as expected, also the MOSFET presented the highest value. In Fig. 3 it can be noted that the TFET device reach the saturation for higher V_{DS} values.

From the inclination of the curve in saturation, it can be noticed that the TFETs curves presents higher Early voltage (V_E), also due to the higher I_{DS}, the they show higher output resistance, the extracted parameters are presented in Table I. The higher V_E presented by the Si-TFET is explained by the transport mechanism of the TFETs. At $g_m/I_D = 8\ V^{-1}$, the Si-TFET have higher influence of the trap-assisted tunneling, which has lower dependence on V_{DS} [18].

III. LDO Design

To facilitate the LDOs comparison, the simple topology of Fig. 4 was implemented. The LDO consists of an amplifier, a power transistor and a feedback network. The amplifier adjusts the power transistor conductance sensing the difference between a reference voltage (V_{REF}) and the feedback voltage provide by the feedback network (V_{FB}). The detailed description of the topology can be found in [10], it consists of:

- A differential amplifier composed by transistors M_1 to M_4;
- Current mirror formed by transistors M_5 and M_6, which mirrors the ideal current source I_B;
- The power transistor M_P;
- A feedback network formed by ideal resistors R_1 and R_2;
- Compensation capacitor C_C;
- The load which is modeled by resistor R_L and capacitor C_L.

The capacitor-less compensation used in this work, defines the pole located at the M_P gate to be the low frequency pole. This choice has the advantage of not using a bulky output capacitor to lower the output pole allowing full integration [22].

To make a fair comparison between the different devices, all amplifier transistors were biased with the same g_m/I_D, its dimensions were found using the g_m/I_D methodology [23], with $g_m/I_D = 8\ V^{-1}$. The load was defined to be $I_L = 1\ \mu A$ and $C_L = 10$-pF. To minimize the current consumption in the differential amplifier, the minimum number of nanowires in parallel were selected.

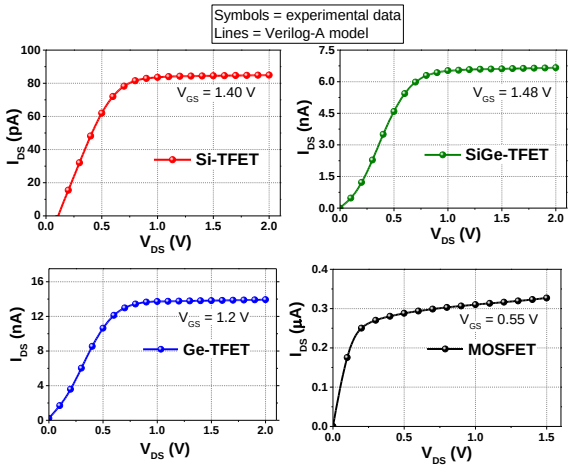

Fig. 3 Output characteristics per nanowire for different technologies where V_{GS} is biased in order to have the same $g_m/I_D \approx 8\ V^{-1}$ when the devices are saturated.

Table I. Early voltage and output resistance for the nanowires operating in the saturation region extracted from Fig. 3.

Parameter	Si-TFET	SiGe-TFET	Ge-TFET	MOSFET
V_E (V)	89	64	69	12
r_{ds}	900 GΩ	9 GΩ	5 GΩ	3 MΩ

Table II. Number of parallel nanowires for the designed LDOs devices.

Transistor	Si-TFET	SiGe-TFET	Ge-TFET	MOSFET
$M_{1\text{-}2}$	3	3	3	5
$M_{3\text{-}4}$	3	3	3	5
M_5	6	12	6	10
M_6	3	6	3	5
M_P	15×10^3	414	166	4

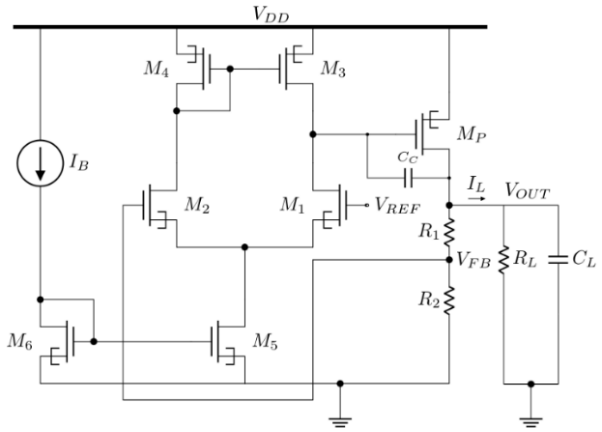

Fig. 4 TFET LDO Topology.

The drain current used in the design is proportional to the number of nanowires of the measured devices, the simulator takes the number of parallel nanowire and delivers the equivalent current. As the only degree of freedom related to the transistor dimensions is the number of nanowires in parallel, and since the nanowire MOSFET shows a smaller diameter, to use the same equivalent width, the MOS transistors have a greater number of nanowires in parallel. The number of parallel nanowires for all transistors can be seen in Table II. First, observe that the number of nanowires placed in parallel for the power transistor is high for the Si-TFET design and decreases for the LDOs designed with TFETs with greater amount of germanium in the source. More details about the sizing are discussed in [10].

IV. Results and Analysis

A. LDO Parameters

To explain the LDO results, its main parameters were extracted and can be seen in Table III. The power transistor transconductance $g_{m(MP)}$ is in the same order of magnitude for all LDOs, this happens because M_P provide the same load current in all designs. The M_P small-signal output resistance ($r_{ds(MP)}$) is smaller in the TFETs LDO due to the higher number of parallel devices together with the delayed saturation voltage showed in TFETs, that make it not possible to design an LDO with this topology that makes M_P transistor to operate in saturation. If M_P worked in saturation, the $r_{ds(MP)}$ parameter would be higher in the LDOs designed with TFETs.

The differential amplifier voltage gain (A_D) is higher for the LDO with TFETs, due to the higher output resistance, that, for Si-TFET, is four orders of magnitude greater than the MOSFET. This characteristic is expected since TFETs have higher output resistance and the transistors in the differential amplifier are saturated. Since the SiGe-TFET LDO operates with higher bias current, the transconductance of the differential pair is higher and together with the high Early voltage, the differential amplifier gain of the SiGe-TFET LDO is better. The M_P gate-to-source ($C_{GS(MP)}$) and gate-to-drain ($C_{GD(MP)}$) capacitances are higher in TFET LDOs, as M_P has a greater equivalent width. The feedback factor β is given by V_{FB}/V_{OUT}.

The analyzed LDO specifications are divided DC, AC and transient analysis. The DC results include the quiescent current (I_Q), the efficiency and the load regulation. The AC specifications comprise the power supply rejection, the loop gain and the gain-bandwidth product (GBW), the dropout and the settle time for load and line transients also are evaluated, the specifications are outlined in Tables IV and V.

B. LDO DC Results

Observe in Table IV that the LDOs designed with TFET has lower quiescent current resulting in a higher efficiency. The LDO designed with Si-TFET presented the lowest I_Q, which is expected since the addition of the Ge amount in the source increases the tunneling current. The efficiency is calculated as the relation between the power supplied by V_{DD} and the power delivered to the load, since all LDO have the same dropout voltage, better results are obtained to smaller quiescent current. Since the other devices have lesser current drive, the efficiency is degraded in MOSFET LDO given that the current through the amplifier is in the same order of magnitude of I_L, for higher I_L it is possible to design the MOSFET LDO to achieve high efficiency.

The load regulation indicates the output voltage variations for changes in the load current, it can be calculated by $(g_{m(MP)}A_D\beta)^{-1}$. Note that the load regulation does not depend on $r_{ds(MP)}$, thereby the load regulation is better in TFETs based LDO with the SiGe-TFET LDO presenting the best results due to its higher A_D.

C. LDO AC Results

In the AC analysis, the frequency response and power supply rejection (PSR) are evaluated. In the frequency response analysis, the loop is opened at the V_{FB} node to find the loop gain and phase showed in Fig. 5. The loop gain is given by $g_{m(MP)}R_{OUT}A_D\beta$, where R_{OUT} is the open-loop output equivalent resistance, given by $R_{OUT} = r_{ds(MP)}//(R_1+R_2)//R_L$.

It can be seen that the SiGe-TFET based LDO, presented the highest voltage gain, followed by the Ge-TFET circuit which can be explained by the high amplifier gain A_D. As explained in [10], the voltage gain of the second stage (g_mR_{OUT}) are low for the TFETs low-dropout regulators since $r_{ds(MP)}$ is degraded since it is not possible to design M_P to operate in the saturation region. With M_P operating in saturation, the output resistance of the TFET LDOs would be higher.

Table III. LDO parameters.

Devices	Si-TFET	SiGe-TFET	Ge-TFET	MOSFET
$g_{m(MP)}$ (µS)	6.64	5.70	7.56	7.62
$r_{ds(MP)}$ (KΩ)	171	182	234	2072
A_D (dB)	43	60	52	27
R_D (MΩ)	7705	636	556	9
$C_{GS(MP)}$ (fF)	5330	234	92	25
$C_{GD(MP)}$ (pF)	52.20	0.99	0.35	0
β	0.73	0.73	0.73	0.8

Table IV. LDO results for V_{DO} = 300 mV, I_L = 1 µA and C_L = 10 pF.

Devices	Si-TFET	SiGe-TFET	Ge-TFET	MOSFET
V_{OUT} (V)	3.3	3.3	3.3	1.5
I_Q (nA)	0.3	21.2	42.9	1468.5
Efficiency	91.6 %	89.7 %	87.9 %	32.4 %
Load Regulation (mV/µA)	1.40	0.25	0.58	7.37
Line Regulation (mV/V)	13.3	8.7	2.6	3.4
Loop Gain (dB)	41.2	56.7	51.1	41.4
GBW (Hz)	2	7000	70000	52500
C_C	-	-	-	5 pF

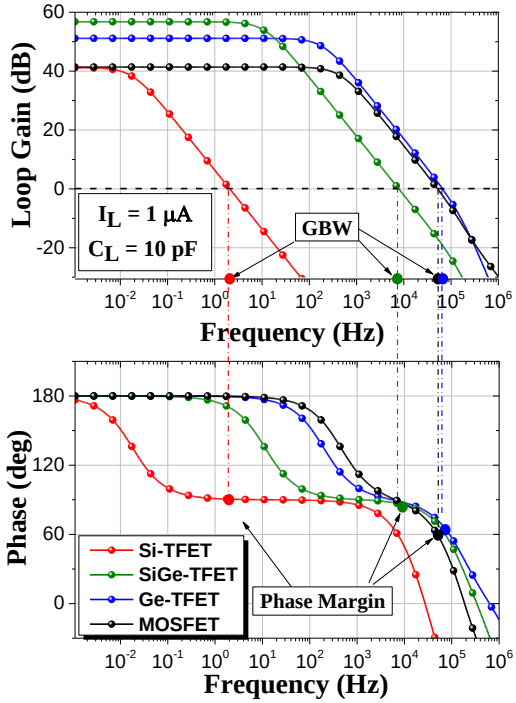

Fig. 5 Loop gain and Phase as a function of frequency.

The dominant pole is $(2\pi R_D g_{m(MP)} R_{OUT} C_{GD(MP)})^{-1}$, from Table III, it can be seen that the Si-TFET have the highest R_D and $C_{GD(MP)}$, therefore its pole is located at a lower frequency resulting in the lowest gain-bandwidth product (GBW), which accounts for a slower response.

All TFET LDOs are compensated without the need of an extra compensation capacitor, C_C in Fig. 4, a 5 pF capacitor was needed to in the MOSFET LDO to ensure a 60 degree phase margin. The Ge-TFET based LDO has the highest GBW due to its high gain even with dominant pole located at a frequency lower than the MOSFET LDO. It is possible to notice in Fig. 6 that all TFET LDOs have a phase margin greater than 60 degrees, therefore it is possible to drive a wide range of output capacitance even without using a compensation capacitor. The phase margin as a function of the load capacitance for all TFET LDOs was extracted and the result is illustrated in Fig. 6. Observe that, to have a minimum of 60 degrees phase margin, the Si-TFET LDO can drive load capacitances up to 650 nF, the SiGe-TFET LDO can guarantee the phase margin constraint with a maximum of 140 pF for the load capacitance and 15 pF for the Ge-TFET LDO.

Usually, LDOs are supplied with a noisy voltage delivered by switching regulators, therefore the PSR is an important specification, it measures the V_{DD} ripple reduction on V_{OUT}. The PSR as a function of frequency is presented in Fig. 7. It can be seen that the Ge-TFET based LDO presents better results, with a higher PSR for all frequency range. Although presenting the higher loop gain, the SiGe-TFET LDO PSR is degraded due to ripple passing through the differential amplifier injected in the M_P gate. The Si-TFET LDO has the lowest supply rejection that decays at low frequencies, this is expected due to its loop gain behavior. The MOSFET LDO has a PSR almost equal to the Ge-TFET LDO, even with lower loop gain, since the $r_{ds(MP)}$ is in the same order of magnitude of R_L, which is 1.2 MΩ for MOSFET LDO, the PSR reaches better values [24].

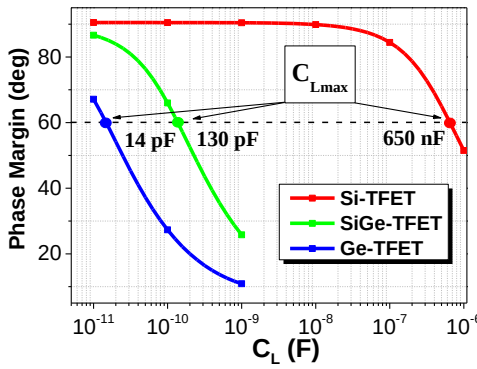

Fig. 6 Phase margin as a function of the load capacitance for the TFET LDOs. The maximum load capacitance that guarantees a phase margin of 60 degrees is indicated for each LDO.

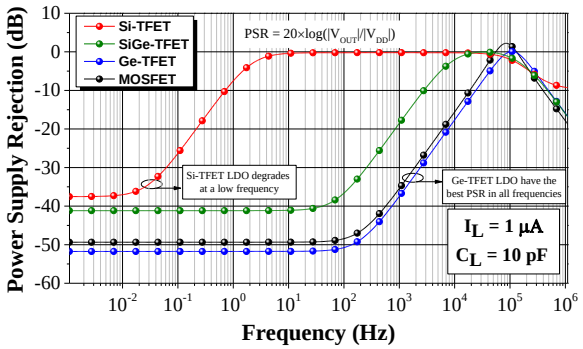

Fig. 7 Power supply rejection (PSR) as function of frequency.

D. LDO Transient Analysis

The line transient was performed with a V_{DD} step from 3.6 V to 5 V on the TFET LDOs and from 1.8 V to 2.5 V on the MOSFET LDO, the output voltage response is showed in Fig. 8 and the settling time (t_S) together with the overshoot (ΔV) are indicated on Table V. With the same load capacitance, all LDOs have an overshoot in the same order of magnitude, with the SiGe-TFET LDO showing the best result. Due to low GBW, the Si-TFET LDO presented the slowest response, since t_S is inversely proportional to the GBW, the MOSFET LDO have the fastest response with the Ge-TFET showing a 5 µs slower settling time due to the higher M_P capacitances. Although the Ge-TFET LDO showed the best GBW, the higher capacitances of M_P together with the low I_B, results in a smaller slew-rate that deteriorates the settling.

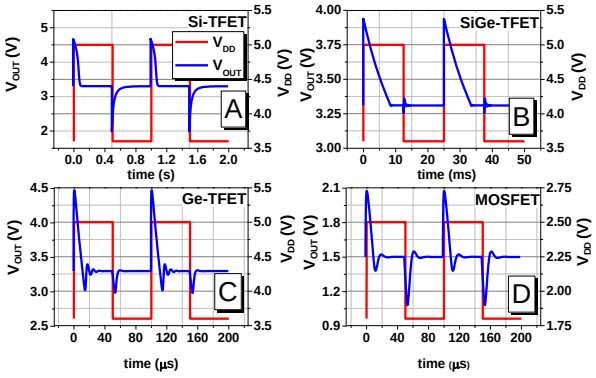

Fig. 8 Line transient response for all LDOs. The TFET LDOs (A to C) were subjected to a 1.4 V voltage step, while the MOSFET LDO (D) response is for a 0.7 V step.

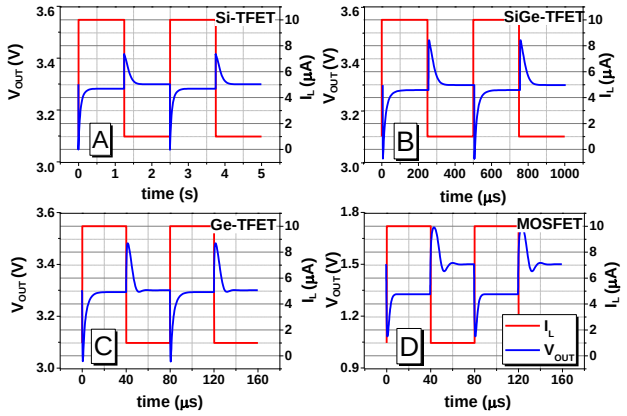

Fig. 9 Load transient response for all LDOs. The load current I_L varies from 1 µA to 10 µA.

Table V. LDO transient results with C_L = 10 pF. All data were extracted for positive steps.

Devices		Si-TFET	SiGe-TFET	Ge-TFET	MOSFET
Line Transient	ΔV(%)	39	18	33	40
	t_S	90 ms	7.5 ms	30 µs	25 µs
Load Transient	ΔV(%)	7.6	9.1	8	32
	t_S	0.5 s	80 µs	15 µs	8 µs

The load transient was analyzed with the load current changing from 1 µA to 10 µA, the results can be seen on Fig. 9. As can be seen in Table V, the MOSFET LDO have the higher overshoot, but it is important to mention that the absolute value in volts is almost the same for all LDOs, since V_{OUT} is 1.5 V in the MOSFET LDO, the overshoot becomes higher. The settling time follows the same trend as for the line transient, with the MOSFET LDO showing the best result and the Si-TFET LDO with the slowest response. Due to the low load regulation and gain degradation for I_L = 10 µA, the output voltage of the MOSFET LDO falls to 1.3 V.

V. Conclusions

The behavior of nanowire TFETs with different source compositions and nanowire MOSFET used in low-dropout voltage regulator design were compared in this work. The results showed that, the Si-TFET based LDO is recommended when an ultra-low current consumption is required and fast response is not essential since it presented an I_Q of 300 pA with a GBW equals to 2 Hz, while for SiGe-TFET LDO, which presented the second lower I_Q is 21.2 nA. The SiGe-TFET LDO have the highest loop gain, which guarantees the best load regulation (0.25 mV/µA) followed by the Ge-TFET LDO (0.58 mV/ µA). Despite of dissipating higher I_Q than SiGe-TFET LDO, the Ge-TFET LDO presents better performance in all other results, with a higher GBW (70 KHz) than MOSFET LDO (52.5 KHz), consuming thirty times less current. The transient analysis showed that the MOSFET LDO have the fastest settling time followed by the Ge-TFET LDO that has a t_S in the same order of magnitude.

Since the load current is relatively low for the nanowire MOSFET current drive capability, it presents poor efficiency (32.4 %), higher efficiency can be achieved with higher load currents that can be delivered by the nanowire MOSFET due to its higher current drive. It was observed that, for a given load capacitance, TFET based LDOs can reach stability without a compensation capacitor allowing higher load capacitances, therefore the TFET LDOs are suited for capacitor-less LDO implementations.

Acknowledgements

The authors would like to thank CNPq and CAPES for the financial support. The authors also would like to thank imec for suppling the devices and Alexandro de Moraes Nogueira for providing the device data.

References

[1] F. Balestra, “Challenges for high performance and very low power operation at the end of the Roadmap,” *Solid State Electron*, vol. 155, pp. 27–31, May 2019,

[2] A. M. Ionescu and H. Riel, “Tunnel field-effect transistors as energy-efficient electronic switches,” *Nature*, vol. 479, no. 7373. pp. 329–337, Nov. 17, 2011.

[3] P. Agopian, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, and C. Claeys, “Experimental comparison between trigate p-TFET and p-FinFET analog performance as a function of temperature,” *IEEE Trans Electron Devices*, vol. 60, no. 8, pp. 2493–2497, 2013,

[4] N. O. Adesina, M. A. U. Khan, and J. Xu, “A Low Power MoS2TFET-Based Op-amp Design for Computational Circuits,” in *2021 IEEE 12th Annual Information Technology, Electronics and Mobile Communication Conference, IEMCON 2021*, 2021, pp. 731–736.

[5] A. De Moraes Nogueira, P. G. Der Agopian, and J. A. Martino, “Operational transconductance amplifier designed with nanowire tunnel-FET with Si, SiGe and Ge sources using experimental data,” *Semicond Sci Technol*, vol. 35, no. 9, Sep. 2020,

[6] R. S. Rangel, P. G. D. Agopian, and J. A. Martino, “A Tunnel-FET device model based on Verilog-A applied to circuit simulation,” Aug. 2018.

[7] C. -N. Chang, Y. -N. Chen, P. S. P. -T. Huang, and C. -T. Chuang, “Exploration and evaluation of low-dropout linear voltage regulator with FinFET, TFET and hybrid TFET-FinFET implementations,” 2017.

[8] M. R. Tripathy *et al.*, “Device and Circuit-Level Assessment of GaSb/Si Heterojunction Vertical Tunnel-FET for Low-Power Applications,” *IEEE Trans Electron Devices*, vol. 67, no. 3, pp. 1285–1292, Mar. 2020,

[9] L. Barboni, M. Siniscalchi, and B. Sensale-Rodriguez, “TFET-Based Circuit Design Using the Transconductance Generation Efficiency gm/Id Method,” *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 208–216, May 2015,

[10] R. do Nascimento Toledo, J. A. Martino, and P. G. Der Agopian, “Nanowire TFET with different Source Compositions applied to Low-Dropout Voltage Regulator,” in *2022 36th Symposium on Microelectronics Technology (SBMICRO)*, Aug. 2022, pp. 1–4.

[11] R. J. Milliken, J. Silva-Martínez, and E. Sánchez-Sinencio, “Full on-chip CMOS low-dropout voltage regulator,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 9, pp. 1879–1890, 2007,

[12] A. Vandooren *et al.*, “Analysis of trap-assisted tunneling in vertical Si homo-junction and SiGe hetero-junction Tunnel-FETs,” *Solid State Electron*, vol. 83, pp. 50–55, 2013,

[13] A. Vandooren, D. Leonelli, R. Rooyackers, K. Arstila, G. Groeseneken, and C. Huyghebaert, “Impact of process and geometrical parameters on the electrical characteristics of vertical nanowire silicon n-TFETs,” *Solid State Electron*, vol. 72, pp. 82–87, Jun. 2012,

[14] Woo Young Choi, Byung-Gook Park, Jong Duk Lee, and Tsu-Jae King Liu, “Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec,” *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 743–745, Aug. 2007,

[15] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, “Tunnel field-effect transistor without gate-drain overlap,” *Appl Phys Lett*, vol. 91, no. 5, 2007,

[16] K. M. Liu and C. P. Cheng, “Investigation on the Effects of Gate-Source Overlap/Underlap and Source Doping Gradient of n-Type Si Cylindrical Gate-All-Around Tunnel Field-Effect Transistors,” *IEEE Trans Nanotechnol*, vol. 19, pp. 382–389, 2020,

[17] P. G. D. Agopian *et al.*, "Comparison between vertical silicon NW-TFET and NW-MOSFET from analog point of view," in *EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon*, Jan. 2015, pp. 233–236.

[18] P. G. D. Agopian *et al.*, "Influence of the source composition on the analog performance parameters of vertical nanowire-TFETs," *IEEE Trans Electron Devices*, vol. 62, no. 1, pp. 16–22, Jan. 2015,

[19] C. Bordallo *et al.*, "Influence of the Ge amount at source on transistor efficiency of vertical gate all around TFET for different conduction regimes," in *2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, EUROSOI-ULIS 2016*, Mar. 2016, pp. 242–245.

[20] A. de M. Nogueira *et al.*, "OTA Performance Comparison Designed with Experimental NW-MOSFET and NW-TFET Devices," in *2019 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct. 2019, pp. 1–3.

[21] A. A. Youssef, B. Murmann, and H. Omran, "Analog IC Design Using Precomputed Lookup Tables: Challenges and Solutions," *IEEE Access*, vol. 8, pp. 134640–134652, 2020,

[22] J. Torres *et al.*, "Low drop-out voltage regulators: Capacitor-less architecture comparison," *IEEE Circuits and Systems Magazine*, vol. 14, no. 2, pp. 6–26, 2014,

[23] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sep. 1996,

[24] V. Gupta, G. A. Rincón-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proceedings - IEEE International SOC Conference*, 2004, pp. 311–315.