An Analytical Gate Delay Variability Model for Low-Power Applications under the Process Variations Effects

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***Abstract*— Defining the timing characteristics behavior, such as the gate delay and the oscillation period, is an essential task in integrated circuits (ICs), especially for low-power CMOS-based technologies. The nanometric-sized devices designed to achieve low-power consumption have higher threshold voltages. Hence, these devices are operated at the near-threshold regime, or slightly above the threshold. In these regions, shifts in electrical parameters (expressed in terms of drain current or threshold voltage) may severely impact the integrated circuit behavior. Consequently, the time-dependent sources of variability (e.g., the bias temperature instability) impose a crucial reliability problem that affects time delay variability and induces slope propagation effects along the signal path. In this context, an improved analytical model to properly account for both the gate delay and its variability is presented, taking into account the properties of low-power devices. Additionally, the applicability of the model is presented in a case study of a ring oscillator. The analytical model derived allows a suitable and low computational time-consuming estimative for the parameters' degradation. Supported by Monte Carlo simulations, the extracted results indicate that the proposed method provides a better estimate for the ring oscillator jitter when compared to the simplified propagation of uncertainty method.**

***Index Terms*— Time-dependent variability; slope propagation; near-threshold regime; bias temperature instability (BTI); CMOS technology.**

I. Introduction

The CMOS technology is widely employed in integrated circuits (ICs) design. Alongside the massive MOSFET scale to nanometric sizes to achieve high performance, the sources of variability have imposed a crucial reliability problem that scales inversely with the area [1]. In this context, significant efforts have been made to understand and precisely model the IC's behavior with analytical methods to support engineers in their projects and reduce computational costs.

There are time-independent and time-dependent sources of variabilities that cause the MOSFETs electrical parameters to change. The latter, which modifies the behavior of the transistors over time, include the bias temperature instability (BTI), an aging mechanism that degrades the response and may lead to circuit malfunction [2].

In circuit analysis, BTI degradation is usually translated to threshold voltage (V_T) fluctuations, resulting from a reduced driving capability, i.e., a drain current decrease. This time-dependent variability stems from the charge trapping and de-trapping phenomenon, which occurs in traps located in the oxide and oxide-semiconductor interface. Briefly, one defining aspect of BTI is the time constants of the traps (named capture and emission times). BTI degradation arises when the emission times of the traps are considerably longer than the capture times [2, 3]. For this reason, understanding and properly accounting for time-dependent sources of variability is key to understanding logic delay variability over time, posing an important challenge for reliability modeling toward robust circuit design, particularly at low-power (LP) conditions.

To achieve low-power consumption, the CMOS devices display high threshold voltages and are subjected to low supply voltages, causing them to operate at the near-threshold regime. At this conduction point, MOSFETs' drain current is exponentially dependent on both V_T and supply voltage values [4, 5, 6], thus, making these transistors highly susceptible to electrical parameter shifts – expressed in terms of threshold voltage or drain current.

The signal slopes, that are propagated forward through the circuit's nodes materializing on other inputs and outputs [7], hold an elevated influence due to the properties of slower devices (i.e., low-power and low-voltage transistors): the higher sensitivity of these devices enhance the slope propagation of the signals and its effects in the subsequent nodes of an integrated circuit. Owing to that, time-dependent sources of variability, such as BTI, degrade the slope propagation due to V_T shifts, affecting the gate delay variability and the critical path delay estimation. Hence, to properly account for timing variability, it is necessary to account not only for the delay variability of the individual logic gates but also for the impact of their variability on the adjacent gates due to the enhanced slope propagation.

In this work, an improved analytical method to evaluate the delay propagation and oscillation period of CMOS logic gates and their variability is proposed. The goal of deriving a simple semi-mathematical analysis is to:

1. Account for the time-dependent sources of variability through V_T deviations – due to the charge trapping phenomenon – and the signal slopes impact – induced by the high sensitivity of low-power transistors – through the circuit.

2. Simplify the analysis and the computational cost required to address the charge trapping phenomenon that relies on costly Monte Carlo (MC) simulations, by simplifying the approach through the propagation of uncertainty technique.

To that, a first-order linear system and the principles of propagation of uncertainties alongside sensitivity analysis

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are employed to approximate the mean and variance of logic gates' propagation delay and oscillation period. A 7- stage CMOS-based ring oscillator, built with a 22nm Predictive Technology Model (PTM) [8] for low-power applications, is used as the case study. Monte Carlo simulations were used to validate the results. The circuit simulations were performed using NGSpice [9].

The following sections of this work are organized as follows. Section II provides a brief analysis on different analytical and statistical models for gate delay approximations. In sections III and IV, we derive the model proposed in this work – for both gate and circuit-level investigation, respectively. In section V, the extracted results were compared to MC simulations and to conventional delay estimation methods, disregarding slope propagation effects. Finally, section VI provides the final remarks and summarizes the contributions of this work.

II. Related Works

There are different means to estimate the logic gate delay from devices that operate near to or within the subthreshold region. They can be defined through the current analysis at this conduction point and employing different statistical analyses, such as log-normal (LN) distributions [4, 5] and log-skew-normal (LSN) distributed gate delay values [6].

The LN distributions are widely seen to precisely approximate the circuit behavior [4, 5]. In [4], the model defines a gate and circuit-level analysis taking into account the correlation between the adjacent gates in digital circuits' path operating near to the threshold voltage (NTV) regime. The delay analysis is analytically extended to stacked gates designs in [5], suitable for transistors in the NTV domain. LSN-distributed gate delay models are proposed as a high-accuracy method by [6], especially for devices at the NTV regime, considering the process variations impacts that induce the threshold voltage to fluctuate.

It is clearly defined that the gate delay evaluation is crucial to comprehending circuit behavior and its reliability. The estimation of this metric has been a leading topic of MOSFETs' analysis for a long time, especially with the impulse of submicrometer devices [10]. Additionally, low-power and low-voltage delay modeling has been debated, also, as a meaningful consideration in the last decades [11, 12, 13]. These works point to the impact of input ramps - due to the properties of low-power devices - in the delay approximation of modern MOSFET technologies at that time. As the evolution to nanometer sizes grows, these properties emerge as essential factors to be studied.

The methods presented in [4, 5, 6] share a common characteristic in their deduction, as each proposes an analytical methodology based on the analysis of the drain current of the MOSFETs. Therefore, these models are expected to be integrated as modifications in simulation tools. However, there is another analytical manner to define the gate delay from low-power devices: using the logic gates delay extracted straight through easy and low computational cost SPICE simulations. This is the goal of this work and defines an advantageous form to approximate the results without underestimating them, at the same time that it can be used in parallel with different simulation and mathematical tools. Meanwhile, both the complexity and the number of circuit simulations are reduced.

Unlike the studies previously introduced, the use of SPICE simulations as tools in these characterizations defines that any changes in the software codes are not required since the analyses predict the behavior of the integrated circuits from voltage nodes of its digital logic gates.

III. Analytical Gate Delay Model

To define the timing characteristics – and the variability – of ICs that operate near the subthreshold region, it is essential to understand the slope propagation consequences to the following stages as a function of threshold voltage shifts and the low-power device's properties [11, 12, 13].

The signal slopes propagated to the subsequent elements of the integrated circuits will depend on the properties of the technology node. Fig. 1 helps to clarify how the gate delay-induced degradation phenomenon arises, where the number of stages affected by the delay impact of a single gate of the integrated circuit is presented. Three different technologies nodes are used for comparison [8]. As the low-power technology shrinks, the number of stages affected by the threshold voltage fluctuation increases as well as the impact values.

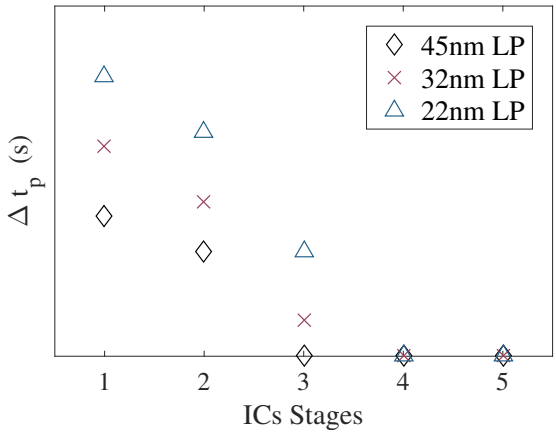

Fig. 1: Stages affected by the presence of slope signals (gate delay induced-degradation or shift, Δt_p) due to a threshold voltage fluctuation (equal to $20mV$) in a single ICs gate (for different low-power (LP) technology nodes [8]).

Thus, to model the behavior of low-power integrated circuits, the stages cannot be approximated individually and account only for their behavior. It is also necessary to consider the additional contribution of the other circuit stages. For that, the analytical delay model focuses on two levels of analysis: first, on the device (logic gate) level and, the second part, on the circuit level, to define the behavior of larger and more complex circuits. CMOS inverters (device level) and ring oscillators (circuit level) are used as a case study to demonstrate the applicability of the proposed model.

A compact model for BTI simulations under cyclostationary conditions presented in [3] is considered to address the issues caused by BTI in the MOS transistor threshold voltage. This model adopts the BTI effect on the time-zero operating point and is suited for oscillator circuits.

The first step in modeling the logic gate's behavior is to evaluate the influence caused by a shift of its V_T (ΔV_T) on

adjacent devices through circuit simulations. A simple chain of logic gates can be simulated to extract the necessary parameters.

A. Circuit Simulation

To start the model derivation, two simple circuit simulations were performed to determine the delay properties and to study each V_T shift-induced impact. The circuit under analysis consists of a chain of the elements chosen to be studied: in this case, at the device level, CMOS inverters are examined. Fig. 2 consists of a CMOS inverters chain, simulated at a first moment without any ΔV_T. In series with the circuit, two CMOS inverters were placed to represent the fan-in and fan-out elements of the chain.

The logic gate delay (t_p) is measured from its typical definition which is the average between the response times of a gate when its signals change from low-to-high and high-to-low as they reach $V_{DD}/2$, respectively. In this case, t_p defines the mean value of gate delay without any V_T shift in the device and V_{DD} describes the nominal supply voltage of the transistors of the CMOS inverters.

Subsequently, a new simulation is evaluated for the same circuit. For that, a V_T shift is applied at the chain's first CMOS inverter stage (defined as INV_1), and each effect caused by this deviation is extracted – employing the sensitivity analysis principles [14]. From Fig. 3, the characterization is defined by focusing only on the chain's behavior.

The difference between the analysis of the two states (different simulations) represents the impacts caused to the gate delay due to a threshold voltage variability in a time observation window.

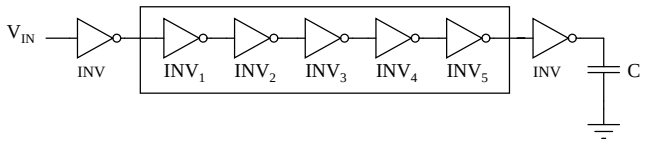

Fig. 2: CMOS inverter chain composed of 5 inverters in series with fan-in and fan-out elements, a load capacitance (C = 1pF), and a square-wave source ($\approx$ 2.2GHz, with a 0.95V amplitude) as the input voltage V_{IN}. The W/L ratio is 44nm/22nm for the PMOS and 22nm/22nm for the NMOS transistors, based on a 22nm technology for low-power applications [8].

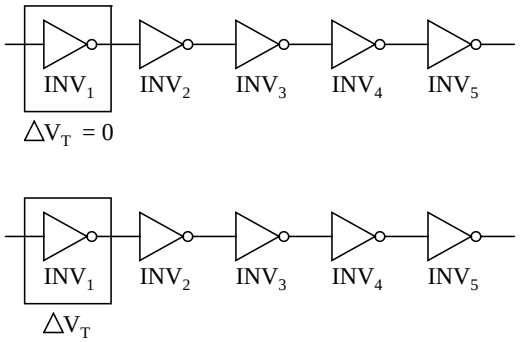

Fig. 3: 5-CMOS inverters chain. The top figure depicts the first part of the characterization: a simulation without any shift in the threshold voltage. The bottom figure is used for the second part of the analysis, applying a threshold voltage shift at the first stage of the chain.

In Fig. 1 it is shown that the impact is different for each technology node considered. In this work, the transistors are based on a 22nm LP technology node [8], upon which not only the circuit's first stage (INV_1) will be affected by a V_T variation but also the second (INV_2) and third (INV_3) stages due to slope propagation. Also from Fig. 1, it is seen that the gate delay induced-degradation (Δt_p) caused by ΔV_T can be neglected after the third stage due to their small values (Δt_p tends to zero), this implies that the upcoming ICs stages will not be impacted due to slope propagation.

Then, generically, the average gate delay (t_{p_n}) of a n-stage is given by t_p added to the sum of the individual impacts of the adjacent gates due to a V_T shift, so that:

$$t_{p_n} = t_p + \Delta t_{pn}, \tag{1}$$

where Δt_{pn} is the *n*–stage average gate delay induced-degradation. Thus, the problem of deriving a model that takes into account the gate delay induced-degradation due to slope propagation resides in analytically solve Δt_{pn}.

B. Gate Level

The average gate delay induced-degradation, Δt_{pn}, of an *n*–CMOS gate is given by the sum of the individual impacts of the previous gates to their impact due to a V_T shift, which can be written as

$$\Delta t_{pn} = a_{n1}\Delta_{tp_1} + a_{n2}\Delta_{tp_2} + ... + a_{nm}\Delta_{tp_i}, \tag{2}$$

or in an extended form for each stage of the circuit,

$$\begin{cases} \Delta t_{p1} = a_{11}\Delta_{tp_1} + a_{12}\Delta_{tp_2} + ... + a_{1m}\Delta_{tp_i} \\ \Delta t_{p2} = a_{21}\Delta_{tp_1} + a_{22}\Delta_{tp_2} + ... + a_{2m}\Delta_{tp_i} \\ \vdots \\ \Delta t_{pn} = a_{n1}\Delta_{tp_1} + a_{n2}\Delta_{tp_2} + ... + a_{nm}\Delta_{tp_i} \end{cases}, \tag{3}$$

that is characterized as a first-order linear system, where a_{nm} is the delay coefficient of the *n*-th inverter caused by shifts on the *m*-th inverter, Δ_{tp_i} is the total delay shift of the *i*-th inverter. Note that eqs. 2 and 3 can be expressed in matrix notation to evaluate the simultaneous impacts of all logic gates of the circuit at the same time. It is defined as

$$\begin{bmatrix} \Delta t_{p1} \\ \Delta t_{p2} \\ \vdots \\ \Delta t_{pn} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1m} \\ a_{21} & a_{22} & \cdots & a_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nm} \end{bmatrix} \cdot \begin{bmatrix} \Delta_{tp_1} \\ \Delta_{tp_2} \\ \vdots \\ \Delta_{tp_i} \end{bmatrix}. \tag{4}$$

For simplification purposes, eq. 4 and its matrices can be described trough component notation,

$$\mathbf{\Delta t_p} = \mathbf{J_n} \cdot \mathbf{x}, \tag{5}$$

where $\mathbf{\Delta t_p}$, $\mathbf{J_n}$ and $\mathbf{x}$ are composed of coefficients related to the delay induced-degradation, defined as the average gate delay induced-degradation for each stage evaluated, the normalized Jacobian matrix and the main impact caused by ΔV_T (i.e., the current stage impact), respectively. $\mathbf{\Delta t_p}$ describes the matrix evaluated to understand the induced-delay shift. Consequently, the coefficients of $\mathbf{J_n}$ and $\mathbf{x}$ must be defined.

It is pivotal to understand and use the results extracted from the two distinct simulations previously described in order to define the terms of the matrices. The graphical representation of the results is illustrated in Fig. 4.

Fig. 4 shows the generic behavior of a 22nm LP technology node [8] due to slope propagation. Firstly, the mean behavior of t_p without threshold voltage shift is plotted. Subsequently, a threshold voltage shift is applied to the CMOS inverter chain, producing the slope propagation effects (Δ_{tp_m}) through the subsequent gates. It was defined earlier that fluctuations of V_T – for this technology – cause the delay induced-degradation on the following two stages (in addition to the stage being directly impacted). In short, each node has to consider the slopes propagated from the last two stages, while the remaining stages are unaffected.

To characterize the terms of $\mathbf{x}$ it is necessary to define the higher impact caused in each stage, i.e., the main impact caused by ΔV_T at the evaluated stage. The main delay shift emerges at the evaluated stage (*n*). In the graph analysis, the main impact for the stage where the fluctuation is applied are equal to Δ_{tp_m}. Therefore,

$$\Delta_{tp_i} = \Delta_{tp_m}, \tag{6}$$

where Δ_{tp_m} is m-th impact produced by the slope propagation effects at each stage of a circuit.

The difference between the two simulations defines Δt_p as normalized term. The gate delay-induced degradation is normalized as a function of the observation window, which is approximated from the V_T shift. Additionally, the behavior of logic gates delay is assumed to follow a first-order linear system under which the highest value of its coefficients will be equal to 1 (the highest value will always be on the main diagonal). Therefore, to define the induced-delay coefficients – $\mathbf{J_n}$ coefficients –, the terms are also normalized as a function of the matrix $\mathbf{x}$ terms. Analytically, for the 22nm LP logic gate,

$$\begin{cases} a_{n1} = \Delta_{tp_{m-3}}/\Delta_{tp_1} \\ a_{n2} = \Delta_{tp_{m-2}}/\Delta_{tp_2}. \\ a_{n3} = \Delta_{tp_m}/\Delta_{tp_3} \end{cases} \tag{7}$$

Generically, for each logic gate of an integrated circuit, a_{nm} is defined as:

$$a_{nm} = \frac{\left(\frac{\partial t_{pn}}{\partial V_{Tm}}\right)}{\left(\frac{\partial t_{pn}}{\partial V_{Tn}}\right)} \approx \frac{\left(\frac{\Delta t_{pn}}{\Delta V_{Tm}}\right)}{\left(\frac{\Delta t_{pn}}{\Delta V_{Tn}}\right)}, \tag{8}$$

where it is evaluated the n-th stage delay variations caused by the V_T variabilities in the m-th stage, normalized by the n-th stage delay variations due to V_T variabilities in the n-th stage (defining the normalization factor, i.e., $\Delta t_p/\Delta V_T$). The highest impact (the main value of the Δ_{tp_m} term, defined by eq. 6) occurs when the indices *n* and *m* are both equal (that is, $n = m$, resulting in $a_{nm} = 1$).

The analysis presented in eq. 8 demonstrates that the derivative terms that describe the Jacobian matrices are evaluated through circuit simulations, approximated by the delay variabilities over threshold voltage shifts.

Furthermore, note that eq. 8 uses the criteria for normalizing the matrix coefficients once the results were characterized through the analysis of distinct simulations defined in Fig. 3. Owing to that, the delay coefficients have their values established due to variations of the threshold voltage (within an observation window, ΔV_T).

To estimate the delay variability, we use the propagation of uncertainty properties [15]. In component notation, the propagation of uncertainty for non-linear and correlated combinations in delay terms is defined as:

$$\sigma\mathbf{t_p^2} = \mathbf{J}\boldsymbol{\Sigma}^{\mathbf{V_T}}\mathbf{J^T}, \tag{9}$$

where $\sigma\mathbf{t_p^2}$, $\mathbf{J}$, $\mathbf{J^T}$ and $\boldsymbol{\Sigma}^{\mathbf{V_T}}$ are the gate delay induced-degradation variance matrix – assembling the variance of each stage (named σt_{pn}^2) –, the Jacobian matrix composed of denormalized delay coefficients, the transpose of the Jacobian matrix, and the variance-covariance matrix of V_T, respectively.

$\mathbf{J}$ was previously presented in its normalized form, $\mathbf{J_n}$, as shown in eq. 5. The term is rearranged through the normalization factor ($\Delta t_p/\Delta V_T$). Thus, $\mathbf{J}$ is defined as $\mathbf{J} = \mathbf{J_n}[\mathbf{x}/\Delta V_T]$ or in matrix notation:

$$\mathbf{J} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1m} \\ a_{21} & a_{22} & \cdots & a_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nm} \end{bmatrix} \cdot \begin{bmatrix} \Delta_{tp_1}/\Delta V_T \\ \Delta_{tp_2}/\Delta V_T \\ \vdots \\ \Delta_{tp_i}/\Delta V_T \end{bmatrix}. \tag{10}$$

In typical applications of propagation of uncertainties to circuit analysis, the correlations between the gates are neglected (i.e., assumed that they are independent). However, due to the characteristics of low-power and low-voltage devices, we cannot disregard this behavior since all logic gates are associated with each other and, consequently, their delay times are dependent due to the threshold voltage variabilities. As a consequence, we have to consider the variance-covariance matrix, expressed in terms of V_T, defined as:

$$\boldsymbol{\Sigma}^{\mathbf{V_T}} = \begin{bmatrix} \sigma_{11}^2 & \sigma_{12} & \cdots & \sigma_{1m} \\ \sigma_{21} & \sigma_{22}^2 & \cdots & \sigma_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ \sigma_{n1} & \sigma_{n2} & \cdots & \sigma_{nm}^2 \end{bmatrix}, \tag{11}$$

where $\boldsymbol{\Sigma}^{\mathbf{V_T}}$ describes the variance-covariance matrix of V_T. The matrix coefficients are the standard deviation (σ) and variance (σ^2) of V_T. If an applied V_T shift in one stage does not change the V_T of others (they only impact the gate delay), we can assume that this deviation will be present only at the current analyzed stage, which implies that all off-diagonal elements (i.e., σ_{nm} entries where $n \neq m$) of $\boldsymbol{\Sigma}^{\mathbf{V_T}}$ are equal to zero.

Once all terms are appropriately defined, eq. 9 can be expanded to its matrix notation,

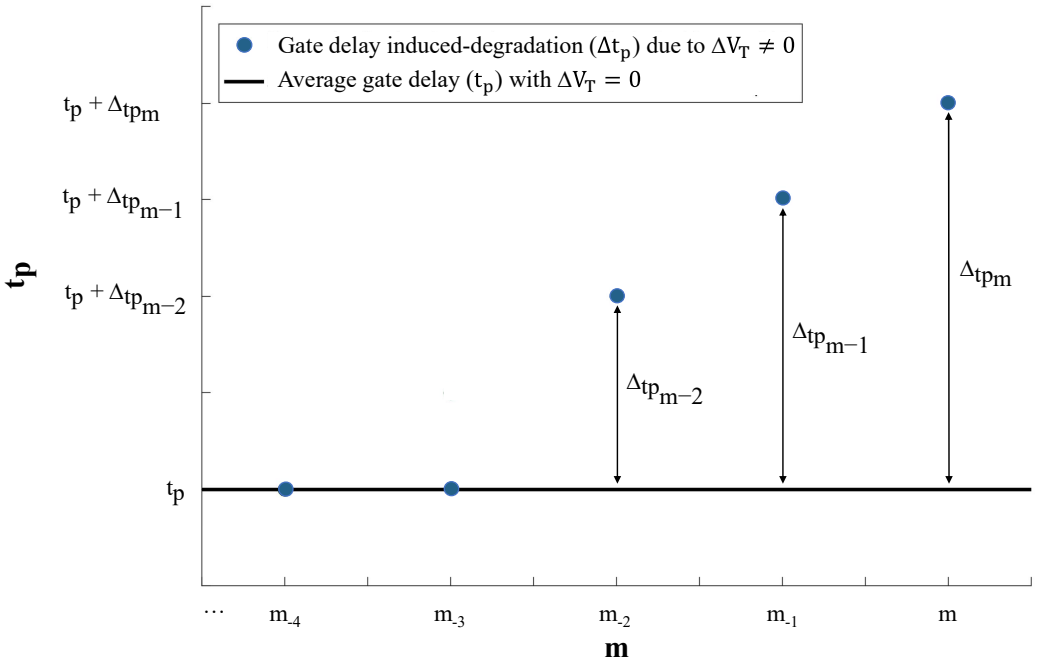

Fig. 4: Gate delay (t_p) as a function of the stages (m) that impacts the evaluated stage (n) due to slope propagation caused by the threshold voltage (V_T) variabilities. The Δ_{tp_m} terms define the delay induced-degradations as a function of V_T fluctuations, i.e., the slope propagation effects. The graph shows the generic behavior for a 22nm LP technology node [8].

$$\sigma\mathbf{t_p^2} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1m} \\ a_{21} & a_{22} & \cdots & a_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nm} \end{bmatrix} \cdot \begin{bmatrix} \Delta_{tp_1}/\Delta V_T \\ \Delta_{tp_2}/\Delta V_T \\ \vdots \\ \Delta_{tp_i}/\Delta V_T \end{bmatrix} \cdot \begin{bmatrix} \sigma_{11}^2 & \sigma_{12} & \cdots & \sigma_{1m} \\ \sigma_{21} & \sigma_{22}^2 & \cdots & \sigma_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ \sigma_{n1} & \sigma_{n2} & \cdots & \sigma_{nm}^2 \end{bmatrix} \cdot \left(\begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1m} \\ a_{21} & a_{22} & \cdots & a_{2m} \\ \vdots & \vdots & \ddots & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nm} \end{bmatrix} \cdot \begin{bmatrix} \Delta_{tp_1}/\Delta V_T \\ \Delta_{tp_2}/\Delta V_T \\ \vdots \\ \Delta_{tp_i}/\Delta V_T \end{bmatrix} \right)^T \cdot \tag{12}$$

As a result, eq. 12 returns a $n \times m$ matrix. To specify the total variability of $\mathbf{\Delta t_p}$ to each device, still, in matrix terms, the sum of the matrix $\sigma\mathbf{t_p^2}$ is performed, resulting in eq. 13,

$$\sigma\mathbf{t_p^2} = \sum(\mathbf{J} \cdot \mathbf{\Sigma^{V_T}} \cdot \mathbf{J^T}) = \begin{bmatrix} \sigma t_{p1}^2 \\ \sigma t_{p2}^2 \\ \vdots \\ \sigma t_{pn}^2 \end{bmatrix}, \tag{13}$$

where σt_{pn}^2 describes the variance of the n–th logic gate under which the behavior is evaluated. The total gate delay variance of each device considers only the variability of Δt_{pn} (eq. 2) since the variations are related to their behavior. Specifically, in eq. 1, the only term that shows deviations is Δt_{pn} – i.e., t_p is the mean value extracted without any degradation in V_T and does not change its value.

IV. Circuit Level Analysis

One of the most crucial tasks of ICs is to understand its time characteristics, especially its variabilities, under the fluctuations caused by aging mechanisms, such as BTI. In addition to these, there are also the slope propagation effects in low-power devices due to their sensitivity to process parameters deviations. Both behaviors have been analytically addressed at a device (logic gate) level, as shown from eq. 1 to eq. 13. Even so, we can extend this to a circuit level, using the techniques provided by the propagation of uncertainty to define the gate delay variability.

A. Circuit Level

Alongside the analytical model for device analysis, the characterization for the circuit evaluation can be easily defined. The model (as shown from eq. 1 to eq. 13) is established on gate delay coefficients, where all stages' behavior of a digital IC are evaluated simultaneously since all logic gates are correlated. This analysis implies that they cannot be studied considering only their behavior due to threshold voltage shifts but also the behavior of the previous devices. Thus, to define the induced-gate delay degradation and the variability of a circuit, it is only needed to apply the sum of all the coefficients that compose the matrices $\mathbf{\Delta t_p}$ and $\sigma\mathbf{t_p^2}$ (described in eqs. 5 and 9). Analytically,

$$\overline{\Delta t_p} = \sum(\mathbf{\Delta t_p}) \tag{14}$$

and

$$\overline{\sigma t_p^2} = \sum(\sigma \mathbf{t_p^2}), \tag{15}$$

where $\overline{\Delta t_p}$ and $\overline{\sigma t_p^2}$ are the average gate delay shift and the average gate delay variance of the circuits, respectively. The extracted results define the additional gate delay shift – and their variabilities – caused to the mean gate delay of the circuits, arising from the simultaneous variability of the devices and the degradation induced by the delay of the gates – due to the fluctuations of V_T. It is important to define that eq. 15 is a simplification that overestimates the jitter as it assumes that the gates' delay and the variance are uncorrelated, which is not true (the variability of one gate affects the variability of the following nodes). This simplification will define the overestimated results presented in section V.

B. Ring Oscillator Approximation

The model is characterized to estimate the behavior of any logic gate (device level) or integrated circuit (circuit level). For that, as the case study, it was chosen to demonstrate its applicability to approximate the behavior of a ring oscillator, built from CMOS logic inverters – employed as the elements at the device level analysis. As shown in Fig. 5, a 7-stage ring oscillator was chosen to test the methodology.

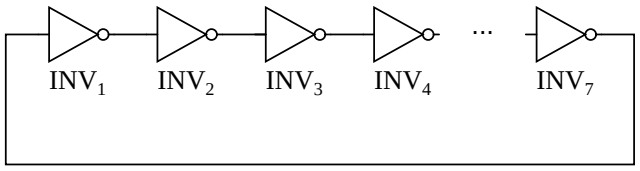

Fig. 5: 7-stage CMOS-based ring oscillator, with V_{DD} = 0.95V and $f \approx$ 2.2GHz. The ratio W/L is 44nm/22nm for the PMOS and 22nm/22nm for the NMOS devices, design with a 22nm PTM technology node for low-power applications, incorporating high-k metal gate and stress effect [8].

The use of oscillating circuits provides simplifications as their properties are employed. The analysis of the gate delay can also be used to approximate the oscillation period and its jitter due to the relationship between these metrics, defining the effects of the aging mechanisms in the oscillators.

Under the assumption that the effects of ΔV_T only affect the device itself and the next two adjacent states, as shown in Fig. 4, all the other coefficients in $\mathbf{J_n}$ – which represent the additional logic gates – will be equal to zero. Furthermore, the circuit we used for this evaluation is built with similar gates (CMOS inverters). Consequently, all logic gates have the same behavior. In mathematical terms, all the results that form the matrices $\mathbf{\Delta t_p}$ and $\mathbf{x}$ will be the same – the induced-gate delay of each gate is the same for all cases.

Thus, we can simplify eqs. 3, 4 and 5 to adjust to this estimation. By that, the normalized Jacobian matrix, $\mathbf{J_n}$, is defined as:

$$\mathbf{J_n} = \begin{bmatrix} a_{11} & 0 & 0 & 0 & 0 & a_{16} & a_{17} \\ a_{21} & a_{22} & 0 & 0 & 0 & 0 & a_{27} \\ a_{31} & a_{32} & a_{33} & 0 & 0 & 0 & 0 \\ 0 & a_{42} & a_{43} & a_{44} & 0 & 0 & 0 \\ 0 & 0 & a_{53} & a_{54} & a_{55} & 0 & 0 \\ 0 & 0 & 0 & a_{64} & a_{65} & a_{66} & 0 \\ 0 & 0 & 0 & 0 & a_{75} & a_{76} & a_{77} \end{bmatrix}, \tag{16}$$

where all seven logic gates' variabilities are evaluated, considering the cross effects caused to all gates of the circuit. It is important to note that the coefficients from $\mathbf{J_n}$ will be the same but shifted one term. Moreover, the closest the gate is to the gate where the impact was applied, the higher will be the delay coefficient.

Since $\mathbf{J_n}$ was described, the gate delay estimation (eq. 14) and its variability (eq. 15) can be defined. Following this, the oscillation period (T) of the ring oscillator, taking into account the propierties of low-power devices (eq. 1), is written as:

$$T = 2 \cdot (t_p \cdot i + \overline{\Delta t_p}), \tag{17}$$

where i, t_p and $\overline{\Delta t_p}$ are the number of the ring oscillator stages, the average propagation delay without any shift in the threshold voltage and the average gate delay shift evaluated by eq. 14, respectively. While the oscillation period variability (σ_T), through the propagation of uncertainty properties, is given by

$$\sigma_T^2 = \left(\frac{\partial T}{\partial \overline{\Delta t_p}}\right)^2 \cdot \overline{\sigma t_p^2} \tag{18}$$

or, through its simplification,

$$\sigma_T = \sqrt{4\overline{\sigma t_p^2}}, \tag{19}$$

where $\overline{\sigma t_p^2}$ is the average gate delay variance of the circuit evaluated by eq. 15. The simplifications presented from eq. 16 to eq. 19 are only valid for ring oscillators. Despite that, the derived model (eq. 1 to eq. 15) is suitable for different logic gates and circuit analyses. Both CMOS inverters and ring oscillators are used as a case study to demonstrate the applicability of the proposed model.

V. Results and Discussion

To the best of our knowledge, no data or similar works – performed under similar conditions to the ones proposed here – were found. Thus, two methods were used as comparison, validation, and demonstration of the improvements driven by the derived model. The comparisons were fairly defined, aiming to keep the same characteristics and assumptions for each approximation setup (detailed below). To validate the approximations, Monte Carlo simulations were performed. To demonstrate the improvements, the simplified technique of propagation of uncertainty was used.

Both comparisons, as well as the approximation with the proposed model, include in the simulations the BTI average impact [3] as a mechanism of threshold voltage fluctuation. The aging effect was extrapolated (in a short time of analysis) so that the BTI consequences are employed to illustrate the derived model. The simulations performed in our study were implemented using a hardware with 4GB RAM system memory, 500GB HDD and an Intel® Celeron® 1.10 GHz processor.

A. *Monte Carlo Simulations*

A thousand (1000) MC runs of the ring oscillator illustrated in Fig. 5 were performed only to validate the results evaluated by the model at the circuit-level analysis. For that, a Gaussian-distributed function was taken to induce a sequence of random values for V_T adopting a nominal value to consider the BTI average impact [3] and assuming a $20mV$ standard deviation of V_T. Though the MC method provides a very accurate description of the statistical quantities, it requires significant computational effort through thousands of simulations.

B. *Propagation of Uncertainty Simplification*

To reduce the MC computational cost, statistical techniques are employed to approximate the circuits from a single part that composes them. The propagation of uncertainty is one of these methods, and is used in two ways: in its simplified technique – which does not consider that the gates of a circuit are correlated – and in its complete form that consider the correlations – used in the model derivation.

In the simplified propagation of uncertainty technique, the Δt_{pn} is assumed to be equal to zero. In short, this implies that the stages are not correlated, and each gate is independent of the others. The approximation demonstrates that the effect of Δt_p (especially for low-power devices) should not be disregarded. The simplified methodology is adapted from [15] to the oscillation period analyses of the circuit (through the analysis of eq. 17, with $\overline{\Delta t_p} = 0$). It is assumed a $20mV$ standard deviation of V_T and a $5mV$ observation window ΔV_T.

C. *Analytical Model*

To finish the data analysis, the model proposed in this work is employed. The characterization is defined from eq. 1 to eq. 19 and the graphical analysis, adopting a $20mV$ standard deviation of V_T and a $5mV$ observation window ΔV_T.

The following subsection presents a detailed description of the methods used to estimate the integrated circuit, followed by a comparison and discussion of the results.

D. *Discussion*

The analysis at the circuit level of the oscillation period and its jitter is defined, allowing the investigation of the circuit behavior through the proposed analytical method (the focus of this work) toward the BTI impact. The estimated results shown in Figs. 6 and 7 are the oscillation period (T) and the jitter (σ_T) of a ring oscillator as a function of time on a log x-axis scale, respectively.

It is seen in Fig. 6 that the BTI degradation effects are smaller when lower stress times are considered. Thus, T increases (the device becomes slower) as the impact of BTI in V_T increases (which is a time-dependent term [3]). This result is already expected once the oscillation period is directly related to the threshold voltage variability (i.e., the higher the V_T, the higher becomes the period). The estimated jitter (or variability) is also studied, where a behavior similar to T is seen in Fig. 7. In other words, not only does T increase with BTI degradation but also the oscillation period jitter σ_T. For both cases, the simplified technique of propagation of uncertainty results in an underestimated approximation of the circuit behavior.

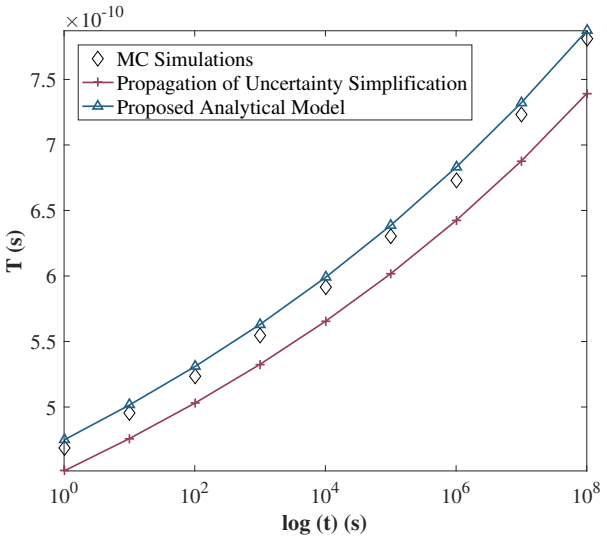

Fig. 6: Estimated oscillation period (T) of a ring oscillator, compared to MC simulations and common propagation of uncertainty simplification.

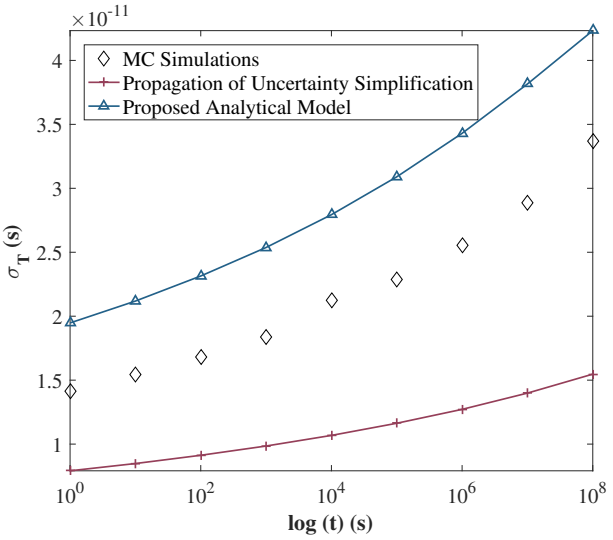

Fig. 7: Estimated oscillation period variability (σ_T) of a ring oscillator, compared to MC simulations and common propagation of uncertainty simplification

The approximation error can also be estimated and compared to demonstrate the improvements of the proposed analytical model. The approximations (the propagation of uncertainty simplification and the derived model) are compared with the validation data (MC simulations) and presented in Table I.

For T, the worst value found with the analytical model is 1.5163% against the 5.3778% estimated with the propagation of uncertainty in its simplest form. For σ_T, where all discrepancies are amplified, the values are 27.5051% (analytical model) versus 54.0871% (propagation of uncertainty simplified form). The period jitter analysis (originated from eq. 15) presents overestimated values – i.e., higher than the MC data, as shown in Table I and in Fig. 7 – due to the simplifications assumed in the derivation of the equation.

Table I.: Approximation error data for the oscillation period (T) and period variability (σ_T) at each time decade evaluated compared to Monte Carlo simulations.

	Oscillation Period Approximation			
	Propagation of Uncertainty Simplification (%)		**Analytical Model (%)**	
Time (s)	$\mathbf{T}$	$\sigma_{\mathbf{T}}$	$\mathbf{T}$	$\sigma_{\mathbf{T}}$
1E+00	3.7515	43.9615	1.2710	27.4931
1E+01	3.8926	44.9818	1.2639	27.2365
1E+02	3.8879	45.7325	1.4217	27.3402
1E+03	3.9570	46.4482	1.5163	27.5051
1E+04	4.3866	49.6843	1.2582	24.0270
1E+05	4.5374	49.1012	1.2999	26.0519
1E+06	4.5174	50.2250	1.5047	25.5139
1E+07	4.9139	51.5049	1.2223	24.4101
1E+08	5.3778	54.0871	0.7561	20.3940

The results show that the model is a proper structure to analyze the behavior both at a device and circuit level, significantly reducing the jitter approximation errors by up to 50% for each decade when the simplified method is applied for the same objective.

The simulation time was also reduced. While the MC simulations are computationally time-consuming, given the number of simulations executed, the proposed model relies on quick and easy simulations. For the extraction of validation MC data, each stress time condition took 30 minutes to run – the total analysis takes 4.5 hours to estimate the aging behavior of a simple ring oscillator. In contrast, the proposed model simulation is performed in 10 seconds for each stress time – the total analysis depends on an average of 1.5 minutes.

The model tendency to present overestimated values is based on the propagation of uncertainty and sensitivity analysis properties, assuming that the gate delay (or oscillation period) is linear around a specific point and, even though it is a widely used approximation, it is not the exact behavior. For the jitter approximations, the significant discrepancies are related to the sum of the variances (eq. 15) that disregards the covariance between the gates delay and the association with parameters whose behavior is also defined through linear estimations.

As a rule of thumb, the equations derived can be used for any other devices, regardless of the technology node they are built. However, they are best suited for low-power and low-voltage design analysis, where the degradation of one stage may significantly affect the performance of the following stages due to slope-induced degradation of the gate delay.

VI. Conclusion

In this work, an analytical model was presented to evaluate the logic gate delay and oscillation period of low-power and low-voltage devices. The proposed method adopts linear systems and propagation of uncertainty alongside sensitivity analysis properties, considering the low-power devices' high sensitivity to process parameters variations; the gates signals slopes that propagate over the circuit; and the BTI degradation as a time-dependent source of threshold voltage fluctuation. It is demonstrated that the properties of low-power devices enhance the slope propagation effects on the logic gates. Not only the average value was estimated through the derived equations, but also the variability, providing a good estimative for the parameters' degradation. The results – supported by MC simulations – demonstrate that BTI degradation causes both the oscillation period as well as period variability to increase. The obtained results show that the proposed model predicts the circuit's behavior by reducing errors – in the best-case – in 85% and 62%, respectively, for the oscillation period and its jitter when the widely employed and simplified propagation of uncertainty method is applied for the same objective. One of the leading advantages of the presented model is to avoid the computational cost of MC simulations. The time analysis is downsized from extended hours to minutes to perform the simulations of a ring oscillator.

Finally, in future works, an improvement in the approximation of the gate delay variance will be derived to reduce the results' overestimation, evaluating the covariance between the gates' delay.

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