A Machine Learning Based Reliability Analysis of Negative Bias Temperature Instability (NBTI) Compliant Design for Ultra Large Scale Digital Integrated Circuit

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Abstract— **NBTI is a key reliability challenge in nanoscale digital design, and it is vital to address it throughout the exploration of design space at high levels of abstraction in order to improve reliability. A prediction model of aging that is adequate for these levels ought to be faster. In addition to this, the model should be able to forecast the recently discovered stochastic consequences of growing older. The purpose of this study is to offer a model that is based on machine learning (ML) and can predict aging effects. After obtaining a training set of sufficient size using Synopsis HSPICE (MOSFET Reliability, MOSRA) in the beginning, the machine-learning-based model is then trained and built in order to forecast the aging statistical features. Evaluation is done on a number of machine learning techniques, including Adaptive Neuro-Fuzzy Inference System (ANFIS), K-Nearest Neighbor (KNN), Support Vector Machine (SVM) and Random Forest (RF). The findings indicate that ANFIS algorithms are very effective in the process of age prediction. The proposed technique shows that the aging prediction runtime is reduced by more than 99% when compared to the MOSRA-based approach, and accurate predictions of the statistical properties of aging are obtained with an accuracy of more than 99% on complementary metal oxide semiconductor (CMOS) and metal gate/high-K (MGK) circuits at the 22nm technology node.**

Index Terms— **Reliability, HSPICE, NBTI, CMOS, Metal Gate High-K**

I. Introduction

A. Background

In the design flow of contemporary digital circuits, the analysis and lifespan optimization of nanoscale digital systems have emerged as key necessities. This has come about as a direct result of recent developments. Reliability effects may be either spatial or temporal, and they can cause circuit to fail. The term ”spatial effects” refers to concerns about fabrication-induced reliability that arise as a consequence of the increasing complexity necessary for manufacturing nanoscale CMOS circuits. These days, the term ”VLSI technology” may refer to more than just CMOS technology. The manufacturer has access to a wide variety of alternative transistor choices, such as MGK. When it comes to replacing the CMOS technology used in electrical circuits, MGK is one of the options. With a shorter propagation delay and less power loss, an MGK transistor is able to perform better [1]- [2].

In reliability variations, the performance of the circuit diminishes over some time period, and this impact is also known as the aging effect [3]- [4]. When evaluating the performance of the circuit, reliability is a key performance metric to look at. After a certain amount of time, the aging effect can be used to predict how well the circuits will work [5]. The two effects of aging are known as NBTI and positive bias temperature instability (PBTI). NBTI is associated with the p-type metal oxide semiconductor (PMOS), while PBTI is more closely associated with the n-type metal oxide semiconductor (NMOS) transistor. The authors of this article focus their attention on NBTI degradation because, in comparison to PBTI, the influence of NBTI on the performance of a circuit degrades more significantly with time. The scaling of gate oxide thickness faster than the operating voltage, which raises the field and produces NBTI degradation, is the primary source of the influence that NBTI has on the performance of a circuit. The presence of nitrogen helps to limit the amount of boron that penetrates the gate dielectric of the transistor, which in turn helps to reduce the amount of gate leakage that occurs [6]. This has the effect of increasing the influence that NBTI has on the transistor. When it comes to the NBTI impact of the circuits, the stress state of the circuits plays a very significant role. The NBTI effect is triggered whenever a negative voltage is supplied to the gate terminal of a PMOS transistor. This results in the formation of interface traps at the oxide interface of the transistor [7]. The biasing state of the transistor is a significant contributor to the formation of interface traps as well as the intensification of the NBTI effect. There are a few distinct ideas that attempt to explain the connection between NBTI deterioration and PMOS transistors. There are three physical explanations that explain the genesis of the NBTI effect in VLSI design. Fig. 1 presents the various physical models [8]- [9].

B. Impact of NBTI on system performance

The impact and behavior associated with aging were first noticed in the 1970s. Since then, a great deal of research has been carried out to identify them.

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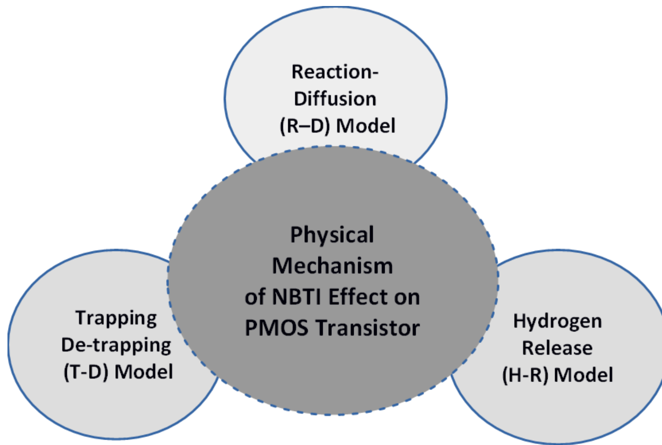

Figure 1: Physical models for NBTI effect

These investigations served as the foundation for the development of effective models that are connected to the aging process. At first, the models projected that the aging-induced deterioration of circuit delay would be a predictable function of operational parameters such as signal probability and temperature. The size of the components, however, continued to decrease, which resulted in the appearance of stochastic behaviors in the aging effects of the circuits. This implies that two absolutely identical transistors may exhibit differing rates of aging even when subjected to the same working circumstances.There are a variety of approaches that have been suggested to combat the negative impact that aging has on the performance of circuits [10].
In the beginning, the majority of aging optimization algorithms concentrated on low levels of abstraction, which are situated very near to the actual physical cause of transistor aging. Due to the fact that a good knowledge of the processes of aging is already accessible, it is possible to construct efficient models for forecasting and assessing the severity of aging at these low levels [11]. Because of the complexity of creating contemporary systems, designers began to focus their attention on higher levels of abstraction over time. This led to a change in the paradigm that governs the design of sophisticated digital systems. Reliability, which presents a significant problem in this age of nanoscale digital circuits, have to be taken into consideration from the very beginning stages of the design process. However, transistor-level models, which are used for assessing and forecasting the aging of electronic circuits, are not suited for usage at high levels of abstraction owing to the fact that they need a significant amount of time to execute and are complicated. In addition to this, the impacts of aging on new technology nodes are stochastic; hence, aging models need to be revised in order to be able to forecast the behaviors associated with these stochastic effects [12]- [14].
Using a variety of models, the researchers are determining how sensitive the electronic devices are to their surroundings [15]- [17]. When a negative bias voltage is supplied to a PMOS transistor, a positive ion will travel toward the gate. This will result in a decrease in the total amount of positive charge near the SiO_2 interface, which will lead to a positive flat band shift. By applying a constant negative voltage to PMOS devices, one of two phenomena can take place at the Si-SiO_2 interface: hole trapping or electron de-trapping. This phenomenon is caused by an increase in the net positive charge in MOS devices, which in turn results in a negative band shift. The R-D and T-D models both provide an explanation of the whole process that these ideas entail. Because of the negative gate voltage, NBTI causes interface traps to form in MOS devices at higher temperatures, as well as a positive oxide charge. The gate charge capacitance, which includes both drain-source and drain-gate capacitance, shifts in response to shifts in the stress temperature and timing circumstances . These shifts are caused by variations in the devices' physical properties [18]. Variations in process parameters are a significant problem that has to be addressed in the ULSI sector, and in the long term, improvements in the reliability of electronic devices are anticipated [19].
This complexity arises as a result of aggressive scaling at the atomic scale. Temporal effects, which are observable while the circuit is operating, may either be permanent or fleeting in nature. For instance, temporary mistakes are caused by soft errors that are created by cosmic rays. Techniques that can protect circuits from being damaged by soft mistakes are now the subject of intensive research because of how important they are. The effects of aging on the components of a circuit may often have long-lasting repercussions for the circuit's reliability [20]. One common example of this is accelerated transistor aging. After the manufacturing of circuits and the beginning of their operation, the effects of aging are detected on the behavior of circuit components as run-time deviations from their ideal behavior. Because of the electron migration phenomenon, interconnects eventually wear out. In addition to this, transistors are susceptible to the effects of aging. When making new nano-sized digital systems, the effects of aging transistors put a lot of limits on what can be done and create a lot of problems.The behaviors that cause transistors to age include time-dependent dielectric breakdown (TDDB), negative bias temperature instability, and hot carrier injection (HCI), with NBTI being one of the most significant mechanisms of transistor aging. The switching delay of the transistors and, therefore, the delay of the combinational pathways are both increased by NBTI. In the end, the circuit blows up because of a timing violation [21].

In this article, a model is given that is good for high levels of abstraction, like that can be used to predict how badly circuits will break down as they age. The model's ability to provide accurate results while having

a very quick runtime is its most important feature. As a result, it is appropriate for high degrees of abstraction, in particular the exploration of design space.

C. Transistor level aging prediction at lower technology nodes

When a PMOS transistor has a negative gate-source voltage applied to it, a phenomenon known as NBTI may be seen. The threshold voltage of a MOSFET transistor will decrease as a result of NBTI effects when the transistor switches on. The term for this stage is the "stress phase." The NBTI effect enters the recovery phase when the transistor is switched off. During the recovery phase, the decrease in threshold voltage is somewhat compensated. However, the recovery rate does not keep pace with the deterioration rate, and as a result, the threshold voltage of the transistor rises after a series of successive stress and recovery phases (this phenomenon is referred to as dynamic BTI), as seen in Fig. reffig:2.

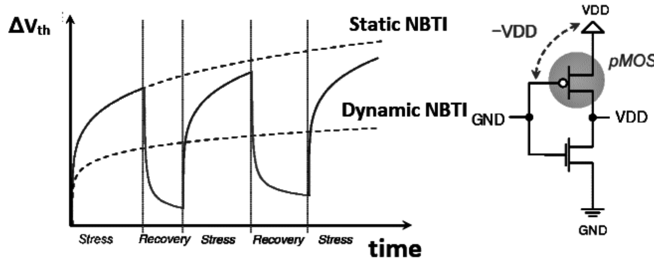

Figure 2: Static and Dynamic NBTI

This gradual decrease in threshold voltage is a function of the duty cycle of the input signal, which is also referred to as the signal probability. Eq. 1 [11] is the formula that deterministically calculates this value.

$$\Delta V_{th} = \left[\frac{\sqrt{K_v^2 \alpha t_{clk}}}{1 - \beta_t^{-2n}} \right]^{2n} \tag{1}$$

The constant K_V in the equation above is depending on the technology being used, α is the signal probability. The t_{clk} symbol denotes the clock period. Also, β_t is determined by the specifications of the technology as well as the signal probability, and n is a constant that is either one quarter or one sixth, depending on the technology. The condition known as static BTI occurs when a transistor is subjected to an unchanging strain with duty cycle equal to 1. The static BTI impact has a greater severity when contrasted with the dynamic BTI due to the fact that continual stressing is applied and there is no opportunity to recover from the deterioration in the static NBTI, as seen in Fig. 2. The formula for figuring out how much the static BTI causes the threshold voltage to drop is as follows [11]:

$$\Delta V_{th} = A \left[(1+\delta) t_{ox} + \sqrt{ct} \right]^{2n} \tag{2}$$

where A and C are constants that change depending on the technology, t_{ox} is the thickness of the oxide, t is the entire stress duration, and n factor is equivalent to either one-fourth or one-sixth. The value of δ which is a constant, is equal to 0.5.The equations shown above hold true for older technology nodes, which have a situation in which the effects of NBTI on relatively big transistors are rather predictable.

The quantity of threshold voltage change in today's world of deep nanoscale technologies is stochastic and needs to be explained by statistical distributions.The charging of individual defect traps that already exist in the gate oxide causes the threshold voltage to rise during the stress phase, while the discharging of these traps causes the threshold voltage to fall during the recovery phase, which results in compensation for the degradation that occurred during the stress phase. The process of charging and discharging these traps is a stochastic one, which means that on the one hand, the number of traps in individual transistors in advanced technology nodes is relatively low (proportional to the decreasing gate area), and on the other hand, the number of traps is proportional to the decreasing gate area. Therefore, a significant time-dependent variation in the NBTI effects may be seen in these deeply scaled devices and, therefore, in the circuit lifespan [22].

The atomic trap-based model [13] uses the characteristics of each transistor to explain the stochastic behavior of BTI effects. These characteristics are as follows: the parameters n which is the number of faults, c which is the time it takes to capture defects, and e which is the defect emission time. Voltage and temperature are two of the factors that affect these time constants. The capture/emission time (CET) maps [14] are used to establish the probability density function (PDF) of widely dispersed defect capture and emission times as well as their correlations. These maps may also be used to visualize the data. When the CET map is integrated throughout the whole of the time domain, the defect density (per unit area) of all of the accessible traps may be calculated. As a consequence of this, the formula for calculating the typical number of flaws, n, in a transistor with the dimensions W and L is as follows [13]:

$$n = N_{TD}.W.L \tag{3}$$

Only a small portion of the available traps will be used and contribute to the deterioration of the threshold voltage, depending on the signal probabilities. The probability of trap occupancy, designated by the acronym P_{OCC} may be calculated as a function of the frequency (f), duty factor (d), and total duration (t), according to the following equation. The time it takes for faults to emit themselves is denoted by the variable τ_e, while the time it takes for them to be captured is denoted by τ_c [14].

$$P_{OCC} = \frac{1 - e^{\frac{-\alpha}{f \tau_c}}}{1 - e^{\frac{-X}{f}}} \left(1 - e^{-tX}\right) \tag{4}$$

$$X = \frac{\alpha}{\tau_c} + \frac{1-\alpha}{\tau_e} \tag{5}$$

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It is not difficult to calculate the ratio of active traps over total traps, which is symbolized by the symbol ρ (and corresponds to the signal probability that is being applied) written as [14]:

$$\rho = \frac{\int\int f(\tau_c, \tau_e) P_{OCC}(\tau_c, \tau_e, \alpha, t, f) d\tau_c d\tau_e}{\int\int f(\tau_c, \tau_e) d\tau_c d\tau_e} \quad (6)$$

Then, given a specific device and stress waveform, it is easy to get the mean value of occupied traps, n_T, by multiplying the average number of traps that are available in that device (n), multiplied by the percentage of total traps that are occupied (T); There is a certain amount of threshold voltage degradation that is contributed by each occupied trap. Experiments may be done to figure out how much of an effect flaws have on average, which is symbolized by the symbol η. The total cumulative distribution function of change in threshold voltage can be calculated as [14]:

$$H(\Delta V_{th}) = \sum_{i=0}^{\infty} \left[\frac{e^{-n_T} n_T^i}{i!} \left[1 - \frac{i}{i!} \Gamma(i, \frac{\Delta V th}{\eta}) \right] \right] \quad (7)$$

It is possible to utilize this distribution to describe the aging characteristics of transistors. The remaining parts of the paper are structured as follows: In Section 2, we provide examples from the research that has been done on how to lessen the negative effects of NBTI. In Section 3, the fundamentals of reliability analysis through HSPICE MOSRA is discussed. The proposed work is presented in section 4, details of experimental setup is described in Section 5, the obtained results are explained in section 6 and the entire work is concluded in section 7.

II. Techniques for mitigating the negative effects of NBTI

NBTI is a phenomenon that can degrade the performance and reliability of transistors in modern microprocessors. Here are some examples of research that have explored ways to mitigate its negative effects:

1. Gate Stacking Techniques: Gate Stacking Techniques are used to mitigate the NBTI effect in MOSFETs. NBTI is a reliability issue that occurs due to the buildup of interface traps in the gate oxide of the MOSFET, which causes a shift in the threshold voltage and a reduction in the device's performance. One of the most effective gate stacking techniques is the use of high-k dielectrics instead of conventional SiO2 gate dielectrics. High-k dielectrics have a higher dielectric constant than SiO2, which allows for a thicker gate oxide layer and reduces the electric field at the interface between the gate oxide and the channel, thus reducing the impact of NBTI. Several studies have reported on the effectiveness of gate stacking techniques in mitigating NBTI. For instance, a study by [23] showed that the use of high-k dielectrics reduced the NBTI degradation in MOSFETs compared to conventional SiO2 dielectrics. Another study by [24] also reported that using a gate stack with a SiO2/HfO2 dielectric layer reduced the NBTI degradation in MOSFETs compared to a conventional SiO2 gate stack.

2. Bias Temperature Stressing: Bias Temperature Stressing (BTS) is a commonly used technique to mitigate NBTI in metal-oxide-semiconductor field-effect transistor (MOSFET) devices. NBTI is a reliability issue that can lead to a decrease in device performance and lifetime, particularly in pMOSFETs. BTS involves subjecting the MOSFET device to a specific bias and temperature condition for a certain period of time, which helps to recover the threshold voltage shift caused by NBTI. The recovery mechanism is believed to involve a combination of charge trapping and detrapping, and the specific bias and temperature conditions used in BTS can vary depending on the device design and technology. Several studies have demonstrated the effectiveness of BTS in mitigating NBTI in MOSFETs. For example, a study by [25] found that BTS at a temperature of 125°C and a gate bias of -1V for 10 hours can recover up to 90% of the threshold voltage shift caused by NBTI in pMOSFETs. Another study by [26] demonstrated that BTS at a temperature of 150°C and a gate bias of -0.5V for 30 minutes can significantly improve the NBTI reliability of advanced pMOSFETs.

3. Process Optimization: Researchers have also studied the impact of process optimization on NBTI. For example, using thinner gate oxide and reducing the number of dopant atoms in the gate oxide can help to reduce NBTI effects. One study published in the Journal of Applied Physics in 2015 [27], investigated various techniques for mitigating NBTI degradation in advanced CMOS devices. The authors found that optimizing the gate oxide thickness, using high-k gate dielectrics, applying stress engineering techniques, and temperature cycling were effective methods for mitigating NBTI. They also found that applying a positive bias stress to recover the threshold voltage can be an effective method for mitigating NBTI.

4. Device Structure Modification: Device structure modification can also help mitigate NBTI. Researchers have explored the use of strained silicon, which can improve the transistor's performance while reduc-

ing the effects of NBTI. One approach to modify device structure is through the introduction of high-k dielectric materials in the gate stack, which can improve the device's immunity to NBTI. A study by [28] investigated the impact of high-k dielectric materials on NBTI in p-type metal-oxide-semiconductor field-effect transistors (pMOSFETs). The authors found that introducing hafnium oxide (HfO2) in the gate stack significantly reduced NBTI degradation in pMOSFETs, compared to traditional silicon dioxide (SiO2) gate dielectric. Another approach to mitigate NBTI is through the introduction of stress engineering techniques, such as strained silicon or silicon-germanium (SiGe) channels, which can enhance carrier mobility and improve device performance. A study by [29] investigated the impact of strained SiGe channels on NBTI in n-type metal-oxide-semiconductor field-effect transistors (nMOSFETs). The authors found that introducing strained SiGe channels reduced NBTI degradation in nMOSFETs, compared to conventional silicon channels.

5. Circuit Design Techniques: Circuit design techniques such as voltage scaling, dynamic voltage and frequency scaling, and power gating can also help to reduce the impact of NBTI on microprocessor performance and reliability. One of the most effective techniques is Bias Temperature Instability (BTI) stress mitigation, which involves applying voltage and temperature cycling to the pMOS devices to minimize NBTI. In [30], the authors proposed a technique called "Complementary Stressed Voltage (CSV)," which uses voltage stress on both nMOS and pMOS devices to reduce the BTI stress on the pMOS devices. The technique was shown to improve the lifetime of digital circuits by up to 2x. Another technique is to use transistor sizing to balance the stress between pMOS and nMOS devices. In [31], the authors proposed a technique called "Bias-Flip," which involves swapping the pMOS and nMOS transistors in a circuit to balance the NBTI stress. The technique was shown to improve circuit lifetime by up to 80%. Additionally, there are techniques that involve voltage scaling and gate oxide thickness tuning. In [32], the authors proposed a technique called "Adaptive Voltage Scaling (AVS)," which adjusts the supply voltage based on the circuit activity to reduce NBTI stress. The technique was shown to improve circuit lifetime by up to 3x. In [33], the authors proposed a technique called "Dynamic Gate Oxide Thickness (DGOT)," which uses a dynamically tunable gate oxide thickness to reduce NBTI stress. The technique was shown to improve circuit lifetime by up to 50

III. Reliability analysis through MOSRA

Changes in the circuit parameters have a significant impact on the performance of the circuits over a long period of time. During the fabrication process, an accurate forecast of these deviations is necessary [34]-[37]. Several different electronic design automation (EDA) tools are used to conduct an analysis of the effects of various parameter modifications. The researchers face a number of difficult challenges, one of the most significant being keeping the circuits' efficiency and reliability intact. It is important to have a low failure rate of the devices during the lifespan of the circuit. The most significant breakdowns in the circuits may be classified into three distinct phases. The device lifespan, including the points at which failure occurs, is shown in Fig. 3. Most of the time, devices break down after they are sent to customers [38]. Failures in early life are caused by defects that were not identified during the testing. Hence, these failures are unavoidable. Failures in early life may arise throughout the fabrication process, but the designers may not be able to discover them while the product is being tested. The primary goal of the circuits is to function within the operational range that was chosen for the reliability simulation throughout the useful working lifespan stage. Conditions of excessive thermal stress are the primary cause of catastrophic breakdowns throughout this period. Failures are caused by electrical stress at the last stage of end-of-life (EOL), which alters the properties of the devices and ultimately leads to their failure [39]. The applications of the devices in a certain area determine the level of reliability and stability that can be expected from them. The designers of automobiles anticipate far longer lifetimes than those of typical consumer applications. The VLSI industry has developed a large number of simulators in order to investigate the effects of aging on electrical devices. Within the scope of this work, the HSPICE Synopsys tool is being used [40]- [41]. The MOSRA flow may be broken down into two distinct phases: the pre-stress simulation phase and the post-stress simulation phase, respectively (Fig. 4). The two simulation stages can be done on the simulator either at the same time or one at a time, depending on what is needed.

Figure 3: Failure stages during the device lifetime

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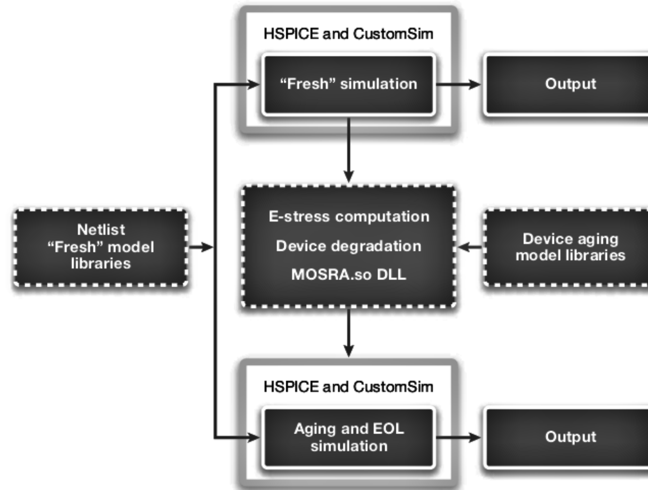

Figure 4: Reliability simulation in HSPICE

During the pre-stress phase (also known as the "fresh" simulation phase), the simulator uses the MOSRA models to compute the electrical stress that will be placed on user-selected MOSFETs in the circuit. The computation is based on the circumstances of the electrical simulation for each device that is being targeted. During the course of the MOSRA transient analysis [42], the value of the stress derived from the MOSRA equation is integrated across a user-specified simulation time frame. The result is then extrapolated to calculate the total stress after the amount of time that the user has specified (circuit has been operating i.e. age). After that, the overall quantity of electrical stress is converted into a performance degradation of the device using the MOSFET aging models. In addition to the built-in model of aging that is described in this article, it is also possible to use models that are based on user specifications by way of a MOSRA application programming interface (API). A second simulation will begin when the post-stress phase has concluded. At this stage, a drop in the performance of the circuit is caused by a drop in the performance of the devices. In the HSPICE MOS reliability simulator, determining the effect that NBTI has on transistors can be done using either of two methods. Within the simulator, the two-way simulation approach is used quite frequently. In this method, the circuit illustrates the device's deterioration through the use of two distinct output waveforms: fresh and aged. The results of a fresh simulation show the output without any stress, while the results of an aged simulation show the difference in performance after a certain amount of time has passed.

IV. Proposed Work

A. Problem definition

The effects of aging on circuits are seen as an increase in their latency as the circuits age. Because of this, the severity of aging in a circuit may be determined by the growing delay of the circuit over time by including the effects of aging into various techniques for timing analysis. Simulations of the timing at the transistor level are precise but exceedingly time-intensive. In addition to this, the simulation has to be run several times for each newly created signal probability. As a result, these techniques are not relevant to the design of massive digital circuits. For the purpose of evaluating large circuits, aging-aware static timing analysis (STA) based techniques are a potential solution because of the small amount of time required for their execution. Utilizing nanoscale transistors has made it feasible for companies to produce sophisticated systems on a chip (SoCs) in recent years. There has been a paradigm shift in digital design flow that has evolved in order to boost design productivity. This movement places a larger focus on higher degrees of design abstraction. As a direct consequence of this, computer-aided design (CAD) systems now extensively enable design techniques that are based on high-level synthesis (HLS) algorithms. HLS investigates the design space by using procedures like scheduling and binding [43]. Because of the growing significance of rapid transistor aging, it is important to consider the lifespan of circuits in the early phases of the design process. To accomplish this:

1. Aging prediction models need to be fast enough for efficient exploration of the design space.
2. The stochastic nature of nano-sized transistor aging effects needs to be included in the analysis of circuit life.

B. ML based aging prediction model

The delay in a circuit grows with time as a direct result of the aging of the transistors. The rate of delay deterioration in relation to the zero-time (fresh) delay is referred to as the "aging rate" (or simply "aging" for simplicity's sake):

$$\%aging = \frac{Delay(aged) - Delay(new)}{Delay(new)} \tag{8}$$

Here, Both the new gate delay and the aged gate delay are denoted by the symbols D(new) and D(aged) respectively. A variety of different factors, such as the nature of the signal probability i.e. signal probability, the effective temperature, and the supply voltage, all contribute to the formation of the aging delay [44]. The signal probability of a multi-input device may be characterized by a vector of the signal probabilities of the many individual input signals. The aging rate should be expressed as a statistical effect using a probability distribution for deep-nanometer transistors. This distribution should have a mean value and a standard deviation. The HSPICE MOS reliability Analysis (MOSRA) tool is used to do the calculations necessary to simulate the reliability of a wide variety of logic gates. This is the reliability simulator that is set as the default in Synopsys, and it offers a high level of performance for complicated circuits. The authors are designing their circuits using the PTM 22nm model for CMOS and the MGK PTM 22nm model. Table I is an illustration of the fundamental simulation parameters that authors are employing in the design of their simulations. At room temperature, simulations of several CMOS and MGK circuits are run while the supply voltage for both CMOS and MGK is set to 1 volt.

C. Estimation Models Based on Machine Learning

Because of their high level of effectiveness, ML approaches are quickly gaining popularity in the field of digital design and the associated CAD tools. In this part, it will be shown that ML regression models are capable of providing a quick and accurate assessment of aging. There are several alternative ML-based models that may be used for the development of an aging estimation framework, and each of these models has a unique level of effectiveness. Several useful techniques for doing ML-based regression are presented in this section of the article.

*C..1 ANFIS*A Takagi–Sugeno fuzzy inference system is the foundation for a kind of artificial neural network known as an adaptive neuro-fuzzy inference system (ANFIS). The method was first conceived of and developed in the early 1990s. As a result of the fact that it incorporates both neural networks and the concepts of fuzzy logic, it has the ability to capture the advantages of both inside a single framework. Its inference system corresponds to a collection of fuzzy IF–THEN rules that are able to learn and approximate nonlinear functions. This system's learning capabilities also allow it to approximate functions that are not linear. As a consequence of this, ANFIS is regarded as a universal estimator [45].

*C..2 ANN*An ANN is built on top of a network of interconnected units, or nodes, that are referred to as "artificial neurons." These neurons are meant to roughly imitate the neurons that are found in a biological brain. Each connection, similar to the synapses that are found in real brains, has the ability to send a signal to other neurons. An artificial neuron is one that first receives signals, then analyzes those signals, and then sends messages to other neurons that it is linked to. The "signal" at a connection is a real number, and the output of each neuron is calculated by some non-linear function of the sum of its inputs. The weight of neuronal dendrites and edge connections often changes as a function of ongoing learning. The intensity of the signal at a connection may be increased or decreased depending on its weight. It's possible that neurons have a threshold, and that only when the total signal exceeds that threshold will the neuron send out a signal. In most cases, groups of neurons are organized into layers. It's possible for each layer to make unique changes to the data that they receive. Signals are sent from the first layer, known as the input layer, all the way through to the last layer, known as the output layer, and may do so more than once along the way [46].

*C..3 SVR*Support Vector Machines are supervised learning models with related learning algorithms that examine data for the purpose of classification and regression analysis. They are part of the field of machine learning. When doing support vector regression, the term "hyperplane" is used to refer to the needed straight line in order to properly fit the data. The purpose of a method known as a support vector machine is to locate, in a space of n dimensions, a hyperplane that can classify the data points in a manner that is unique. The data points that are located on each side of the hyperplane and are in the closest proximity to the hyperplane are referred to as support vectors. These factors affect the location and orientation of the hyperplane and, as a result, contribute to the construction of the SVM [47].

*C..4 KNN*The k-nearest neighbors algorithm, also known as kNN, is a non-parametric supervised learning method that was initially developed by Evelyn Fix and Joseph Hodges in 1951 and later expanded upon by Thomas Cover. It has applications in both regression and classification. In both scenarios, the input is made up of the k training instances in a data collection that are the closest to one another. The classification of an item is determined by the majority vote of its neighbors, with the object being placed in the category that is the most prevalent among its k closest neighbors (k is a positive integer, typically small). In the event that k equals one, the item in question is just designated as belonging to the category of its one closest neighbor. The classification method known as k-nearest neighbors only makes local approximations of the function, and it puts off all computing until after the function has been evaluated. Because the classification of this algorithm is based on distance, if the features represent different physical units or come in vastly different scales, then normalizing the training data can significantly improve the algorithm's accuracy. This is because distance is used to determine which features belong to which category [48].

*C..5 RF*An ensemble learning approach for classification, regression, and other problems known as "random forests" function by creating a large number of decision trees during the training phase of the method.

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Table I.: Simulation parameters for CMOS and MGK technologies

Simulation parameters	CMOS	MGK
Model used	Bulk CMOS PTM	MGK PTM
Technology used (nm)	22	22
V_{DD} (V)	1	1
Temperature (°C)	27	27
Time period (Years)	10	10

Random-choice forests are a subset of random forests. When used to solve classification problems, the output of the random forest is the category that was chosen by the majority of trees. When doing regression tasks, the result that is delivered is the mean or average forecast of the individual trees. The tendency of decision trees to overfit their training set is something that random decision forests are able to adjust for. Random forests have a higher overall performance compared to decision trees, but their accuracy is lower than that of gradient-enhanced trees. However, the quality of the data may influence how well they function [49].

V. Experimental Setup

It is possible to get the sensitivity of each gate from the threshold voltage shift of all of its internal transistors. Both the fresh delay, also known as zerotime, and the degradation of gate output transition time are determined at the same time. All of these values are derived from extensive HSPICE MOSRA simulations, run using the 22nm bulk and MGK MOSFETs predictive technology model (PTM) [50], for a variety of load capacitances and and supply voltages (keeping temperature constant at room temperatutre of 27°).
A Python script is used to construct the necessary netlists in order to accomplish this goal. The aging-aware STA, which is used for data collection and the development of training sets, requires large amount of simulations on HSPICE MOSRA. In order to carry out STA analysis, a Verilog description of the circuits must first be produced. The Synopsys Design Compiler must then synthesize the description while also adhering to the limitations of speed and area. In order to carry out the synthesis procedure, a 22-nm standard-cell library has been built by scaling the cells of an open-source standard-cell library called Nangate 45nm Open Cell Library [51]. This library is based on 45nm bulk CMOS technology.
By propagating the signal probability values of the major inputs of the circuit, it is possible to retrieve the signal probability values of all of the internal nodes of the gate-level description of the circuit. This is done for a certain signal probability. These statistical statistics are derived from the distribution of the deteriorated threshold voltage that is present in each internal transistor to arrive at the conclusion. A training set for a machine learning-based prediction model of sufficient size may be created by HSPICE MOSRA simulations with varying supply voltages and Signal probabilities. This research makes use of a three-fold cross-validation method. The Neural Network package's MLPRegressor function is used to evaluate the accuracy of ANN calculations on the aging process. In this study, the SVR regression technique with the RBF kernel is used. The sklearn.svm package contains an implementation for support-vector-machines regression algorithms. In addition, the RandomForestRegressor function that is included in the sklearn.ensemble package is used for the purpose of determining how effective the Random Forest (RF) algorithm is. Random forests and support vector regressions are used as the basic estimators, and a neural network model is employed to produce the final prediction. The parameters of the base models are identical to the parameters that were measured for these models in earlier research.

VI. Results

The probability distribution function (PDF) for aging severity that corresponds with a certain signal probability was obtained utilizing HSPICE MOSRA. After that the mean value and standard deviation of the severity of aging is determined by applying the distribution. The aging-aware STA approach is used as the foundation for each HSPICE MOSRA simulation till the appropriate pair training data set for the model is obtained. Table 1 highlights the simulation parameters utilized for CMOS and MGK technologies. Using a number of different ML-based regression models, the method that has been suggested calculates the mean and standard deviation of the aging severity distribution for the benchmark circuits.
R Value, also known as the Pearson correlation coefficient, measures the strength and direction of a linear relationship between two variables. It ranges from -1 to 1, where a value of 1 indicates a perfect positive linear relationship, a value of -1 indicates a perfect negative linear relationship, and a value of 0 indicates no linear relationship. R2 Value, also known as the coefficient of determination, represents the proportion of variance in the dependent variable that can be explained by the independent variable(s). It ranges from 0 to 1, where a value of 1 indicates that all the variance in the dependent variable is explained by the independent variable(s). MSE, or Mean Squared Error, measures the average of the squared differences between the actual and predicted values. It is a common metric used to evaluate the performance of a regression model. RMSE, or Root Mean Squared Error, is the square root of the MSE. It is a popular metric for evaluating the accuracy of a regression model, as it measures the average deviation of the predicted values from the actual values in the same units as the dependent variable. **These metrics are relevant because they provide a quantitative measure of how well a model fits**

Table II.: Artificial Neural Networks (ANN) & Adaptive Neuro-Fuzzy Inference Systems (ANFIS) Results for Bulk CMOS and MGK technologies

		22nm Bulk CMOS			22nm Metal Gate High-k (MGK)		
		Mean Absolute Error (MAE)	Root Mean Squared Error (RMSE)	R Value	Mean Absolute Error (MAE)	Root Mean Squared Error (RMSE)	R Value
Inverter	ANN	0.0024	0.0067	0.9820	0.0018	0.0044	0.9534
	ANFIS	0.0014	0.0040	0.9935	0.0005	0.0004	0.9989
NAND	ANN	0.0016	0.0046	0.9965	0.0006	0.0008	0.9989
	ANFIS	0.0005	0.0017	0.9990	0.0004	0.0005	0.9992
NOR	ANN	0.0021	0.0059	0.9988	0.0025	0.0072	0.9887
	ANFIS	0.0004	0.0013	0.9992	0.0004	0.0005	0.9981
XOR	ANN	0.0001	0.0003	0.9996	0.0002	0.0002	0.9998
	ANFIS	0.0001	0.0003	0.9999	0.0001	0.0002	0.9999
XNOR	ANN	0.0015	0.0041	0.9934	0.0019	0.0051	0.9975
	ANFIS	0.0002	0.0003	0.9998	0.0016	0.0042	0.9917

Table III.: SVR, RF Regression and KNN Machine Learning Models Results for Bulk CMOS and MGK technologies

		22nm Bulk CMOS			22nm Metal Gate High-k (MGK)		
		R2 Value	Mean Absolute Error (MAE)	Root Mean Squared Error (RMSE)	R2 Value	Mean Absolute Error (MAE)	Root Mean Squared Error (RMSE)
Inverter	SVR	0.9532	0.1746	0.4854	0.8959	0.2615	0.5048
	RF	0.9972	0.0007	0.0020	0.9641	0.0012	0.0027
	KNN	0.9969	0.0009	0.0021	0.9604	0.0012	0.0029
NAND	SVR	0.9256	0.2316	0.3080	0.8876	0.2772	0.6296
	RF	0.9939	0.0018	0.0044	0.9883	0.0006	0.0016
	KNN	0.9928	0.0017	0.0048	0.9859	0.0007	0.0018
NOR	SVR	0.9712	0.1518	0.3904	0.9658	0.1030	0.4448
	RF	0.9946	0.0037	0.0095	0.9913	0.0016	0.0042
	KNN	0.9942	0.0041	0.0099	0.9932	0.0013	0.0037
XOR	SVR	0.9649	0.1094	0.4261	0.9589	0.1235	0.4862
	RF	0.9938	0.0035	0.0116	0.9910	0.0015	0.0044
	KNN	0.9942	0.0037	0.0115	0.9919	0.0013	0.0042
XNOR	SVR	0.9635	0.1084	0.4128	0.9749	0.1161	0.3900
	RF	0.9939	0.0052	0.01631	0.9969	0.0022	0.0040
	KNN	0.9943	0.0051	0.0158	0.9815	0.0046	0.0099

the data and predicts the outcome variable. They are commonly used in regression analysis to evaluate the performance of a model and compare it to other models. A higher R2 value and a lower MSE and RMSE indicate a better fit and better predictive performance. Table II illustrates the results of ANN & ANFIS of Bulk CMOS and MGK technologies at 22nm technology node for basic digital gates. Table III illustrates the results of SVR, RF Regression and KNN Machine Learning Models Results of Bulk CMOS and MGK technologies at 22nm technology node for basic digital gates. Table IV highlights data collection runtime and number of gates for each benchmark circuit. The amount of time required for the training of each model is illustrated in table V. The table also includes a listing of the parameters of the models. Table VI and VII displays the amount of time required to complete the HSPICE MOSRA aging analysis for each circuit in bulk and MGK technologies. This amount of time is roughly equivalent to the amount of time required to complete the age-aware STA. The approach of machine learning results in the production of two distinct models: one is used to estimate the mean value, and the other is used to estimate the standard deviation. The entire amount of time spent running these two models is included in the runtime that is shown in the table. When compared to the HSPICE MOSRA technique, the findings demonstrate that ML-based methods may significantly cut down on the amount of time required to complete an aging study by more than 99%. This improvement is accomplished by increasing the amount of time spent offline in training.

The HSPICE MOSRA and the proposed ML-based models are used to extract statistical characteristics of stochastic aging severity for different circuits and workloads in order to evaluate the accuracy of the proposed method. This is done for the purpose of determining whether or not the proposed method is accurate. Tables VIII, IX and X, XI show, respectively, the average values of the mean value and standard deviation using HSPICE MOSRA for each circuit. These results are presented in tabular format. These tables also reflect the degree of accuracy achieved by the ML-based models in comparison to the HSPICE MOSRA findings. According to the findings, ANFIS approach has the highest level of efficiency in terms of accurately forecasting aging traits. It is important to note that the runtimes required to retrieve these values have been greatly reduced, as can be seen in Table 3. In conclusion, the findings of the experiments indicate that the approach that was presented is capable of obtaining the statistical properties of stochastic aging with an accuracy of up to 98% and a decrease in runtime of more than 99%. As a result, the suggested method is appropriate for carrying out aging analysis in order to investigate the design space at relatively high levels of abstraction.

Table IV.: Data collection runtime and number of gates for each benchmark

Benchmark	# gates	Data collection runtime (s)	
		22nm Bulk CMOS	22nm Metal MGK
Adder	492	870.84	1102.08
Subtractor	511	904.47	1144.64
Comparator	251	444.27	562.24
C432	160	283.2	358.4
C880	383	677.91	857.92
C1355	546	966.42	1223.04

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Table V.: Training runtime and parameters of each ML-based regression model

Estimation model	Training runtime (s)		Model Parameters
	22nm Bulk CMOS	22nm MGK	
ANN	68.41	92.62	power-t=0.5 alpha=0.001 #neurons=100
ANFIS	94.45	130.24	Number of membership functions (MF) =10 Epochs = 200 Error tolerance = 0
SVR	25.92	38.56	gamma=0.001 C=100

RF	31.84	44.35	#estimators=150
			depth=20

KNN	30.56	42.75	mode='connectivity' n_neighbors=2

Table VI.: The runtime of aging analysis for different approaches for 22nm Bulk CMOS

Circuit	Runtime (msec) for 22nm Bulk CMOS					
	ANN	ANFIS	SVR	RF	KNN	HSPICE
add	1.58	2.68	1.32	1.47	1.67	1121
sub	1.56	2.62	1.31	1.56	1.36	1202
comp	1.88	2.24	1.29	1.45	1.51	524
C432	1.47	2.35	1.29	1.54	1.24	375
C880	1.52	2.24	1.12	1.48	1.32	674
C1355	1.56	2.15	1.12	1.55	1.62	1262

Table VII.: The runtime of aging analysis for different approaches for 22nm MGK

Circuit	Runtime (msec) for 22nm MGK					
	ANN	ANFIS	SVR	RF	KNN	HSPICE
add	1.68	2.86	1.45	1.54	1.73	1223
sub	1.66	2.82	1.47	1.58	1.59	1359
comp	1.85	2.74	1.32	1.65	1.83	589
C432	1.57	2.55	1.40	1.75	1.76	412
C880	1.58	2.45	1.37	1.75	1.51	724
C1355	1.65	2.68	1.30	1.65	1.85	1425

Table VIII.: The mean value of aging severity obtained by HSPICE, and accuracy of ML models for 22nm Bulk CMOS

Circuit	The Mean value of aging severity for 22nm Bulk CMOS					
	Accuracy (compared to HSPICE) %					HSPICE
	ANN	ANFIS	SVR	RF	KNN	
Add	98.55	99.85	97.33	99.21	99.43	7.54
Sub	98.45	99.98	97.84	99.10	99.54	7.02
comp	98.64	99.86	98.12	99.32	99.47	8.00
C432	98.75	99.75	97.27	99.25	99.51	7.24
C880	98.66	99.65	97.98	99.35	99.49	8.15
C1355	98.83	99.92	97.84	99.50	99.45	7.25
average	98.65	99.84	97.73	99.29	99.48	NA

Table IX.: The mean value of aging severity obtained by HSPICE, and accuracy of ML models for 22nm MGK

Circuit	The Mean value of aging severity for 22nm MGK					
	Accuracy (compared to HSPICE) %					HSPICE
	ANN	ANFIS	SVR	RF	KNN	
Add	98.45	99.75	97.35	99.25	99.44	7.24
Sub	98.55	99.79	97.33	99.30	99.64	6.75
comp	98.46	99.88	98.30	99.35	99.55	7.88
C432	98.65	99.67	97.35	99.20	99.56	7.00
C880	98.75	99.80	97.88	99.40	99.43	7.80
C1355	98.85	99.85	97.75	99.45	99.58	7.10
average	98.62	99.79	97.66	99.32	99.53	NA

Table X.: The standard deviation of aging severity obtained by HSPICE, and accuracy of ML models for 22nm Bulk CMOS

Circuit	Standard deviation of aging severity for 22nm Bulk CMOS					
	Accuracy (compared to HSPICE) %					HSPICE
	ANN	ANFIS	SVR	RF	KNN	
Add	98.65	99.87	97.45	99.45	99.55	0.95
Sub	98.54	99.98	97.90	99.31	99.65	0.85
comp	98.70	99.90	98.38	99.53	99.78	0.89
C432	98.80	99.81	97.40	99.45	99.60	0.83
C880	98.75	99.72	97.99	99.55	99.57	0.78
C1355	98.85	99.95	97.90	99.70	99.64	0.82
average	98.72	99.87	97.83	99.50	99.63	NA

Table XI.: The standard deviation of aging severity obtained by HSPICE, and accuracy of ML models for 22nm MGK

Circuit	Standard deviation of aging severity for 22nm MGK					
	Accuracy (compared to HSPICE) %					HSPICE
	ANN	ANFIS	SVR	RF	KNN	
Add	98.77	99.91	97.55	99.64	99.65	0.91
Sub	98.54	99.98	97.92	99.57	99.70	0.80
comp	98.78	99.92	98.44	99.70	99.80	0.87
C432	98.85	99.84	97.46	99.62	99.65	0.79
C880	98.80	99.83	97.99	99.65	99.62	0.76
C1355	98.87	99.97	97.92	99.75	99.70	0.81
average	98.77	99.91	97.88	99.66	99.69	NA

VII. Conclusion

In this work, a ML based aging prediction model was built. The training set was acquired via considerable HSPICE MOSRA simulations. The proposed solution reduced prediction runtime by up to 99% while maintaining 99% accuracy throughout the process. The training of the model required a considerable amount of time. On the other hand, it was only carried out once as an offline operation, prior to the forecast, and it had no impact on the outcome. To a high degree, the model was able to fulfill the criteria of the aging analysis.

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