

Impact of the gate work function on the experimental I-V characteristics of MOS solar cells simulated with the Sentaurus TCAD software

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Abstract—In this work, the influence of gate work function on the experimental J-V_G characteristics of MOS solar cells was investigated with the aid of the Sentaurus TCAD for 2D numerical simulations of TiN/SiO_xN_y/Si Al/SiO_xN_y/Si and Al/MgO/Mg/SiO_xN_y/Si structures aiming at solar cells for energy harvesting applications. The increase of the gate work function led to the increase of the reverse current density as pointed out by the Sentaurus TCAD simulations and by the experimental J-V_G characteristics. The work functions of Mg, Al, and un-annealed TiN used in the TCAD simulations were 3.7 eV, 4.1 eV, and 4.4 eV, respectively. It was observed that the onset voltage at 0.5 mA/cm² in the forward-biasing region was at a lower voltage for TiN (~ - 0.06 V) compared to Al (~ - 0.42 V) and the Al/MgO/Mg stack (~ - 0.47 V). On the other hand, the current density increased steeply in the forward biasing for TiN and Al compared to the Al/MgO/Mg stack gate and the thin MgO layer between Al and Mg worked as a potential barrier in an opposite direction to the potential barrier of the Mg/SiO_xN_y/Si structure, which meant an onset voltage lowering for the Al/MgO/Mg/SiO_xN_y/Si solar cell. For the Al/MgO/Mg stack, the barrier effect of the MgO layer was fitted as a series resistance R_S = 100 Ω and an equivalent Al/MgO/Mg work function of 4.15 eV considering a substrate doping N_A = 1.2x10¹⁶ cm⁻³ and parallel conductance G_P = 0. Also, the experimental JxV_G characteristic of the Al/SiO_xN_y/Si cell was fitted for Al work function of 4.10 eV, a series resistance R_S = 100 Ω, a parallel resistance R_P = 0.02 Ω (G_P = 50 S) and a substrate doping N_A = 5.5x10¹⁵ cm⁻³. In this case, the high parallel conductance fitted was attributed to the tunneling through the dielectrics as a predominant effect possibly caused by a high concentration of defects in the SiO_xN_y layer. Finally, the MOS solar cell parameters were relatively lower compared to those of commercial outdoor solar cells, but the power generated by the MOS cells reached the mW range, and the conversion efficiency from light energy into electrical energy was higher (12.7%) than the typical values found for energy-harvesting solar cells.

Index Terms— I-V electrical characteristics; Sentaurus TCAD; MOS solar cells.

INTRODUCTION

Currently, the energy conversion efficiency of commercial outdoor C-Si solar cells is about 27% [1-4] and indoor solar cells for energy harvesting, also known as IPV_s (Indoor Photovoltaics), is about 5-7% and reaches the mW range for output power [1, 5]. The global market for IPV_s has grown rapidly as these devices have great potential for powering IOT (Internet of Things), including integrated circuits, communication devices, and distributed and remote sensors. Among the different types of structures used for power generation, solar cells based on MOS (metal-oxide-semiconductor) technology are suitable candidates for improving the efficiency of indoor power generation, since the manufacturing process of these cells has low complexity and low costs [5, 6]. For these devices, the charge carriers tunnel through the potential barrier of the gate dielectrics, which requires a high

control of the ultrathin film thickness in the range of 1 to 2 nm and the work function of the gate material [7, 8].

There are several works in the literature on the manufacture of MOS solar cells using thin gate dielectrics as a mean for tunneling the generated charge carriers of the electric current [6, 9-14]. In the 1970s, researchers from NASA showed that it is possible to fabricate solar cells MOS with inversion region induced by positively charged layers of SiO to achieve high efficiency in converting light energy into electrical energy. [15-16]. As late as the 1970s, articles were published on MOS solar cells that showed conversion yields comparable to those of PN solar cells. The scheme proposed in 1978 by Pulfrey [17] for the MOS solar cell consisted of using any substrate, glass or metal, as a support for one or more semiconductors. The case studies were silicon and gallium arsenide (GaAs) in combination with germanium [17].

In MOS solar cells, the thermally grown ultrathin gate dielectric leads to the passivation of the semiconductor surface, so that the barrier height is mainly determined by the work function of the gate metal rather than by the charge effect of the interface states [10]. For metal/SiO₂/p-Si structures with a metal/insulator barrier height (φ_o) of less than 3.6 eV, the predominant mechanism is the tunneling of minority carrier electrons through the dielectrics, while for more than 3.6 eV, conduction by majority carrier holes is also activated. Figure 1 shows the energy band diagram of the Al/SiO₂/p-Si solar cell (φ_o ≅ 3.2 eV) where the predominant tunneling process is by minority carrier conduction from the inversion layer, which is why this cell is called inversion layer MOS solar cell [10].

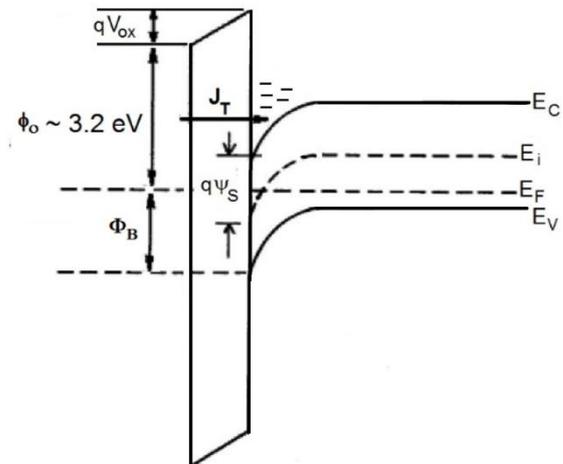


Fig.1 Energy band diagram for the Al/SiO₂/p-Si structure (adapted from [10])

The current through inversion MOS solar cells with ultrathin gate oxides can be described by a similar modeling to

that of the Schottky contact by taking into account the influence of the incident light illumination [18].

Figure 2 shows the MOS solar cell described by an equivalent circuit model [18, 19] consisting of a Schottky exponential-type junction (D_1), a constant photo-generated current-density source (J_L), a series resistance (R_S) due to the contact and the substrate-bulk resistances and a parallel conductance (G_P) that model a tunneling-limited current through the gate dielectrics [20].

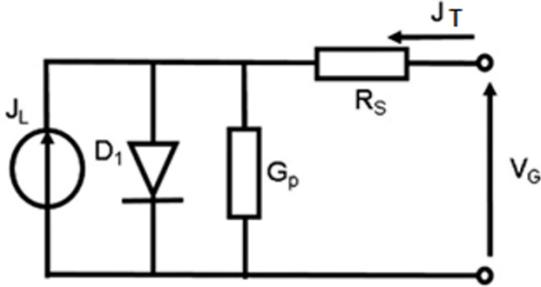


Fig.2 MOS solar cell model

Equation 1 is a mathematical description of the circuit in Figure 2 with the given parameters J_T , R_S , G_P , J_L , V_G . $V_T = kT/q$ is the thermal voltage (0.02552 V at 23°C) and n is the ideality factor. This equation can be solved for J_T and V_G by means an analytical procedure that makes use of the Lambert function [19].

$$J_T = J_0 \left(e^{\frac{-V_G - R_S * J_T}{n * V_T}} - 1 \right) + (-V_G - R_S * J_T) G_P - J_L \quad (1)$$

MOS solar cells with structures TiN/SiO_xN_y(1.73nm)/p-Si, Al/SiO_xN_y(1.73nm)/Si-p and Al/Mg/SiO_xN_y(1.73nm)/p-Si were manufactured at LSI/EPUSP for indoor energy harvesting applications using typical intensities in the range of 10 μW/cm² to 1mW/cm² [5, 20] on substrates with resistivity simulating possible post-processing applications of MOS solar cells on integrated circuits for specific applications, for example, subcutaneous implants for monitoring health parameters [21].

Sentaurus TCAD (Technology Computer-Aided Design) is a powerful tool for 2D/3D numerical simulation which allows one the analysis of electrical, thermal, and optical properties using command scripts of parameters related to electrical biasing, operating temperature, series resistance, the parallel conductance and the incident light on silicon solar cells [22].

In the present work, the influence of the gate work function on the experimental J-V_G characteristics of MOS solar cells is investigated with the aid of the Sentaurus TCAD for simulation of TiN/SiO_xN_y/Si Al/SiO_xN_y/Si and Al/MgO/Mg/SiO_xN_y/Si structures.

METHODOLOGY

A. Manufacture of MOS solar cells and electrical measurements

TiN/SiN_xO_y/p-Si, Al/SiN_xO_y/p-Si and Al/Mg/SiN_xO_y/p-Si solar cells were manufactured at LSI/EPUSP on 3-inch

P(100) substrates with thickness of ~ 380 μm and resistivity of 1-10 Ω.cm. Figure 3 shows the details of the manufacturing process of the MOS solar cells, starting with the chemical cleaning (step “a” in Figure 3) using a modified RCA cleaning, according to the two baths as follow: (a) 400 ml H₂O + 25 ml NH₄OH (38%) + 175 ml H₂O₂ (37%) and (b) 400 ml H₂O + 100 ml HCl (38%), both heated at 90°C, for 15 min [5].

After the chemical cleaning the gate oxynitride was grown by Rapid Thermal Processing (RTP) at 850 °C for 100 s with a thickness of 1.73 nm (step “b” in Figure 3) using an adapted conventional thermal oxidation furnace [10]. RTP was performed by the quick insertion of the wafer from the furnace front till its center position, allowing a rapid increase of the temperature till the plateau. Each wafer was processed in a mixed ambient of ultrapure 5N₂:1O₂. The quartz carrier, for 3 inches wafers, was made using three thin brackets welded on a quartz rod in order to assure rapid increase of the temperature due to the low thermal mass in contact with each silicon wafer [5].

Then, the gate material was deposited, which was a ~200-nm thick layer of aluminum by Physical Vapor Deposition (PVD). 30-nm thick layer of magnesium with a protective ~200-nm thick aluminum layer also was deposited by PVD using an Edwards vacuum coater auto 306 at 1x10⁻⁵ Torr. Also, 18-nm thick layer of un-annealed titanium nitride (TiN) was made by Sputtering Deposition [23] (step “c” in Figure 3) using an equipment Prest Vácuo PV600 at a work pressure of 5 mTorr, argon flux of 20 sccm, deposition time of 350 s and RF power of 250W. Following, the dimensions of the MOS solar cells were defined by optical lithography (exposure of the photoresist to UV light) (step “d” in Figure 3). The gate material was then defined (step “e” in Figure 3) and the photoresist was removed. The dielectric material grown on the backside of the wafer was removed in diluted Hydrofluoric (HF) acid solution (20 H₂O:1 HF (49%)) using wet etching by localized drops followed by natural drying. Following, aluminum was deposited on the backside of the wafer by PVD using an Edwards vacuum coater auto 306 at 1x10⁻⁵ Torr (step “f” in Figure 3).

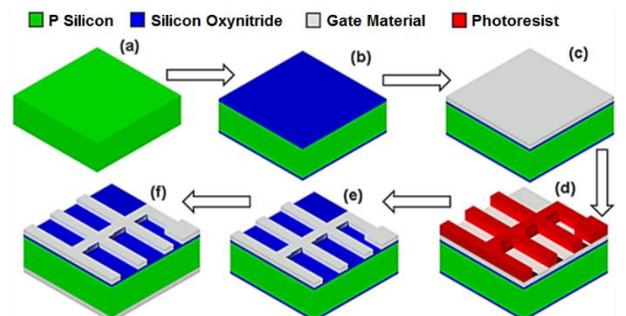


Fig.3 Profiles of the MOS solar cell obtained during the fabrication process.

Finally, an anti-reflective (AR) coating layer of SiO₂, 108nm thick, was deposited onto the defined metal gate over the area of the MOS solar cells using low temperature evaporation (PVD: Edwards vacuum coater auto 306) at 1x10⁻⁵ Torr in order to obtain a positively charged layer to invert the Si and decrease the surface reflectance from 0.345 to 0.0825

[15, 16].

During the fabrication of the MOS cells (Figure 3), a multi-finger or "fishbone" geometry was used with a finger width (L) of 50 μm and distances (D) between finger lines of 50 μm as illustrated in Figure 4. The total area (AT) was 3.24 cm^2 considering the square on which the metal grid was defined. Figure 4 shows the MOS solar cell in plan view (Figure 4a), in profile view (Figure 4b) and in plan view of the mask used for manufacturing (Figure 4c).

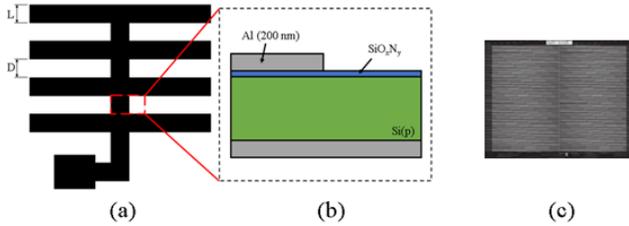


Fig.4 Images of the MOS cell top view (a), profile view (b) and mask top view (c).

The $I \times V$ measurements were performed for the solar cells in a grounded black box to avoid external electrical interference. A halogen lamp with a luminous intensity (IL) of 650 cd and a standard light spectrum of 4100 K [24] was positioned at a selected distance " d " (9 cm) above the cells adjusted to obtain an incident power density $P_{in} = 7.7 \text{ mW/cm}^2$. The distance " d " to achieve this power density was calculated using the following equation [25]:

$$d = \sqrt{\frac{IL \int f(\Delta\lambda)}{683 P_{in}}} \quad (2)$$

where IL is the luminous intensity in candela (cd), d is the distance between the halogen lamp and the solar cell and $f(\Delta\lambda)$ is the integrated light function that accounts for different penetration depths at different wavelengths (λ) for the tabulated spectrum of the halogen lamp at a temperature of 4100 K and it can be assumed to be uniform for MOS solar cells [20].

The chosen power density of 7.7 mW/cm^2 falls within the range of energy harvesting for lighting in supermarkets and department stores [26, 27], considering that the incident power outdoors on sunny days is about 100 mW/cm^2 [26].

An Agilent 4146C Source Measurement Unit (SMU) was used, programmed to apply a potential between 2 V and -2 V to the metal gate with step voltage of 0.1 V/s in order to extract the $I \times V$ characteristics and obtain the usual important parameters of the solar cells: Short Circuit Current Density (J_{sc}), Open Circuit Voltage (V_{oc}), Maximum Power Density (P_{max}) and Fill Factor ($FF = P_{max}/(V_{oc} \cdot J_{sc})$) and the conversion efficiency ($\eta = P_{max}/P_{in}$) obtained from the incident power density $P_{in}(\text{mW/cm}^2)$ [1, 20].

B. Simulation with Sentaurus TCAD

MOS solar cells MOS were simulated in 2D using the Sentaurus TCAD software. It is a Unix platform developed by Synopsys with an interface based on text codes, where the simulation parameters are specified in the form of command

scripts or by means of the Structure Editor module. The SDEVICE module of TCAD allows the simulation of electrical, thermal, and optical properties using command scripts of electrical biasing, operating temperature and optical parameters related to the incident light [22].

The simulations of current density characteristics as a function of gate voltage ($J \times V_G$) for MOS solar cells with and without light were performed using the 2D profile in the Sentaurus TCAD using the profile view as shown in Fig 4(b). The typical values of the work function for Al [28], un-annealed TiN [23] and Mg [28] were used. Since the 2D simulations provided current per unit width, it was divided by the length of the structure to obtain the current per unit area and to allow comparison with the experimental ones. In addition, R_S and G_P [19] were introduced in the TCAD script to consider the influence of the parallel conductance attributed to defects in the SiO_xN_y layer and the series resistance due to the contact and the substrate-bulk resistances, respectively, to be shown in the results and discussions.

The structures $\text{TiN}/\text{SiN}_x\text{O}_y(1.73\text{nm})/\text{p-Si}$, $\text{Al}/\text{SiN}_x\text{O}_y(1.73\text{nm})/\text{Si-p}$ and $\text{Al}/\text{Mg}/\text{SiN}_x\text{O}_y(1.73\text{nm})/\text{p-Si}$ with ultrathin dielectrics, were simulated as Schottky contacts considering the barrier height is mainly determined by the work function of the gate metal rather than by the charge effect of the interface states [10]. The barrier height for p-type semiconductors can be described as follows [10, 22]:

$$\Phi_B = \frac{E_g}{q} + \chi - \Phi_M \quad (3)$$

where E_g is the bandgap width of the semiconductor, Φ_B is the Schottky barrier height as indicated in Figure 1, Φ_M is the metal work function, and χ is the electron affinity of the semiconductor.

For aluminum gate and p-type silicon ($\Phi_M = 4.10 \text{ eV}$, $\chi = 4.05 \text{ eV}$ and $E_g/q = 1.10 \text{ eV}$) the MOS structure ideally has a Schottky barrier height Φ_B of $\sim 0.8 \text{ eV}$. In addition, Sentaurus TCAD uses a tuning parameter (pinning) denoted as S . For p-type semiconductors, the Schottky barrier height can be written, as follows [29]:

$$\Phi_B = S \left(\frac{E_g}{q} + \chi - \Phi_M \right) + (1-S) \frac{E_{CNL}}{q} \quad (4)$$

where E_{CNL} is the energy level in the charge neutrality at the silicon oxide/silicon interface and S is a Sze or Mönch-type fitting [29].

Some metals were studied in the gate region with different work functions and barrier heights, as shown in Table I below:

Table I. Work function and barrier heights for Mg, Al and un-annealed TiN.

Metal	Work function $\phi_M(\text{eV})$	Barrier Height $\phi_0(\text{eV})$
Mg	3.70 [28]	~ 2.2 [30]
Al	4.10 [28]	~ 3.2 [10]
TiN	4.40 [23]	~ 3.8 [31]

Current densities were also simulated for incident light

with power density $P_{in} = 7.7 \text{ mW/cm}^2$ of a halogen light source at 4100 K.

RESULTS AND DISCUSSION

First of all, Sentaurus TCAD 2D simulations were performed to evaluate the influence of the barrier height on the J- V_G Characteristics of MOS solar cells with $R_S = 100 \Omega$ and $G_P = 0$. Figure 5 shows simulations of the current density as a function of gate voltage V_G for un-annealed TiN, Al and Mg with work functions of 4.40 eV, 4.10 eV and 3.70 eV, respectively, in the dark condition (without light illumination). To highlight and evaluate the behavior of each section of the curves, a logarithmic scale was set for the current density axis. Also, the abscissa axis had its direction inverted starting from $V_G > 0$ (reverse voltage at the left side) to $V_G < 0$ (forward voltage at the right side). This axis inversion leads to a usual representation mode for PN diodes that will be also employed for all the J-V characteristics of the MOS diodes in the following.

For $V_G > 0$, Figure 5 shows the dark current density levels increasing progressively from Mg to Al to TiN. This behavior adheres to the work function (ϕ_M) feature shown in Table I, this is to say, the higher the work function, the lower the Schottky barrier in Equation 3 and the higher the reverse current density is. On the other hand, for $V_G < 0$, it is observed sections with linear slopes corresponding to the exponential growth which tend to saturate when the voltage drop across R_S becomes appreciable. It is worth of note that the higher the reverse current density is, the sooner the exponential section increases as predicted by a Schottky exponential-type modeling [10].

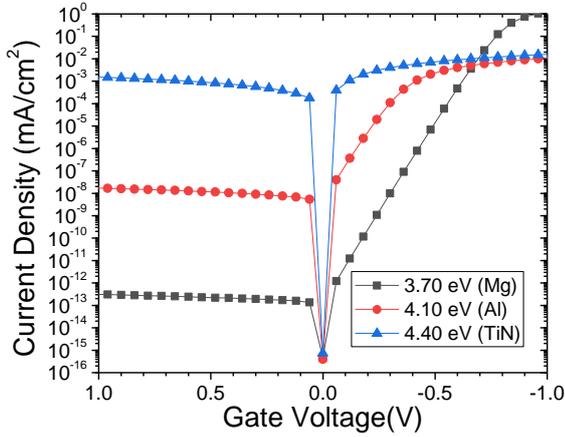


Fig.5 Sentaurus TCAD simulation of the current density as a function of the gate voltage V_G for Mg, Al and TiN as gate materials with work functions of 3.70 eV, 4.10 eV and 4.40 eV, respectively, in the dark condition. (V_{ON} at 0.5 mA/cm^2 is -0.06 V for TiN, -0.36 V for Al and -0.60 V for Mg).

Figure 6 shows typical graphs of the current density (J) as a function of gate voltage (V_G) obtained experimentally for TiN, Al and Mg, without light illumination. Assuming the onset voltage at 0.5 mA/cm^2 in the forward region ($V_G < 0$), it is at a lower voltage for TiN ($\sim -0.06 \text{ V}$) compared with Al ($\sim -0.42 \text{ V}$) and Mg ($\sim -0.47 \text{ V}$). On the other hand, the current density increases steeply for TiN and Al compared with Mg.

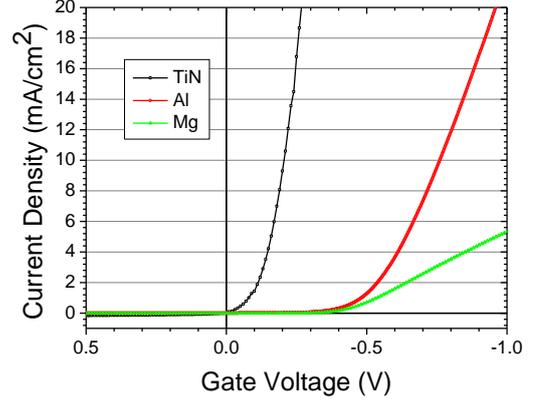


Fig.6 Typical experimental curves of current density as a function of gate voltage V_G for TiN, Al and Mg as gate materials, without light illumination (V_{ON} at 0.5 mA/cm^2 of -0.05 V for TiN, -0.43 V for Al and -0.47 V for Mg).

For Mg in Figure 6, it was expected that the onset voltage would occur at a higher value of $\sim -0.60 \text{ V}$. In this case, the series resistance was clearly higher compared to the Al gate in the same figure. As it will be shown in the following, a thin MgO layer between Al and Mg, which is formed during the Al deposition, will work as a potential barrier in an opposite direction to the potential barrier of the Mg/SiO_xN_y/Si structure.

As mentioned in the methodology, a protective $\sim 200\text{-nm}$ thick aluminum layer was deposited by PVD to avoid magnesium surface oxidation. However, after the exchange of process chamber, it was not possible to avoid the incorporation of H₂O onto the magnesium surface, which can lead to the formation of the phases MgO and MgOH through the following chemical reactions [32]:



Reaction 5 occurs rapidly in gaseous media limited to the residual H₂O and reaction 6 occurs very slowly in aqueous media [32]. Thus, the MgO is the main compound formed during the Al-evaporation step since the reaction process will be limited to the residual moisture in the deposition chamber.

As a result, the formed MgO thin layer between Al and Mg will promote a onset voltage lowering as shown in Figure 6 for the Al/MgO/Mg/SiO_xN_y/Si structure, which can be understood knowing that the Mg work function ($\sim 3.7 \text{ eV}$) is smaller than the Al work function ($\sim 4.1 \text{ eV}$). In this case, the energy-band diagram shown in the Figure 7a makes clear the opposite effect of the potential barrier due to the MgO layer which behaves as an insulator with a band gap of $\sim 7.8 \text{ eV}$ [33] in the dark condition (without light illumination). The voltage drop across this layer achieves a reverse voltage governed by the internal work function difference between Al and Mg that is given by $V_{MgO} = (\Phi_{Al} - \Phi_{Mg})/q$. As a result, the maximum voltage drop across the cell decreases from Φ_B/q to $(\Phi_B/q - V_{MgO})$.

In addition, Figure 7b illustrates the energy-band diagram of the Al/MgO/Mg/SiO_xN_y/Si cell under light illumination

showing the voltage drop $V_a = (E_{F_{Mg}} - E_{F_{Si}})/q < \Phi_B/q$ at the Mg/SiO_xN_y/Si section and the opposite voltage drop $V_b = (E_{F_{Mg}} - E_{F_{Al}})/q < V_{MgO}$ at the Al/MgO/Mg section. The total voltage drop across the Al/MgO/Mg/SiO_xN_y/Si cell is the photovoltaic voltage $V_G = V_a - V_b$.

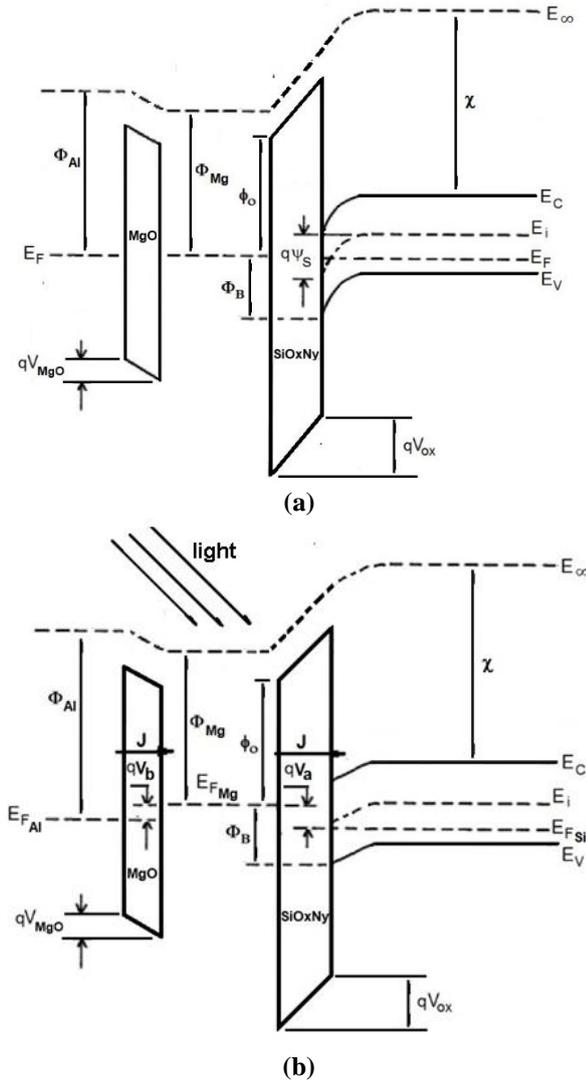


Fig.7 Band diagram of the Al/MgO/Mg/SiO_xN_y/Si without illumination (a) and under illumination (b)

Figure 8 shows the typical experimental and simulated curves of the current density (linear scale) as a function of the gate voltage V_G , obtained for Al and Mg with light illumination ($P_{in} = 7.7 \text{ mW/cm}^2$). For the Al/MgO/Mg/SiO_xN_y/Si case obtained with light illumination, it is important to point out the downward shift of the experimental $J \times V_G$ curve due to the minority carrier generation. In addition, for $V_G < 0$, the rise rate of the current density for the case with light illumination was steeper compared to the case without light illumination (compare the graph in Figure 6 with the graph in Figure 8), which was attributed to different voltage drops across the Al/MgO/Mg section with and without light illumination, respectively. It is noteworthy that the increase of V_b in Figure 8b for the case with light illumination is associated with the decrease of V_{MgO} which means a higher current density and a lower equivalent series resistance of the Al/MgO/Mg section. The same did not happen for the Al/SiO_xN_y/Si case where the curve shifted downward with an almost linear

shape for V_G in the range of 0.1 V to ~ -0.6 V. For the TiN/SiO_xN_y/Si cell under light illumination (not shown in Figure 8), the tunneling current through the dielectric was predominantly a Schottky exponential-like current, but without a downward shift of the $J \times V_G$ curve so that V_{OC} was null and the photovoltaic effect was not observed. In this case, the reverse current density ($V_G > 0$) increase by about an order of magnitude without significant change of the forward current density ($V_G < 0$).

The TCAD simulations were performed for the gate voltage ranging from 0.10 V to -0.65 V using the available libraries for TiN, Al and Mg as gate materials. For the Al/MgO/Mg gate, the barrier effect of the MgO layer was fitted as a series resistance $R_S = 100 \Omega$ and an equivalent Al/MgO/Mg work function of 4.15 eV considering a substrate doping $N_A = 1.2 \times 10^{16} \text{ cm}^{-3}$ and $G_P = 0$ (see the simulated and experimental curves in blue in Figure 8). For comparison purposes, the solid black line is the simulation for $\Phi_{Mg} = 3.7 \text{ eV}$, $R_S = 0$, $G_P = 0$ and $N_A = 1.2 \times 10^{16} \text{ cm}^{-3}$. It is worth of note that the expected onset voltage for the Al/Mg gate was ~ -0.65 V, which would mean an open-circuit voltage V_{OC} reaching up to 0.77 V without the barrier effect of the MgO layer (see $V_G \cong 0.77 \text{ V}$ for $J = 0$ on the solid black line in Figure 8).

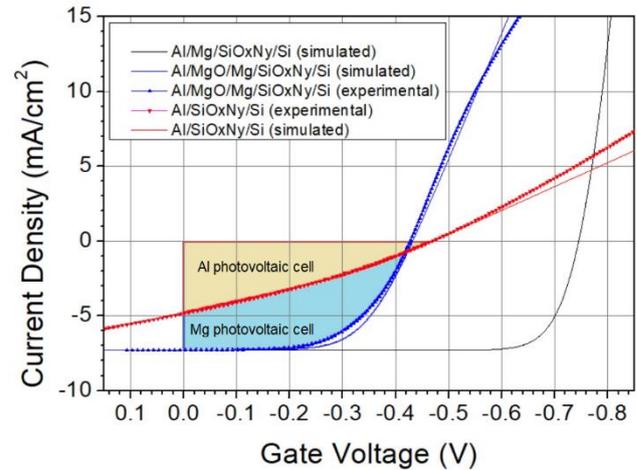


Fig.8 Experimental and simulated curves of the current density (linear scale) as a function of the gate voltage V_G , obtained for Al and Mg with light illumination ($P_{in} = 7.7 \text{ mW/cm}^2$). For comparison, the solid black line is the simulation with $R_S = 0$.

On the other hand, TCAD simulations were performed for the Al/SiO_xN_y/Si cell in the range of 0.10 V to -0.85 V. The experimental $J \times V_G$ curve in red in Figure 8 was fitted with the following parameters: $\Phi_{Al} = 4.10 \text{ eV}$, $R_S = 100 \Omega$, $R_P = 0.02 \Omega$ ($G_P = 50 \text{ S}$) and $N_A = 5.5 \times 10^{15} \text{ cm}^{-3}$. The parallel conductance, also known as shunt conductance, is usually attributed to pre-breakdown sites caused by defects crossing the solar-cell active region that show no or weak conductivity under low forward and reverse bias [34]. In the Al/SiO_xN_y/Si diode of this work, the high parallel conductance was attributed to the tunneling through the SiO_xN_y dielectrics as the predominant effect on the current density that overrode the exponential-like behavior of the Schottky barrier. This predominant effect was possibly caused by defects in the SiO_xN_y layer that were activated by the voltage drop across the die-

lectrics in the Al/SiO_xN_y/Si structure. In this case, the concentration of defects would be higher compared with that in the dielectrics of the Mn/SiO_xN_y/Si section of the Al/MgO/Mg/SiO_xN_y/Si structure whose $G_P \cong 0$.

Figure 8 also shows the photovoltaic regions for the Al/SiO_xN_y/Si and Al/MgO/Mg/SiO_xN_y/Si cells and Table II in the following shows the extracted photovoltaic parameters which are the short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}) maximum power density (P_{max}), and the fill factor ($FF = P_{max}/(V_{OC} \cdot J_{SC})$) and the conversion efficiency ($\eta = P_{max}/P_{in}$) obtained from the incident power density $P_{in} = 7.7 \text{ mW/cm}^2$.

Table II. Main parameters of the Al/SiO_xN_y/Si and Al/MgO/Mg/SiO_xN_y/Si solar cells

Cell	J_{SC} (mA/ cm ²)	V_{OC} (mV)	FF (%)	P_{max} (mW/ cm ²)	η (%)
Al/SiO _x N _y /Si	4.76	470	23.7	0.53	6.9
Al/MgO/Mg/ SiO _x N _y /Si	7.32	428	31.3	0.98	12.7

It is noteworthy in Table II that FF , J_{SC} , and V_{OC} parameters were smaller compared to the parameters of commercial solar cells [1]. However, the generated power (P_{max}) reached the mW range and the conversion efficiency was higher compared to the typical values reported for energy harvesting applications [1, 27]. In addition, although the MgO layer has triggered a decrease of the V_{OC} parameter for the Al/MgO/Mg/SiO_xN_y/Si cell, the J_{SC} and FF parameters were sufficiently higher to obtain a higher conversion efficiency of 12.7 % compared with 6.9 % for the Al/SiO_xN_y/Si cell.

CONCLUSIONS

In this work, the influence of the gate work function on the experimental J - V_G characteristic of MOS solar cells was investigated with the help of Sentaurus TCAD simulations.

It was observed that the onset voltage at 0.5 mA/cm^2 in the forward-biasing region was $\sim -0.06 \text{ V}$ for TiN, $\sim -0.42 \text{ V}$ for Al and $\sim -0.47 \text{ V}$ for the Al/MgO/Mg stack gate. On the other hand, the current density increased steeply for TiN and Al compared to the Al/MgO/Mg stack gate.

Without light illumination, it was observed that the reverse current levels increased from the Al/MgO/Mg stack to Al to TiN indicating that the higher the work function, the higher the current density level. In addition, the height of the Schottky barrier decreased as the metal work function increased and led to an increase of the reverse current density.

A thin MgO layer between Al and Mg, which was formed during the Al deposition, worked as a potential barrier in an opposite direction to the potential barrier of the Mg/SiO_xN_y/Si structure. This MgO thin layer promoted an onset voltage lowering for the Al/MgO/Mg/SiO_xN_y/Si structure, which was explained based on the Mg work function ($\sim 3.7 \text{ eV}$) smaller than the Al work function ($\sim 4.1 \text{ eV}$), which means an opposite effect of the potential barrier due to the MgO thin insulator.

A halogen lamp with a luminous intensity (IL) of 650 cd and a standard light spectrum of 4100 K was positioned above the cells to obtain an incident power density $P_{in} = 7.7 \text{ mW/cm}^2$. For the Al/MgO/Mg stack, the barrier effect of the

MgO layer was fitted as a series resistance $R_S = 100 \Omega$ and an equivalent Al/MgO/Mg work function of 4.15 eV considering a substrate doping $N_A = 1.2 \times 10^{16} \text{ cm}^{-3}$ and $G_P = 0$.

TCAD simulations were also performed for the Al/SiO_xN_y/Si cell in the range of 0.10 V to -0.85 V. The experimental $J \times V_G$ curve was fitted with $\Phi_{Al} = 4.10 \text{ eV}$, $R_S = 100 \Omega$, $R_P = 0.02 \Omega$ ($G_P = 50 \text{ S}$) and $N_A = 5.5 \times 10^{15} \text{ cm}^{-3}$. In this case, the high parallel conductance was attributed to defects in the SiO_xN_y layer that are activated by the voltage drop across the dielectrics in the Al/SiO_xN_y/Si structure.

The extracted photovoltaic parameters fill factor (FF), short circuit current density (J_{SC}), and open circuit voltage (V_{OC}) were relatively smaller compared to the parameters of commercial solar cells, but the power generated by MOS cells reached the mW range and the conversion efficiency was higher (12.7 %) than the typical values found for solar cells applied in energy harvesting.

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