Area Efficient and Linear MMIC Based Ka Band Power Amplifier for 5G Communication Systems

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***Abstract*— This work presents a monolithic microwave integrated circuit (MMIC) based power amplifier (PA) with single 150 nm GaN high electron mobility transistor (HEMT) using broadband matching. For the proposed amplifier, two stage L-type biasing network is designed. In order to provide good linearity, low Q, broader bandwidth and optimized chip area, band pass filter (BPF) type matching network is proposed. The topology and parameter selection is done by performing proper load pull analysis. This helps in achieving wide band matching to maintain low Q factor. Thus the proposed amplifier is evaluated with post layout EM simulation data. For the 26 GHz band of 5G communication, proposed amplifier has a small signal gain of 11 dB for 21-27.4 GHz. The amplifier offers 33.42 dBm saturated output power and good linearity. The designed PA provides 31.35 dBm output power, 26% power added efficiency (PAE) and 29% drain efficiency (DE) at 1 dB compression with IP3 of 39.67 dBm for 26 GHz band. The designed PA has less complexity and small chip area of 4.3 mm^2.**

***Index Terms*— 5G, Power Amplifier, Area Efficiency, Broadband Matching, GaN HEMT, MMIC.**

I. INTRODUCTION

The need to enhance data transmission efficiency within constrained bandwidth is steadily escalating, particularly in light of recent advancements. Users are increasingly drawn to multimedia data, video streaming, and the ongoing revolution in Internet of Things technology. Consequently, the 5^{th} generation of mobile communication will incorporate a range of technologies to realize its stated objectives. Some of the technologies are: beam forming, carrier aggregation, massive multiple input multiple output (MIMO), and more complex modulation schemes, which produce a high peak to average power ratio (PAPR). The high PAPR requires the power amplifier to be backed off from the most efficient point into a region where the efficiency drops sharply to keep the linearity requirements of any communications standard. When the PA is operated in the back-off region less efficiency is obtained because large amount of supplied power is converted to heat. This shortcoming can be overcome by designing modern power amplifiers using efficiency enhancements technique so as to produce high efficiency at a large output power back-off (OBO). In the pursuit of such designs many studies are done in this field to obtain effective results.

In next generation wireless communication systems power amplifier (PA) plays a very important role for designers [1, 2]. This needs to be made efficient in the best possible way. The millimeter-wave circuits are more popular because of broader bandwidth offered by them. Recently for 5G applications, band allocation was done as ending frequencies of K band and starting frequencies of Ka band being named as 26 GHz band (24.25-27.5 GHz). The designing of Power Amplifier (PA) for this band is crucial as there is a trade-off between its complexity and better performance. The power generated by power amplifier decides the distance for signal reception. Due to high power handling and easy chip formation, GaN devices have gained popularity for millimeter-wave integrated circuit design. MMIC designing helps in reducing circuit complexity and size. High power GaN devices being operational at higher frequency demands MMIC designing which is perfectly matched at input, output and interstage. In high frequency MMIC design, matching networks play an important role.

A review article in [3] has discussed various techniques of power amplifier designing for cm-Wave and mm-Wave frequencies. The target frequency bands are 15 GHz and 28 GHz. Moreover, the choice of device technology for 5G PA designing is discussed based on the performance criterion of design. In earlier works, [4] discussed the designing of driver and high-power amplifier using GaN and CPW technique for Ka band, which shows good results for first iteration and deviation from target due to high transconductance g_m and nearer transmission lines (TL's). A GaN power amplifier with power chain in two stages is simulated in [5]. The output power of 21.4 dBm and PAE of 18% is achieved at 35 GHz. In [6, 7] corporate combiner structures are reported where initial designing of n-stage high power amplifier (HPA) is escalated to 2, 4, 8 level designing combining the output power at each stage to modify the K band power amplifier designing. To reduce the gate size one finger gate is reported in [8] to optimize PA performance and gate pitch length. Later a study was carried as [9] in order to compare the performance of various GaN technologies for InAlGaN and AlGaN based HEMT's where AlGaN based HEMT's have given good performance making the choice of device in this work according to state-of-the-art. A 5 W AlGaN/GaN PA for downlink applications of LEO satellites is in [10] with a TL and Capacitor based output matching networks.

For this work, 150 nm GaN HEMT provided by United Monolithic Semiconductor (UMS) has been chosen. Using the same device [11] presents the simulated results and first small-signal on-wafer measurements of two MMIC PA's, for Ka band applications. The three-stages MMIC 1 and MMIC 2 are operating within a bandwidth of (27.5-31 GHz) and (37-39.5 GHz), respectively. They demonstrate a saturated output power of 40 dBm and 38 dBm, respectively over these bandwidths. Each stage use 8×50 μm gate width HEMTs fabricated with a 0.15 μm gate length on 70 μm thick SiC substrate. In order to achieve these goals, a reac-

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tively matched PA-based on three stages with 2 HEMT's at the 1st stage, 4 HEMT's at the 2nd stage and 8 HEMT's at the output stage was chosen. Similar work is presented in [12] which describes the main characteristics of the new GaN-on-SiC technology. The results of two different MMIC's are reported: a 29.5-36 GHz, 3 stage, 9 W HPA and a 15.5-18.5 GHz, 2 stage, 20 W HPA. In [13] design measurement results of a MMIC PA, for Ka band applications are presented. The three-stages MMIC is operating within a bandwidth of (25-31 GHz)and demonstrate over this bandwidth a saturated output power of 40 dBm. Each stage uses 8×50 μm gate width HEMT's.

The proposed amplifier is intended for use in 5G communication systems of the present scenario. The presented paper is organized as follows, biasing network and matching network discussed in Section II are designed after analyzing the biasing requirements and input-output impedance's. The proposed power amplifier performance is discussed in Section III with gain, output power and PAE, along with harmonics and adjacent channel leakage ratio (ACLR) study. The paper ends with conclusion in Section IV.

II. Power Amplifier Design

For the designing of power amplifier, GaN HEMT on SiC designed by UMS is used. The non-linear model of the device, provided by the manufacturer is applied for simulations performed in RF and Microwave CAD Advanced Design System (ADS). For the operating range of 24.25-27.5 GHz, device characterization is performed. For operating the device in Class-B biasing voltage levels are chosen as V_d= 20 V, V_g= -1.2 V for drain quiescent current (I_q) of 350 mA. Class B is chosen in order to create a basis for further Class-F amplification. For stability of network, a series RC pair is used as R = 670 Ω and C = 0.165 pF. The device size is chosen as 8×75 μm for generating 600 μm gate periphery such that the designed amplifier can be used as power stage while designing multistage amplifier. In order to find the optimum impedance at input and output of HEMT, loadpull analysis simulations were carried out.

A. Biasing Network Design

The selection of an appropriate biasing point is a crucial part of PA design. The DC bias network specifies the PA performance over temperature effects at the gate and current stabilization with R_{th} (thermal resistance). The amplifier should operate within the bounds of its operating point (V_g = -1.2 V) over the whole frequency range of operation in order to maintain a stable DC network. This helps to block unrestrained oscillations which reduces linearity, and finally produces distorted output. Stubs, lumped capacitors, λ/4 transmission lines, and microstrip components are typically used in the construction of bias networks (if required). In this work, two stage L-type biasing structure with quarter wave TL and bypass capacitors (C) is designed as shown in Fig. 1.

B. Load-Pull Analysis

It is necessary that the device should be perfectly matched to the source and load in order to maximize its performance. For proper matching of impedance, specialized impedance

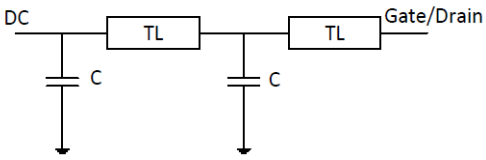

Fig. 1: Two stage L-type biasing network with Quarter Wave TL and Capacitor to transmit the DC voltage at drain and gate while blocking the RF

transformers are required which can down or up convert the 50 Ω to device impedance and vice versa. Filters provide a very good solution for impedance transformation as they offer less losses and high performance for the desired frequency. Low pass filters (LPF) and high pass filters (HPF) are a better choice in terms of their simple design but they generate harmonics in amplifier output. Thus at such high frequencies band pass filter (BPF) becomes a suitable choice as it offers broadband matching with lesser harmonics. After performing load/source pull matching, BPF is designed for input and output impedance's as Z_s (2.136+j2.279) and Z_l (8.9+j4.437) respectively as in Fig. 2 and Fig. 4. Designing is done based (1) for input impedance of transmission line with βl as electrical length, Z_0 characteristic impedance and Z_L load impedance.

$$Z_i(l) = Z_0 \frac{Z_L + jZ_0 tan\beta l}{Z_0 + jZ_L tan\beta l} \tag{1}$$

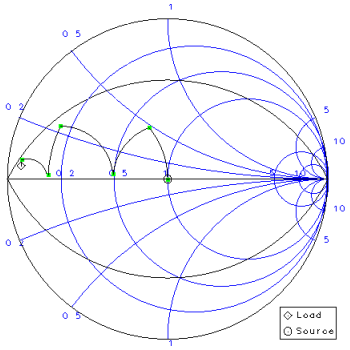

Fig. 2 Input matching network design on smith chart using open stub

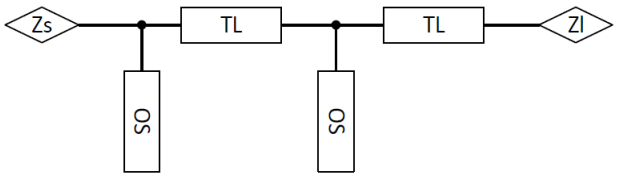

Fig. 3 Designed band pass filter as input matching network

Designing of matching network shown in Fig. 3 and Fig. 5 is performed with the following steps:

a. A 4 order LPF prototype lumped component (L-C) network is designed.

b. The LPF is converted to BPF using lumped element conversion technique.

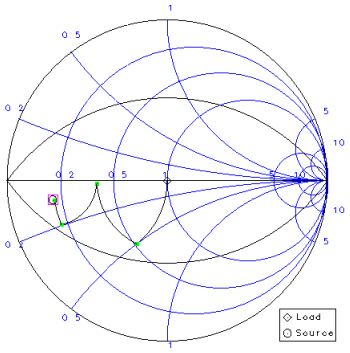

Fig. 4 Output matching network design on smith chart using open stub

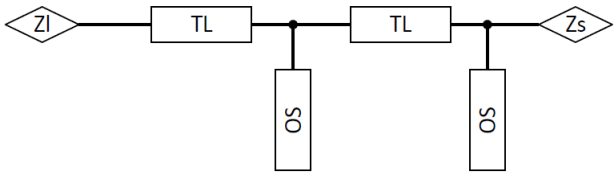

Fig. 5 Designed band pass filter as output matching network

c. Kuroda and Richard identities are used to convert LC network to equivalent QWTL (Quarter wave transmission line) with characteristic impedance of 50 Ω, with the transformation factor n^2 as in (2).

$$n^2 = 1 + \frac{Z_{o1}}{Z_{o2}} = 1.504 \tag{2}$$

d. The impedance and frequency scaling is performed on the transformed circuit.

e. The final obtained topology is then transformed from complex to real and optimized in order to attain the S-parameter performance as in Fig. 6 for the designed input and output matching networks respectively. It can be seen that the designed matching networks are offering good insertion loss for the operating band for power amplifier.

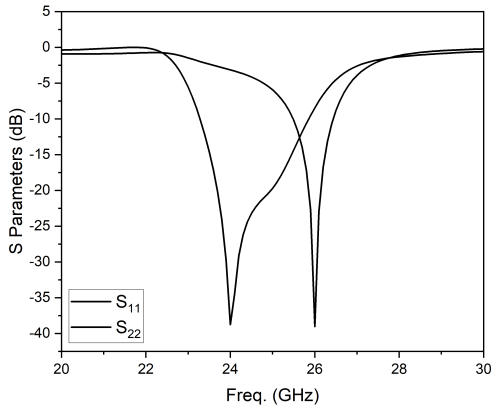

Fig. 6: S-parameters for designed Input matching network and output matching network with open stub

III. Power Amplifier Analysis

The proposed power amplifier is designed on GaN HEMT with L-type biasing network, biasing points and band pass impedance transformer as shown in Fig. 7. The design re-

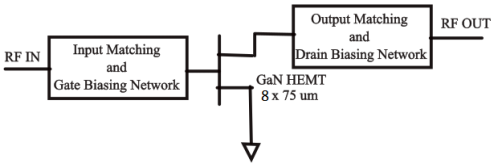

Fig. 7: Common Source amplifier with 8 x 75 μm device size, Band Pass Filter in IMN and OMN, TL-C Biasing network with Class-B biasing points

sembles to common source amplifier with class B biasing. Impedance matching is done with transmission lines and to maintain the Q factor open stubs are used. Open stub matching network design helps in reducing inductive effects and Q factor. A parallel RC network helps achieving stability for gate of HEMT. The design operates for the 26 GHz band with a larger gate periphery (8×75 μm) in order to maximize power output so that it can be used as power stage while designing multistage amplifier. Smaller gate periphery will provide high gain and is used at driver stage. The design is then converted to MMIC as shown in Fig. 8 for post layout simulations to validate the results keeping in mind all the DRC and space constraints.

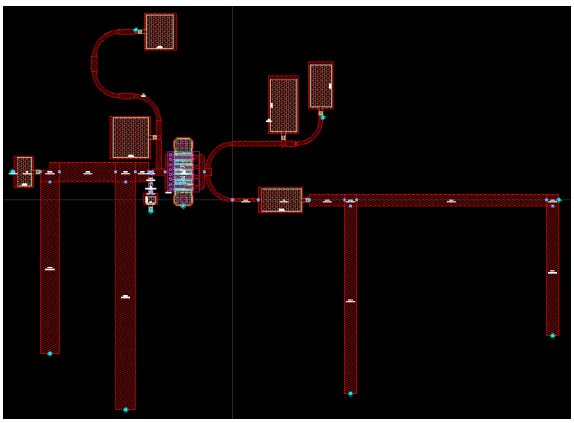

Fig. 8 Layout of proposed power amplifier for EM simulations

The small signal performance can be seen in Fig. 9 where input return loss is less than -10 dB for the frequency range 23.6-27.4 GHz. For post layout simulations this value is shifted to 21-24.3 GHz. The frequency shift is due to high sensitivity of the passive components and circuit design. Further the small line spacing between high power TL's, adds up to the issue. The results shows that proposed amplifier is suitable for the 26 GHz band of 5G communications with small signal gain to a maximum of 11 dB. The small signal gain is flat as the gain flatness factor is 0.91 dB which is near to 1. For any efficient amplifier gain should be as flat as possible which is achieved in proposed amplifier. Also the effect of band pass filter type matching network can be seen in small signal gain and return loss graph.

Apparently, it can be observed that proposed amplifier is capable of providing a power gain of 8.48 dB at 1 dB power

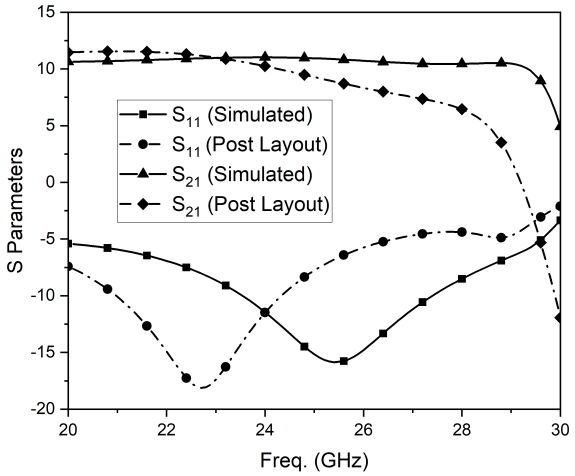

Fig. 9: Return loss and small signal gain for proposed single stage power amplifier

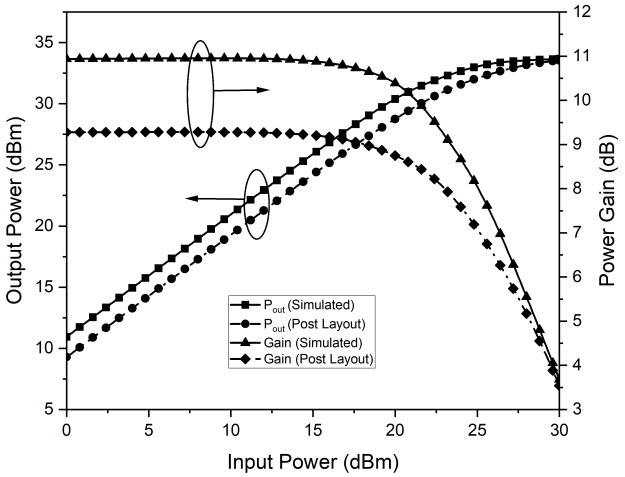

Fig. 10: Power output and power gain of proposed single stage PA with improved linearity an 1 dB compression at 20 dBm.

compression (P_{1dB}) as shown in Fig. 10. At this P_{1dB} point proposed amplifier is generating 31.35 dBm output power (i.e. 1.36 W) in the same figure. A linear PA reflects high value of IP3 at 1 dB compression point. When the amplifier is operated with two tone non linear input then third order harmonics play a very important role. These values try to match the fundamental signal and are known as IP3 (Third-Order Intercept). The standard difference between the values of IP3 and output power at 1 dB is 10 dB. The proposed amplifier gives this difference of 8.32 dB when simulated for IP3. Moreover the slope of the input power vs output power graph is 0.99. These factors supports the fact that the designed PA is linear.

The proposed PA is able to amplify the input power with 26% PAE and is having a 29% DC to RF conversion efficiency or drain efficiency as in Fig. 11. These values of efficiency are taken at P_{1dB} as after this value of input power the amplifier drops into non linear region and has gain compression. All these values for PA performance are considered from the post layout EM simulation.

While discussing class B type of amplifier design, harmonics play a very important role. The output voltage (power) at various harmonics can be seen in Fig. 12 where

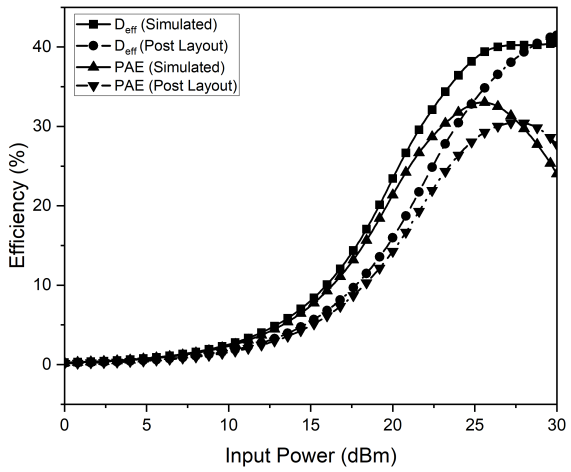

Fig. 11: Power added efficiency and drain efficiency for proposed power amplifier.

maximum value lies with fundamental frequency and higher order harmonics are nullified. The designed amplifier is maintaining unconditional stability in the whole frequency range with value >1 as shown in Fig. 13.

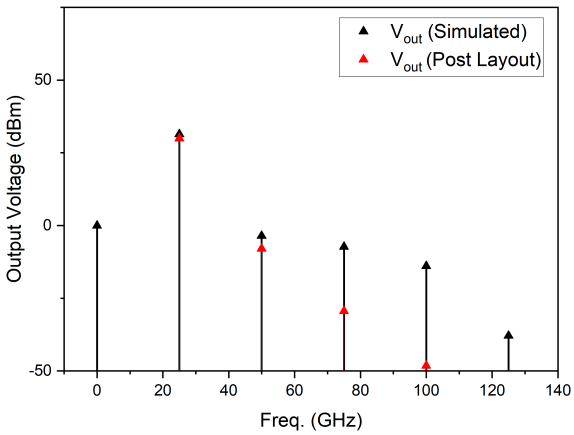

Fig. 12: Output voltage (dBm) or output power w.r.t. frequency for proposed power amplifier

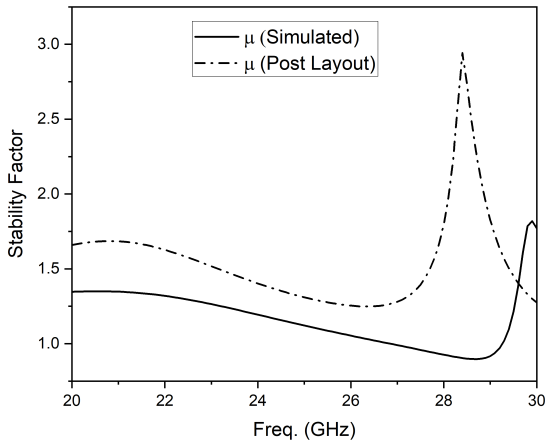

Fig. 13 Stability factor for proposed power amplifier.

The designed layout is operated with a modulating signal of 64-QAM with 400 MHz carrier frequency on the Virtual Test Bench setup. The power spectrum generated is shown

in Fig. 14 where for 400 MHz band adjacent channel power ratio is around -130 dBm which signifies less leakage into nearby channels.

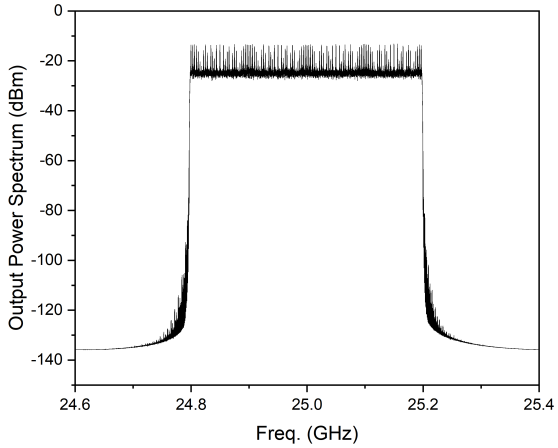

Fig. 14 Power spectral density for 400 MHz carrier.

The proposed amplifier is compared with similar works on 150 nm GaN HEMT for high frequency application in Table I. The designed topology is a single stage common source amplifier. On the contrary other presented works are complex multi-stage amplifier. In [13, 14, 15] corporate combiner topology where FET's are arranged in 2:4:8 topology, have reported less PAE than the proposed amplifier. The commercially available PA by UMS foundry on same FET is presented in [16] which is a 3 stage amplifier having similar performance. Designs from [13, 14, 15, 16] offers good performance parameters at the cost of more FET's. The proposed design matches their performance by using only single FET. This reduces the chip area and complexity of the circuit by many folds. The proposed amplifier when extrapolated to multi stage, results will improve. This shows that the designed band pass filter impedance transformer is able to provide an effective solution for PA designing.

Table I.: Comparison of presented work with reported power amplifier on same Technology

Ref.	Freq. (GHz)	PAE %	Gain (dB)	P_{out} (dBm)	No of FET's	Chip Area (mm^2)
[13]	25-31	25	21	40	14	17.5
[14]	25-29	25-28	25	32-40	7 & 14	13.8 & 23.75
[15]	24-28	30-35	19-21	38.5-39.5	6	13.5
[16]	27.5-31.5	25	24	41	3	16.5
This Work	**23.5-27.30**	**26**	**11**	**31.35**	**1**	**4.3**

IV. Conclusion

A Ka band power amplifier is designed, using UMS GH15 GaN HEMT with 150 nm technology, in commercially available Keysight ADS software. The proposed power amplifier is a single stage common source topology with 1.36 W output power, 26% PAE and linear power gain of 8.48 dB for 5G applications. To resolve the non-linearity issues of high frequency power amplifiers, this designed PA provides good linearity upto P_{1dB} point by generating IP3 of 39.67 dBm. The MMIC design of the proposed power amplifier shows a reduced chip size of 4.3 mm^2, which is highly considerate at such high frequencies. Complexity issues for Ka band are resolved with the help of easy matching, biasing and amplifier design topologies. Our design is a single stage amplifier and looking at the deliverable of the proposed amplifier, one can extrapolate that the design will be suitable for 5G applications.

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