A Novel Method of Digital-to-Analog Converter Combination for Precise Digital Control in Closed Loop Systems

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Abstract— **For precise digital control applications, high-resolution feedback is essential to achieve the required performance. Precise control systems with analog input-output and digital processing are generally limited by the resolution of digital to analog converter (DAC). DACs available for space use are limited in terms of resolution and performance. This paper presents a novel approach of combining two DACs to achieve higher resolution in closed-loop control systems. DACs can be combined with an overlapping range such that the nonlinearity of higher significant DAC does not cause oscillations and instability when lower significant DAC rolls over. A flowchart of the algorithm for combining two DACs is presented, along with a detailed analysis. Simulation results are also shown elaborating on the behaviour of DACs in non-overlapping and overlapping combination methods. The non-overlapping combination may result in oscillations, while the overlapping combination can settle the loop after a small settling time. An implementation example of a digital lock-in amplifier for the rubidium atomic clock, showing the realization of a coarse-fine DAC combination to achieve 20-bit resolution with two 12-bit DACs, is also presented. This approach will result in achieving better performance in small-bandwidth digital control systems.**

***Index Terms*— High-resolution control, digital-to-analog converters (DACs), coarse-fine DAC combination, digital lock-in amplifier, differential nonlinearity (DNL), Integral nonlinearity (INL)**

I. Introduction

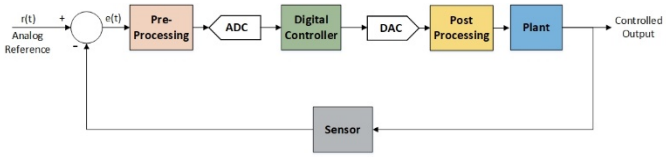
In the current scenario, digital techniques are replacing many analog methods because of significant advantages like flexibility, ease of design, immunity to noise, distortion, and interference, less sensitivity to temperature and process variations, etc. Digital control systems provide the implementation of more complex and efficient algorithms at a lesser cost. However, the quantization effects are the major limiting factors in implementing digital control [1][2].

There are mainly four finite wordlength effects of major concern for digital systems: 1. input/output quantization (resolution of mixed-signal converters), 2. coefficient quantization, 3. quantization of output of arithmetic operations (roundoff errors), and 4. saturation of the digital word (overflow and underflow error) [3]. Digital control systems with analog input and output use analog-to-digital converters (ADCs), digital processors, and digital-to-analog converters (DACs). Coefficient wordlength can be optimized such that the digital processor is satisfying the performance requirements while the effects of quantization of arithmetic operations and saturation of the words can be mitigated by various digital signal processing techniques [4][5]. However, the quantization of input due to ADC and output due to DAC becomes a cause of prime concern for precise closed-loop applications.

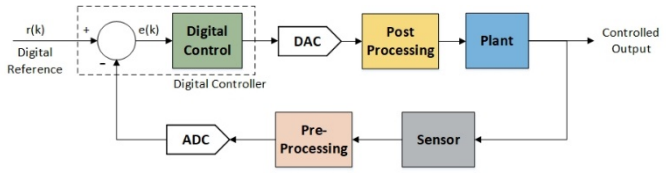
Dithering and noise shaping techniques are used together with oversampling to optimize the performance of ADC [6][7]. The dithering technique is also used in DAC to improve its resolution. Dithering mainly serves the purpose of increasing the effective resolution and reducing nonlinearity effects by (i) decorrelating quantization errors from the input signals and (ii) smoothing the nonlinearity of DAC [8][9][10][11][12]. However, the dithering technique demands additional circuitry like a dither generator, notch or other filters, secondary subtracting DAC, etc. Although dithering may provide around 10-12 dB (about 2 bits) of improvement in DAC resolution, for precise control, even higher resolution may be required.

High-resolution DACs are available for commercial use, but for space applications, the resolution of available DACs is limited. Even with many commercial precision DACs, the nonlinearity performance is poor, which may pose limitations in their use for closed-loop applications.

Fig. 1 shows fundamental system-level block diagrams of the digital control systems with the analog plant. The comparison of set point/reference and plant output can be performed either in the analog domain or the digital domain as shown in Fig. 1 (a) and (b) respectively. The output of the plant is analog which is digitized before feeding to the digital controller and the output of the digital controller is converted to analog to feed to the plant.



(a) Digital control system with analog reference



(b) Digital control system with digital reference

Fig. 1. Block diagrams of the digital control system. ADC and DAC are used around digital controller to convert the signals from/to analog to/from digital.

The postprocessing after DAC generally includes a reconstruction filter and scaling circuit as per the system requirements. The pre-processing before ADC generally includes an anti-aliasing filter and input scaling to occupy the ADC full-

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scale range. A sensor is required to monitor the controlled output. It can be seen from the block diagrams that DAC output is fed as feedback to the plant. DAC resolution plays a significant role as its resolution defines a limit on the precision of the control. This paper presents a novel approach of getting high-resolution control in closed-loop systems by combining two low-resolution DACs.

The paper is organized as follows. Section II briefs about basic requirements for precision digital closed-loop applications, and section III introduces the novel concept of combining DACs for high-resolution digital feedback control. Section IV presents the coarse-fine DAC algorithm and calculations for the required number of overlapping bits. Section V presents simulation results for DAC behaviour in overlapping and non-overlapping combination methods. An implementation example and its results are described in Section VI. The conclusion for the presented approach of achieving precise control in closed-loop systems is given in section VII.

II. Digital Control Systems

Digital control systems like precision temperature controllers, positioning systems, calibration apparatus, laser trimmers, digital servos, etc., require high-resolution feedback to meet the required performance. System designers of such systems usually require very high-resolution ADC and DAC. In the digital control loop, the sense resolution is governed by ADC whereas the control resolution is governed by DAC. To avoid limit cycle oscillations, the control resolution is kept equal to or slightly higher than the sense resolution. In the case of the digital reference, the resolution of reference signal representation must be the same as that of the ADC. If the precision of the reference signal is higher than ADC resolution, the control error will never go to zero, and therefore limit cycle oscillations will occur [13][14].

DACs in feedback need to be monotonic over the entire range of digital codes. DNL (differential nonlinearity) of more than +1 LSB (least significant bit) does not make DAC non-monotonic but is still undesirable in a closed loop as it may cause the loop to oscillate between two consecutive codes in a quest to achieve the desired feedback value. DAC with negative DNL of more than -1 LSB may cause oscillations by changing negative feedback to positive feedback. DAC with $|DNL| \leq 1$ LSB has guaranteed monotonicity [15]. Besides monotonicity, conversion and settling times are other important parameters to consider if the loop is tightly closed with a very fast time constant. Distribution of DNL over output codes also matters and may change the magnitude and time characteristics of oscillations due to nonlinearity effects in the closed loop. Worst-case INL specifications restrict the growth of cumulative DNL error.

As very high-resolution mixed signal devices for space applications are not readily available, designers generally use various techniques to improve the resolution like oversampling, dithering etc. However, dithering techniques can help to increase only a few bits of DAC resolution. Thus, a different approach has to be adapted to increase the resolution to the required level. Further, many commercially available high-resolution DACs do not have good nonlinearity performance and monotonicity and thus make them unsuitable for closed-loop applications. The approach presented in this paper can be used with such DACs to make them suitable for closed-loop applications.

III. Combining DACs for Higher Resolution

The two DACs can be combined in a 'coarse-fine' combination in which a higher DAC (HDAC) provides a coarser resolution and a lower DAC (LDAC) provides a finer resolution. The analog outputs of the two DACs are combined by an adder circuit with an appropriate scaling to achieve a higher resolution output. The digital controller provides a high-resolution digital value. This high-resolution digital value can be divided in two ways for the inputs of the two DACs:

a. Non-overlapping approach: $m+n$ bit number is divided into two numbers of m bits and n bits for m-bit HDAC and n-bit LDAC respectively, as shown in Fig. 2.
b. Overlapping approach: $m+n-c$ bit number is divided into two numbers of m and n bits with overlap of c bits for m-bit HDAC and n-bit LDAC respectively, as shown in Fig. 3.

In Fig. 2, it is assumed that both DACs have same full-scale ranges. However, they can be different also, which may require different scaling to be used while combining their outputs. As there is no overlap between DAC ranges, there may be oscillations in the closed-loop operation whenever the lower DAC rolls over. When the lower DAC rolls over, the higher DAC transits to a new value, and due to the differential nonlinearity of the higher DAC, the loop may oscillate to achieve the desired feedback control.

The above problem can be mitigated by overlapping the ranges of these DACs, as shown in Fig. 3. In this overlapping DAC combination, the lower DAC can be adjusted to settle at the desired value avoiding oscillations due to roll-over of lower DAC and DNL of higher DAC. The overlapping bits can be decided based on the DNL and INL values of the selected higher DAC.

It should be noted that in both overlapping and non-overlapping methods, the lower DAC has to be monotonic for closed-loop applications. In this paper, 'LSB^h' means the LSB magnitude of the higher DAC, while 'lsb^l' denotes the LSB magnitude of the combined output of two DACs, the same as the LSB magnitude of the lower DAC. The relation between these two quantities is given below:

$$LSB^h = 2^{n-c} lsb^l, \tag{1}$$

where 'c' is the number of overlapping bits, it is zero for the non-overlapping case.

After scaling, the full-scale range of lower DAC with overlapping of c bits is 2^c LSB^h. Thus, 2 bits of overlap means that the lower DAC range after scaling is 4 LSB^h. This overlapping can be utilized by bringing the lower DAC near a particular value every time the higher DAC value needs to be changed. Let's say that particular range of values is the

'Fallback region' (FBR). FBR is only of 1 LSB^h and is chosen such that lower DAC has ranges available on both sides of FBR to correct for nonlinearity errors of the higher DAC. It is to be noted that this range is only for the first time whenever the higher DAC value needs to be changed.

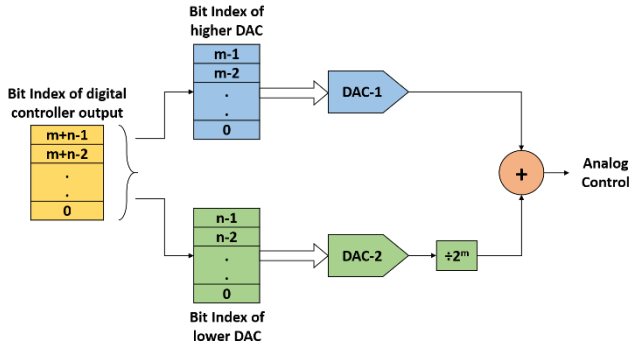

Fig. 2. Non-overlapping approach of DAC Combination

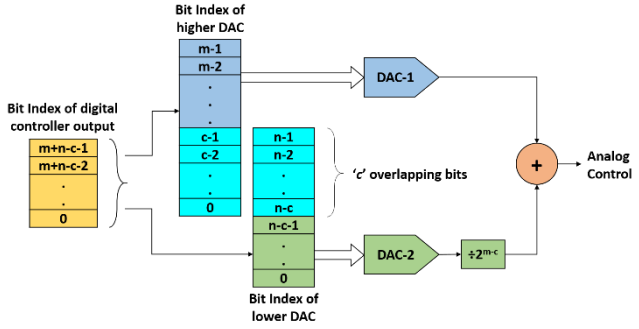

Fig. 3. Overlapping approach of DAC Combination

IV. Required Overlapping Bits and Algorithm for DAC Combination

The initial lower DAC setting should be within the fallback region (FBR). However, subsequent to that, lower DAC value can vary over its full range till the desired output can be achieved by varying lower DAC only, i.e. until the next time when a higher DAC value needs to be changed. Fig. 4 gives a pictorial representation of lower DAC ranges in terms of LSB^h (LSB of higher DAC). The total range of lower DAC is 2^c LSB^h - lsb^l. For the sake of simplicity, the '-lsb^l' term can be ignored, and it can be written that

$$l + u + 1 = 2^c. \tag{2}$$

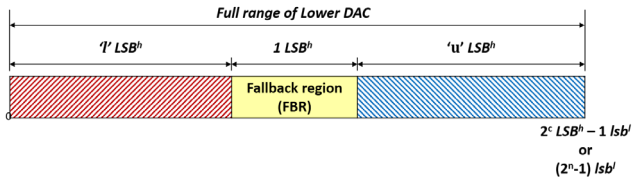

Fig. 4. Lower DAC range

Higher DAC value needs to be changed under two conditions: (a) underflow of lower DAC and (b) overflow of lower DAC. Analysis of both these conditions and how lower DAC can compensate for worst-case higher DAC DNL/INL errors are described below.

a. Lower DAC Underflow

When the lower DAC range saturates and underflows, the higher DAC value needs to be reduced by $\lfloor l+1 \rfloor$ LSBs. Here $\lfloor x \rfloor$ represents the integer part of x. At that time, the lower DAC is brought to FBR depending on the new value to be set. If we consider that higher DAC had worst-case DNL values (either DNL_{max} or DNL_{min}) at all these $\lfloor l+1 \rfloor$ LSBs by which it was reduced, then it would be the worst-case DNL effect of higher DAC that lower DAC should be able to compensate without any oscillations.

Thus, the values of l and u can be decided as follows:

$$l \geq \lfloor l+1 \rfloor d_n \text{ and } u \geq \lfloor l+1 \rfloor d_p \tag{3}$$

where, $d_n = |DNL_{min}|$ and $d_p = DNL_{max}$.

DNL_{min} and DNL_{max} are usually provided in the datasheet and are expressed in terms of LSBs.

b. Lower DAC Overflow

When the lower DAC range saturates and overflows, the higher DAC value needs to be increased by $\lfloor u+1 \rfloor$ LSBs. At that time, the lower DAC is brought to FBR depending on the new value to be set. Similar to the underflow case, lower DAC should compensate for the worst-case DNL effect of higher DAC without causing steady-state oscillations. The values of l and u can be decided as follows:

$$l \geq \lfloor u+1 \rfloor d_p \text{and } u \geq \lfloor u+1 \rfloor d_n \tag{4}$$

From (3) and (4), we can write that

$$l \geq max\left\{\lfloor l+1 \rfloor d_n, \lfloor u+1 \rfloor d_p\right\}$$
$$\text{and} \tag{5}$$
$$u \geq max\left\{\lfloor l+1 \rfloor d_p, \lfloor u+1 \rfloor d_n\right\}$$

It is evident that when a higher DAC value changes by any amount, the worst-case nonlinearity error cannot exceed the INL range (INL_r). INL range is defined as

$$INL_r = INL_{max} - INL_{min} \tag{6}$$

Thus, from (5) and (6), it can be written as

$$l \geq min\left\{INL_r, max\left\{\lfloor l+1 \rfloor d_n, \lfloor u+1 \rfloor d_p\right\}\right\}$$
$$\text{and} \tag{7}$$
$$u \geq min\left\{INL_r, max\left\{\lfloor l+1 \rfloor d_p, \lfloor u+1 \rfloor d_n\right\}\right\}$$

We can infer that d_p and d_n should be less than 1 (one) LSB for satisfying (5). If any/both of them is/are greater than or equal to 1 (one) LSB, l and u should be chosen based on INL_r, as can also be seen from (7). If d_p and d_n both are less than 1

LSB, i.e., higher DAC is monotonous, l and u value may be determined as

$$l, u \geq \frac{d}{1-d}, \tag{8}$$

where, $d = max.\{d_p, d_n\}$.

From (2) and (8), the number of overlapping bits can be determined as

$$c \geq log_2\left(\frac{1+d}{1-d}\right). \tag{9}$$

However, if INL_r is smaller than the value obtained in (8), the number of overlapping bits should be chosen as

$$c \geq log_2(2\,INL_r + 1) \tag{10}$$

The number of overlapping bits, as calculated from (9) and (10), may not be optimum as it is for the worst-case conditions, but it does provide a convenient means of obtaining a satisfactory solution. Most of the monotonic DAC manufacturers mention DNL values as ±1 LSB. As mentioned above, if d ≥ 1 LSB, (7) and (10) should be used to calculate l, u, and the number of overlapping bits; otherwise, (7) to (10) should be used.

Fig. 5 shows the plot of the required overlapping bits calculated from (9). It can be seen that as the maximum DNL magnitude approaches 1 LSB, the required overlapping bits increase exponentially. However, as mentioned earlier, 'c' is limited by INL_r. In most DACs available for commercial or space applications, maximum and minimum DNL or INL values are much higher than the typical range. Depending on the application and operating conditions, the designer can choose the worst-case numbers or typical values.

The overlapping bits required for combining two DACs with maximum or typical specifications for various available DACs are shown in Table 1. It can be seen that there is a considerable difference between overlapping bits requirement for worst-case and typical specifications. One important point to note is that fewer overlapping bits would give an advantage of better final resolution and cost, but it also means that the higher DAC value would need to be changed frequently than for more overlapping bits. This incurs frequent settling processes to compensate for the effect of higher DAC nonlinearity. Thus, depending on the application and operating conditions, one should make a choice for the optimum number of overlapping bits.

Fig. 6 shows the flowchart of the algorithm for deriving inputs of each DAC in the overlapping combination method. The flowchart is given for the combined output of m+n-c bits from the digital controller, which is adjusted in m-bit coarse (higher) DAC, n-bit fine (lower) DAC with overlapping of c bits. The DACs can be initialized as per the system requirement at the start-up (or after reset).

As mentioned earlier, in the overlapping DAC combination, if the lower DAC is monotonic and the higher DAC is non-monotonic, the combined output would behave as monotonic due to overlapping and closed-loop action. However, the loop would require some time to allow the lower DAC to compensate for the nonlinearity error of the higher DAC. A similar behavior is also true when both DACs are monotonic as the combination of two monotonic DACs may also become non-monotonic, but again, the lower DAC would compensate for it and would not allow the loop to oscillate. Generally, the loops with small bandwidths can tolerate such a settling process in the loop.

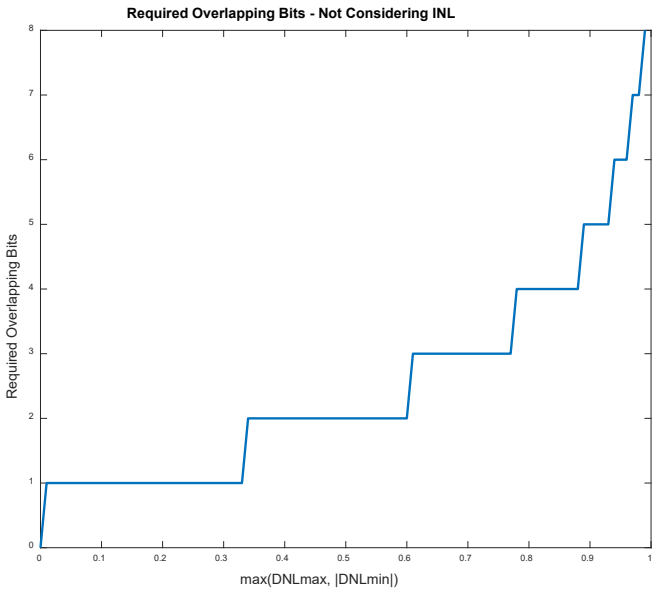

Fig. 5: Overlapping bits required for monotonic DACs

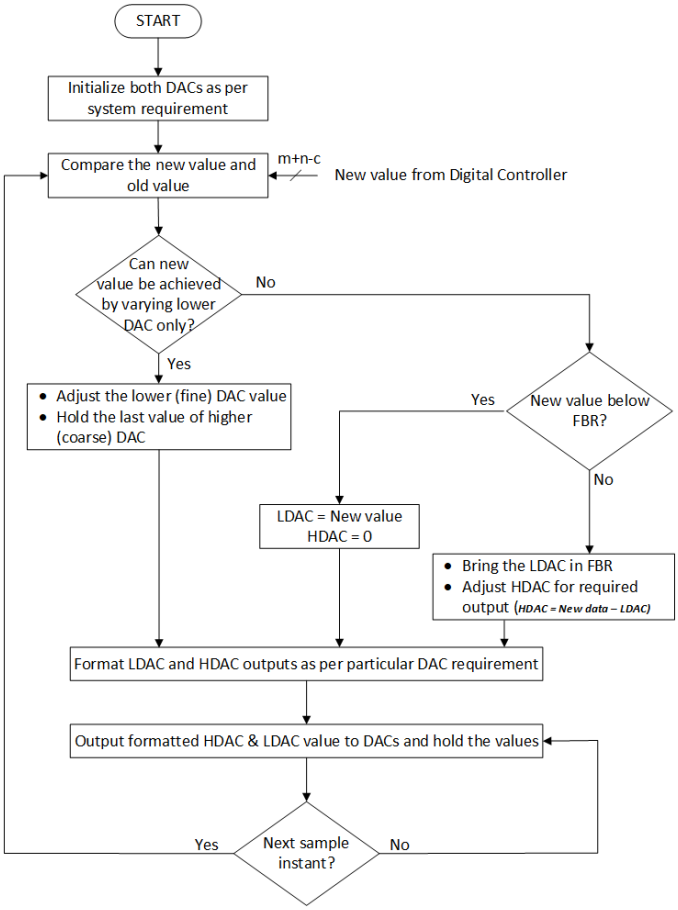

Fig. 6: Flowchart of overlapping DAC combination algorithm

Table 1: Required overlapping bits for various DAC parts

DAC	DAC121S*	DAC9881S	DAC8411	AD5721	AD667J	AD7840S
Make	Texas Instruments (TI) Incorporated			Analog Devices, Inc.		
Resolution	12 bits	18 bits	16 bits	12 bits	12 bits	14 bits
DNL_{max}	+1	+2	+2	+0.5	+0.75	+0.9
DNL_{min}	-0.7	-1	-2	-0.5	-0.75	-0.9
INL_{max}	+8	+3	+12	+0.5	+0.75	+2
INL_{min}	-8	-3	-12	-0.5	-0.75	-2
Required '*c*'(worst-case)	***6***	***4***	***6***	***2***	***2***	***4***
DNL_{typ}	+0.21, -0.1	±0.75	±0.5	-	±0.5	-
INL_{typ}	±2.75	±2	±4	-	±0.5	-
Required '*c*' (typical)	***1***	***3***	***2***	***-***	***2***	***-***

* Space qualified DAC, DAC121S101QML-SP

It is imperative that combining two DACs or using a very high-resolution single DAC may not result in very high effective number of bits as it depends on many factors like board noise, flicker noise, thermal noise, loop noise, etc. However, the proposed method of combining two DACs is useful for precision closed-loop systems mainly dominated by white noise processes. Further, oversampling and dithering may also be used intelligently along with the DAC combination approach for improving the linearity and noise performance.

I. Simulation of DAC Behaviour in Coarse-Fine Combination

We simulated the DAC behaviour in overlapping and non-overlapping combinations using MATLAB and Simulink, as shown in Fig. 7. For the non-overlapping case, the resolution of both the DACs are kept as 4 bits. For the overlapping case with an overlap of 2 bits, higher DAC resolution is kept as 4 bits while that of lower DAC is kept as 6 bits. Thus, the combined resolution of 8 bits is achieved in both cases. The full-scale range is taken as eight units for individual DACs and also for the combined output. The full-scale range is bipolar, i.e., from -4 to +4 (unreachable). It is clear that the overlapping method requires higher resolution DACs than that in the non-overlapping case to produce the same combined resolution. It also requires memory to store previous digital words of higher and lower DACs.

We did simulations for both triangular and sinusoidal signals. The discrete signal is quantized and encoded through an 8-bit quantizer and encoder. The encoder formats the digital data as per the Bipolar Offset Binary (BOB) coding scheme. The digital data is then given to the DAC combining algorithm, which is implemented in function as per the flowchart of Fig. 6. The function block outputs the digital codes for higher and lower bipolar output DACs, again in BOB format. BOB format is taken as an example for the simulation. DACs are also implemented as MATLAB functions. The outputs of the DACs are combined as shown in Fig. 2 and Fig. 3. Input digital code, outputs of the DAC combining algorithm, and the final combined output are tapped in the simulation model. These tapped signals for triangular and sinusoidal inputs are shown in Fig. 8 and Fig. 10 for non-overlapping DAC combination, and in Fig. 9 and Fig. 11 for overlapping DAC combination.

The behaviour in the case of the non-overlapping combination is simple and similar to how a single DAC of 8-bit would behave. The higher DAC increases/decreases in the unit step while the lower DAC rolls over from maximum/minimum to minimum/maximum. The behaviour of the overlapping approach is not that straightforward. For the overlapping combination case, FBR was chosen as the center values for lower DAC, i.e., 24-39 out of 0-63. It can be noted that while input is increasing (for triangular input), lower DAC falls to 32, whereas, during the negative slope of triangular input, lower DAC falls to 31 post saturation. Obviously, the higher DAC changes more frequently in the non-overlapping cases compared to overlapping cases.

I. Implementation Example

Atomic Frequency Standards are timekeeping or time measurement standards that are the heart of satellite-based navigation systems. Space Application Centre, ISRO have developed the Indian Rubidium Atomic Frequency Standard (IRAFS) [16][17]. Fig. 12 shows the fundamental block diagram of IRAFS.

As shown in the figure, the output of the frequency source, Voltage Controlled Oven Compensated Crystal Oscillator (VC-OCXO), is frequency multiplied in the RF chain to generate a microwave field near the rubidium (Rb) ground state hyperfine resonance frequency ($\nu \approx 6.8347$ GHz for ^{87}Rb). The microwave field is frequency-modulated so that rubidium resonant absorption can be monitored by phase-sensitive detection [18]. The physics package (PP) is composed of (a) the lamp package, the light source, consisting of the Rb plasma lamp, the RF oscillator electronics, and the optical components, and (b) the cavity package, which contains the Rb cell along with filtering and focusing optics and a low-noise photodetector [17]. The error signal from the physics package indicates the difference between the frequency of VC-OCXO and rubidium atomic reference.

Digital lock-in amplifier (DLIA) feeds the required correction to the frequency source (VC-OCXO) based on this error signal [18][19]. DLIA provides a high-resolution frequency control voltage to VC-OCXO. This improves the stability of VC-OCXO by locking it to a stable atomic reference, thereby compensating for its drift and other long-term variations.

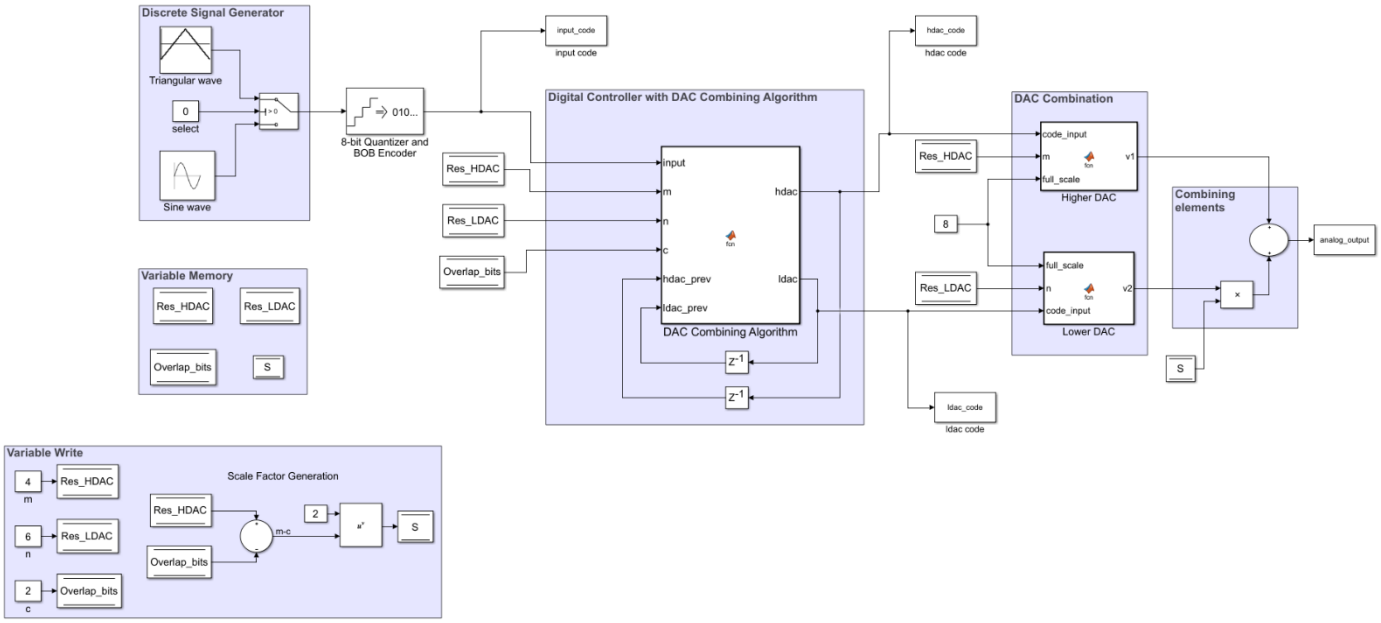

Fig. 7: Simulation Model for DAC behaviour under overlapping and non-overlapping combination

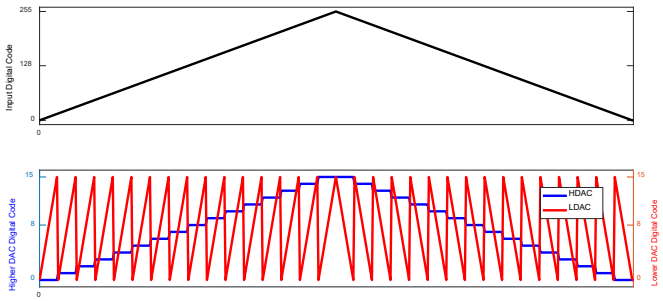

Fig. 8: Non-overlapping DAC combination behaviour (triangular input)

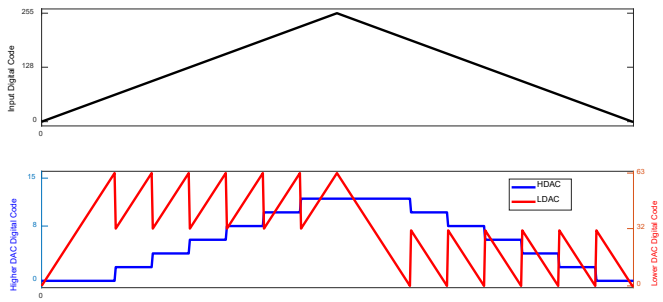

Fig. 9: Overlapping DAC combination behaviour (triangular input)

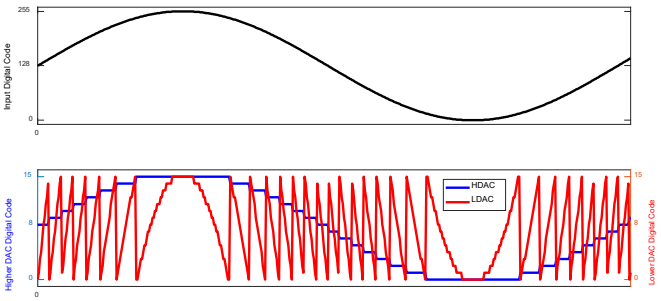

Fig. 10: Non-overlapping DAC combination behaviour (sinusoidal input)

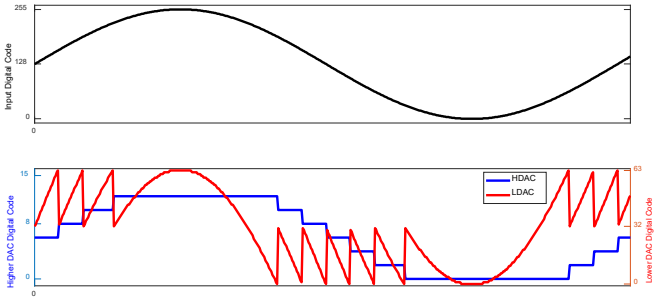

Fig. 11: Overlapping DAC combination behaviour (sinusoidal input)

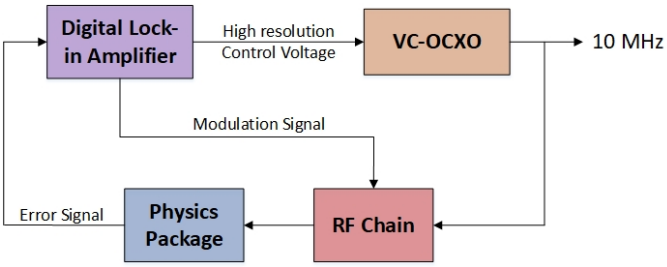

Fig. 12. Fundamental IRAFS Block Diagram

VC-OCXO frequency has to be stabilized at micro Hertz level for frequency stability of the order of 10^{-14} Hz/Hz. For its various merits over analog, the digital approach was selected for the implementation of the lock-in amplifier (LIA) [20]. Digital LIA requires a very high-resolution DAC (20 to 24 bits) to provide precise frequency control voltage [19]. The digital LIA hardware block diagram is shown in Fig. 13.

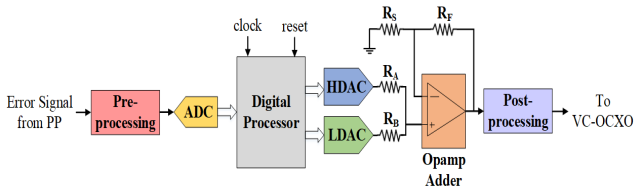

Fig. 13. Digital Lock-in Amplifier Hardware Block Diagram

To achieve high-resolution output and precise frequency control, we combined two DACs by overlapping coarse-fine combination [21]. Both DACs are the same part from the same manufacturer, TI make DAC121S101QML-SP [22]. These are space-qualified precision DACs with a resolution of 12 bits. As shown in Table 1, as per typical specifications, only 1 bit of overlapping is required, while as per worst-case specifications, 6 bits of overlapping is required. As the operating conditions are not severe and also to avoid frequent higher DAC change, overlapping bits are chosen as 4. Output of lower DAC is scaled by dividing it by 256 ($2^8 = 2^{12-4}$). The combined bit output is 20-bit providing a frequency resolution of around 5 µHz.

The output of the op-amp adder can be represented as

$$\therefore V_o = s_1 V_{hdac} + s_2 V_{ldac} \tag{11}$$

where $s_1 = \frac{R_B G}{R_A + R_B}$, $s_2 = \frac{R_A G}{R_A + R_B}$ and $G = 1 + \frac{R_F}{R_S}$.

V_{hdac} and V_{ldac} are voltage outputs from higher and lower DACs, respectively. s_1 and s_2 are scaling factors of higher and lower DAC outputs, respectively, R_A and R_B are the weighting resistors for the DACs' output as shown in Fig. 13. R_F and R_S are feedback and input resistors of the op-amp adder circuit, respectively. The ratio of the scaling factors of these DAC outputs is $\frac{R_B}{R_A}$ which is kept as 256 (2^8).

The IRAFS has been tested for many months in a thermovac chamber, and the stability of better than $2\text{x}10^{-12}$ @ 1 s, better than $2\text{x}10^{-13}$ @ 100 s, and better than $5\text{x}10^{-14}$ @ 10000 s is achieved over the mounting plate temperature range of -5 °C to +20 °C. They reliably meet the system requirements. For this particular application, overlapping of 4 bits was used as it meets the requirement. However, overlapping of 2 bits was also implemented and tested with the system, which provided similar performance as the performance was not limited by DAC resolution beyond 20 bits.

In the example presented here, the DACs used are voltage output DACs and thus combined by a non-inverting op-amp adder. Other adder configurations can also be used as per the application and supply requirements. For current output DACs, the outputs can be combined either by using the current node or by converting current to voltage at the output of each DAC before combining them by op-amp adder [23].

In this implementation example, the full-scale value of the combined output remains the same as the full-scale values of individual DACs. In the overlapping case, the output may go beyond the full-scale if both the DACs are at their maximum values, although this case should never occur in the closed-loop operation. If the subsequent system is prone to overvoltage damage, a fail-safe check should be put in the logic to prevent further failure.

II. Conclusion

High-resolution feedback is required to achieve the desired performance in precise digital control applications like temperature controllers, instruments, metrology systems, nanopositioning systems, medical electronics, servo control, etc. Digital control systems with analog input-output and digital processing are generally limited by the resolution of feedback control governed by data converters, especially digital-to-analog converters. In this paper, we have presented a method to combine two DACs to achieve higher resolution mitigating the oscillations due to the DAC nonlinearity effect.

DACs combined with overlapping ranges have a provision to correct the nonlinearity errors of the higher DAC by adjusting the lower DAC. The number of overlapping bits can be decided from the DNL and INL specifications of the higher DAC and the system requirements. When the higher DAC value needs to be changed, lower DAC output is brought to a range of values assuring sufficient range for mitigating nonlinearity effects of higher DAC. As the resolution of the combined result is the same as the resolution of the lower DAC, the lower DAC must be monotonic with |DNL| < 1 to avoid oscillations in the loop.

Simulations are presented in the paper showing DAC behaviour in overlapping and non-overlapping combinations. An algorithm flowchart and application example are also presented. The approach mentioned in the paper was successfully implemented and tested in IRAFS, achieving the desired performance. Two 12-bit DACs were used to provide higher resolution control voltage to the frequency source. DLIAs with overlapping coarse-fine DAC combination approaches with 20-bit and 22-bit combined DAC outputs were tested with two different IRAFS, and both performed quite satisfactorily.

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REFERENCES

[1] J. Slaughter, "Quantization errors in digital control systems," in *IEEE Transactions on Automatic Control*, vol. 9, no. 1, pp. 70-74, January 1964, doi: 10.1109/TAC.1964.1105624.
[2] A. Koivo, "Quantization error and design of digital control systems," in *IEEE Transactions on Automatic Control*, vol. 14, no. 1, pp. 55-58, February 1969, doi: 10.1109/TAC.1969.1099091.
[3] E.C. Ifeachor and B.W. Jervis, "Digital Signal Processing - A practical approach", 2nd edition, Prentice Hall, pp. 805-864.
[4] Pin Wah Wong, "Quantizations noise, fixed-point multiplicative roundoff noise, and dithering," *IEEE Transactions on Acoustics, Speed, and Signal Processing*, Vol. 38, No. 2, February 1990.
[5] A. Rajan, H S Jamadagni, A. Rao, "Minimizing quantization effects in digital filtering", IEEE, 2009.
[6] J.M. Dias Pereira, A. Cruz Serra and P. Girão, "Flexible ADC: A Dither and Oversampling Based Solution to Improve the Performance of ADC Systems".
[7] Overcoming Converter Nonlinearities with Dither, Appl. Notes, Analog Devices, USA.
[8] P. Carbone and D. Petri, "Effect of additive dither on the resolution of ideal quantizers," *IEEE Trans. Instrum.Meas.*, vol. 43, no. 3, pp. 389–396, Jun. 1994.
[9] S. P. Lipshitz, R. A. Wannamaker, and J. Vanderkooy, "Quantization and Dither: A Theoretical Survey," *J. Audio Eng. Soc.*, vol. 40, no. 5, pp. 355–375, 1992.
[10] J. Vanderkooy and S. P. Lipshitz, "Resolution below the least significant bit in digital systems with dither," *J. Audio Eng. Soc.*, vol. 32, no. 3, pp. 106–113, 1984.
[11] A. A. Eielsen and A. J. Fleming, "Improving Digital-to-analog Converter Linearity by Large High-frequency Dithering," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 6, pp. 1409-1420, June 2017, doi: 10.1109/TCSI.2016.2561778.
[12] G. Zames and N. A. Shneydor, "Dither in nonlinear systems," *IEEE Trans. Autom. Control*, vol. 21, no. 5, pp. 660–667, Oct. 1976.
[13] M. S. Fadali, A. Visioli, *Digital Control Engineering Analysis and Design*, 2nd ed. Elsevier, 2013, pp-494-500.
[14] A. V. Peterchev, S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM Converters", *IEEE transactions on power electronics*, vol. 18, no. 1, January 2003.
[15] W. Kester, The importance of data converter static specifications, Tutorial MT-010, Analog Devices Inc., 5 (2009).
[16] T. N. Bandi et al., "Indian Rubidium Atomic Frequency Standard (iRAFS) Development for Satellite Navigation," 2019 URSI Asia-Pacific Radio Science Conference (AP-RASC), New Delhi, India, 2019, pp. 1- 1.
[17] T.N. Bandi et al., "Advanced Space Rubidium atomic frequency standard for Satellite Navigation", GPS Solutions 26, 54 (2022).
[18] J. C. Camparo, "The Rubidium atomic clock and basic Research", Physics Today, 60, No. 11, 33 (2007).
[19] W. J. Riley, "Rubidium Frequency Standard Primer", pg. 11-12, 15-19, 58-60.
[20] PerkinElmer Inc, The digital lock-in amplifier (USA, 2000).
[21] Pratik Jain, et al, "Digital lock-in amplifier for space rubidium atomic clock", Rev. Sci. Instrum. 92, 124705 (2021).
[22] See https://www.ti.com/product/DAC121S101QML-SP for information about DAC.
[23] W. Kester, DAC Interface Fundamentals, Tutorial MT-019, Analog Devices Inc., 2009.