A Voltage-Gated Spin-Orbit Torque (VgSOT) Magnetic Tunnel Junction based Non-Volatile Flip Flop design for Low Energy Applications

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***Abstract*- In this paper, a Voltage-gated Spin-Orbit Torque based non-volatile flip-flop design has been discussed. The flip-flop consists of a conventional CMOS master latch used in normal operations, and a VgSOT-MTJ based slave latch has been considered for interim data saving during power-gating. The current circuit uses the same write current to write data into two magnetic tunnel junctions, saving 50% of storing energy. The proposed NVFF circuit has been simulated using Cadence Virtuoso 45nm. The performance parameters like energy consumption and delay during restore and store operations of VgSOT-MTJ based NVFF circuit have been analyzed in this paper and compared with SOT-MTJ based and STT-MTJ based NVFF circuits. Simulation results show that for the switching delay, VgSOT-MTJ based NVFF performs 40% and 58% better than SOT-MTJ NVFF and STT-MTJ based NVFFs, respectively during storing mode and 83% and 88% better than SOT-MTJ and STT-MTJ based NVFFs during restoring mode. In terms of energy consumption, during storing mode, VgSOT-MTJ based NVFF consumes 84% less energy than SOT-MTJ NVFF and 90 % less energy than STT-MTJ based NVFFs. During restoring mode, VgSOT-MTJ based NVFF consumes 70% and 80% less energy than SOT-MTJ NVFF and STT-MTJ, respectively.**

***Index Terms*- Non-Volatile Memories (NVM), Spin-Orbit Torque Magnetic Random-Access Memory (SOT-MRAM), Flip Flop (FF), Voltage gate SOT (VgSOT), Antiferromagnetic (AFM), Non-Volatile Flip Flop (NVFF).**

I. INTRODUCTION

The leakage current is becoming a bottleneck in the semiconductor industry, preventing the continuous scaling down of a transistor size as per Moore's law [1][2]. Due to the increase in leakage current, the standby power also increases [3]. One of the techniques to lower the leakage current [4] in a chip is to utilize the "zero VDD" mechanism in standby mode. However, this poses a problem in a volatile flip where stored data is lost for a zero Vdd scenario. Even though multiple new ideas, such as Variable threshold CMOS [5] and multi-threshold MCOS [6], have been proposed, leakage current has not yet been eliminated. This problem exists since they could not capitalize on the zero Vdd mechanism to store data in volatile flip-flops.

To overcome this drawback, researchers have started using the spin-based "MTJ" as a storage element to save the data in standby mode. Using MTJ also provides a non-volatility feature to these flip-flops and helps reduce energy consumption.

In general, a flip flop is utilized for internal memory cells to save and synchronize the information in FPGA computing and SOC circuits. So far, SRAM-based flip flops have been widely used in the industry. Since SRAM [7] is a volatile component, all of the data gets lost when the power goes down. From the SOC industry's point of view, it is essential to have data security in case of power failures or system crashes. Thus, non-volatile-based components [8][9][10] are required in flip-flops to improve the performance and data storage capability of circuits. Non-volatile flip flops are hybrid versions of traditional FFs currently used in industry. They use MOSFET transistors for normal operations and MTJs [11] for interim storage during the shutdown mode. Using components based on the MTJ principle provides advantages such as infinite endurance, CMOS compatibility, reduced leakage current and energy consumption, less area overhead [12], and non-volatility. In general, D-FF consists of a master and slave latch. The data gets stored onto MTJ (part of the slave latch) during the "Storing operation" before power down occurs and is restored during the "Restoring operation" after power is back on. Because of its desirable features, such as faster reading capability and zero standby current [13], Spin Transfer Torque (STT) MTJ [14] provides significant opportunities and capabilities for non-volatile data storage in NVFFs. However, significant challenges are present that limit STT-MTJ usage. For example, a complete current pulse is needed for a successful write operation, which consumes considerable energy. Also, thermal fluctuations drastically affect the magnetic incubation

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time in MTJ [15]. In addition, as high voltage/current is applied to the MTJs tunnel barrier during a write operation, STT-MTJ suffers from read disturbance and endurance issues [16][17][18][19][20]. Recently, Voltage gate Spin-orbit Torque (VgSOT-MTJ) and Spin-orbit torque [21] have been extensively analyzed as they possess lesser incubation time, higher endurance capability, and initial solid magnetization.

This research paper presents a VgSOT-based energy-efficient flip flop for power gating applications. An additional circuit has been incorporated, which uses a single current pulse to write two MTJs simultaneously, thus requiring lesser write energy. The flip flop presented is a hybrid model that uses conventional MOS transistors to implement an inverter and master latch that uses MTJs for storing data in a power-down state. The rest of the paper has been organized as follows. The basic VgSOT-based read-and-write mechanism has been discussed in Section II. NVFF implementation using VgSOT, SOT, and STT has been done in Section III. Model parameters and simulation results have been deliberated upon in Section IV. Section V presents the comparative analysis of different NVFFs based on various performance parameters. The vgSOT-based NVFF implementation layout has been shown in Section VI. Section VII concludes the research work on VgSOT-MTJ based NVFF performance compared to SOT and STT-MTJ based FFs.

II. VGSOT-MTJS READ AND WRITE MECHANISM

An MTJ structure consists of a dielectric layer sandwiched between two magnetic layers, as shown in Fig. 1. These two magnetic layers have their own spin orientations, one having fixed polarization and the other being free. Current can be injected to change the free layer's (FL) orientation. An MTJ can be in an anti-parallel (AP) or a parallel (P) state, depending on the spin direction. Each MTJ state corresponds to a logical resistance corresponding to logical "0" for P and logical "1" for the AP state.

VgSOT-MTJ has three terminals with separate write and read paths, contrary to a Spin transfer torque-MTJ, which consists of only two terminals, and read/write current directly passes through MTJ. VgSOT utilizes a VCMA [22] effect to guide SOT. The energy barrier between the two states is reduced when the bias voltage over MTJ is positive. Thus, it helps to reduce the critical ISOT current.

Fig. 2 shows the three terminal VgSOT circuit [23]. T3,

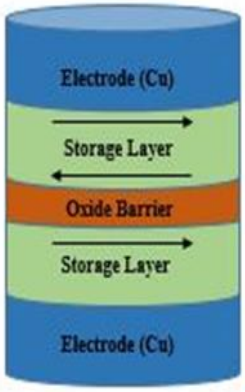

Fig. 1. MTJ Basic Structure [11]

T2, and T1 are real pins, and spin torque can be generated between T2 and T3. The Tmz pin represents the magnetization state of MTJ in the z-direction. It mainly comprises two ferromagnetic layers stacked on top of an antiferromagnetic layer (AFM). Fig. 3 shows a simple VgSOT-MTJ based bit cell. When the access transistors are ON by keeping word lines WL2 and WL1 high, a current flows via the channel layer and access transistors.

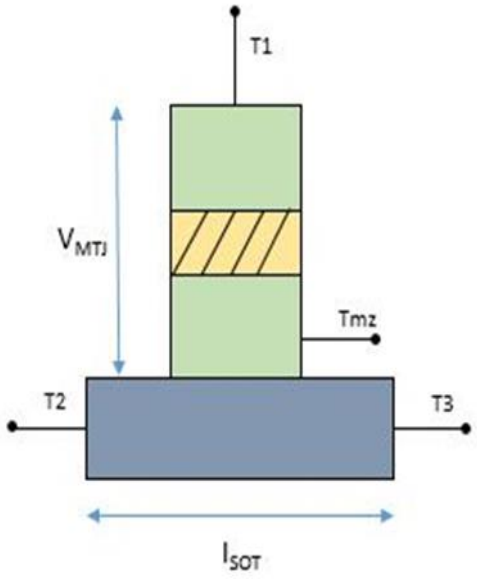

Fig. 2. Three terminal VgSOT symbol [23]

If the applied current is sufficiently more significant, VgSOT undergoes a state of change to a parallel or anti-parallel state upon application of voltages on SL and BL. For reading back the stored information from MTJ, RBL (read bit line) is raised high, and RWL (read word line) is kept low. As both write and read current paths are different, more increased endurance and lesser read disturbances are observed.

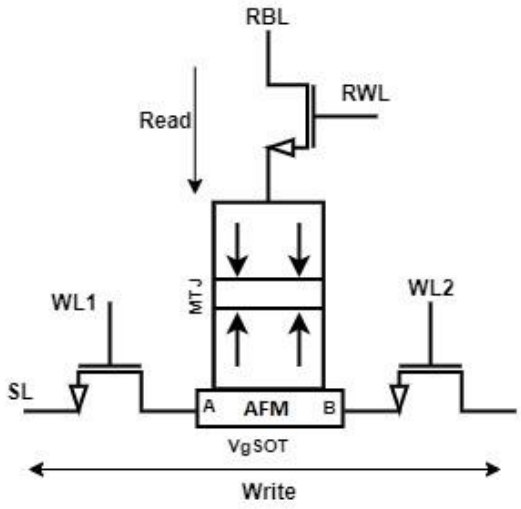

Fig. 3. VgSOT-MTJ Bit Cell

III. IMPLEMENTATION OF NVFF CIRCUIT

A. VgSOT MTJ based NVFF Circuit

NVFFs implemented using two MTJs to store the output Q value of a slave latch generally require six transistors to control the operation. The difference in two MTJ resistances causes the inverter pair's regenerative feedback, thus producing 0 or Vdd in a restore operation. The problem with these circuits is that two write currents are needed separately for each of the two MTJs, thus increasing the energy consumption and area overhead. Generally, two current pulses have been required to write data into two MTJs. In this paper, the write current used for one MTJ has also been re-utilized for another MTJ. Thus, to store the data onto MTJs, a single current pulse is utilized, eventually decreasing the size of the circuit. Connecting two MTJs back-to-back on the same path in the opposite direction has allowed for data storage on both MTJs in a single current pulse. Thus, these MTJs will always be set in opposite orientation states by the same write current. VgSOT-MTJ based NVFF circuit is shown in Fig. 4. A single minimum-size transistor M14 acts as a switch to enable the write operation. With channel-layer resistance being low, no significant voltage drop is seen across the channel layers. This combination reduces the write energy by 50% in a single write attempt. Thus, a single write pulse considerably reduces the energy and area overhead.

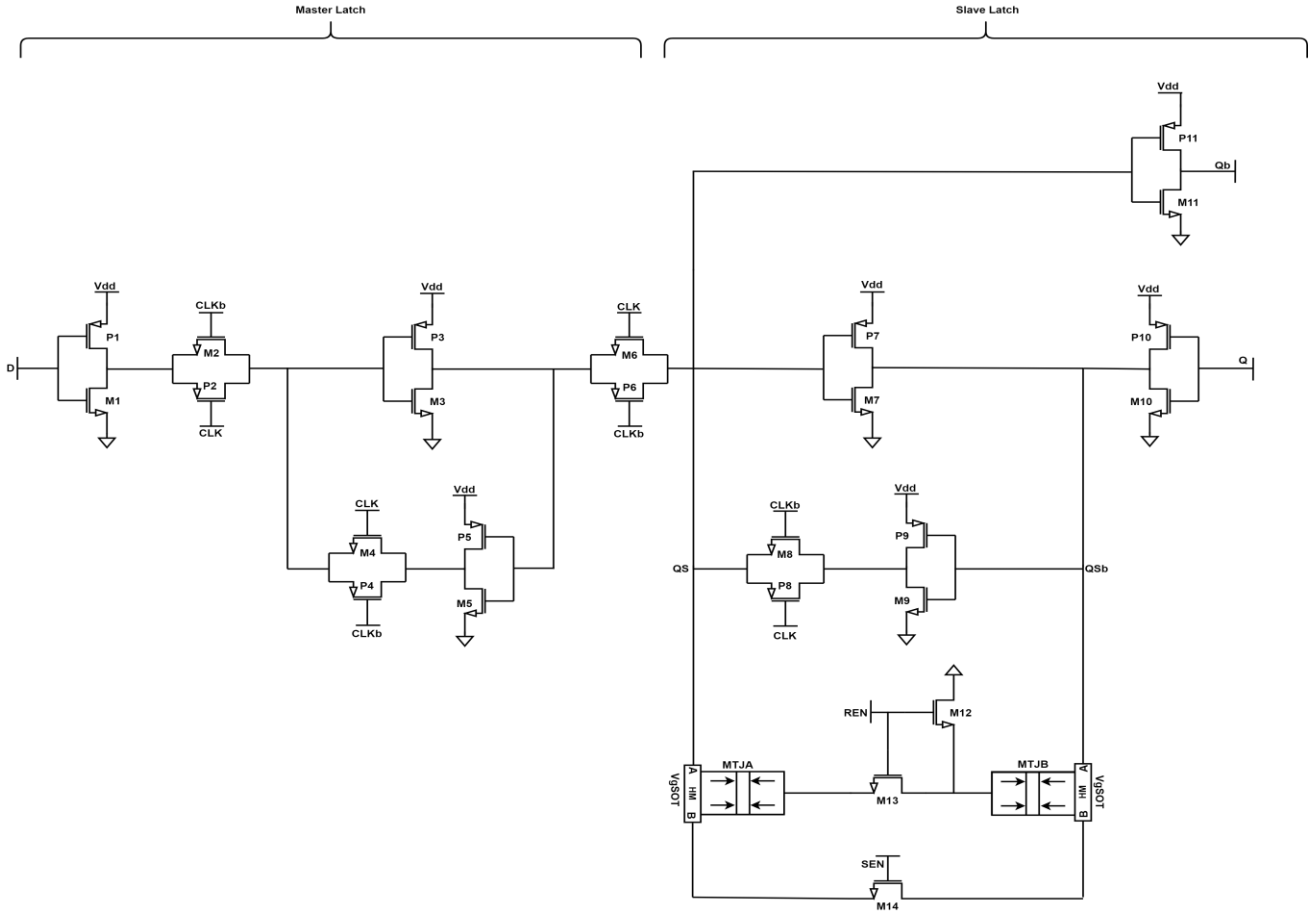

Fig. 4. VgSOT-MTJ based NVFF circuit

The slave latch inverter-pair has been utilized to restore the data. M12 and M13 act as a switch to control the direction of the current path. Once the REN (Restoring Enable) signal is high, the current path changes its direction from the AFM layer of MTJs towards the free layer (FL) via M13. Once power is turned back ON after gating, based on the two VgSOT MTJ resistances, regenerative feedback produces outputs in the inverter pair. Thus, Qs and Qsb nodes become 0 or VDD.

The proposed non-volatile flip-flop works like a conventional D flip in normal mode. Q follows input D before the power shutdown and after the power-up stages. The store operation is carried out before the power shutdown happens to store the data onto MTJs, and similarly, data is restored back on Q once power is ON. Initially, the Q output is initialized to 1 before the shutdown happens. Once SEN is turned ON, current flows from MTJA to MTJB via M14. As the current flows to terminal B via the A path, MTJA is moved to the AP state, and MTJB shifts to the P state simultaneously. As the current flows to terminal B via the A path, MTJA is moved to the AP state, and MTJB shifts to the P state simultaneously.

B. SOT-MTJ based NVFF Circuit

Similar to VgSOT-based NVFF, SOT-based current re-use NVFF has been simulated, and energy consumption and delay comparison has been shown w.r.t VgSOT in section 5. The SOT-based current re-use NVFF schematic is shown in Fig. 5.

C. STT-MTJ based NVFF Circuit

Like VgSOT and SOT-based implementations in previous sub-sections, STT-based NVFF has also been simulated for energy and delay performance comparison. For STT based circuit, terminal T1 has been connected to switch transistors M13 and Qs/Qsb nodes. The STT-based current re-use NVFF schematic is shown in Fig. 6.

IV. MODEL PARAMETERS AND SIMULATION RESULTS

The simulation of VgSOT-based NVFF has been carried out using CADENCE VIRTUOSO software on a 45nm technology node at 1.2 V VDD. Verilog model of VgSOT MRAM [23], STT MRAM [24], and SOT MRAM [25] have been used. Critical device parameters being used for model simulation in the case of VgSOT, SOT, and STT have been shared in Table I.

Table I. Critical Device Parameters

Parameters	**VgSOT**[23]	**SOT**[25]	**STT**[24]
MTJ Surface Area(nm*nm)	50*50	40*40	40*40
Oxide barrier Thickness (nm)	1.4	0.85	0.85
Free Layer Thickness (nm)	1.1	0.7	1.3
TMR	100%	120%	200%
Write Voltage (V)	1.2	1.2	1.2
CMOS Technology (nm)	45	45	45

A. VgSOT-MTJ based NVFF Simulation

Fig. 7 shows the waveform of the proposed VgSOT-MTJ based NVFF. Node voltage changes on D, Q, REN, SEN, CLK, and VDD can be seen on the waveform. There are four modes of operation in which flip-flop works. Between 0-7 ns, “Normal mode” is activated. Between 7 to 32 ns, the flip-flop enters into “Storing mode”. During storing mode, signal SEN is active, and Q follows input D. Post-storing mode, NVFF enters into “Power-down mode”, and Q switches to a low value. Once the power is back, Q gets restored back at ~62ns.

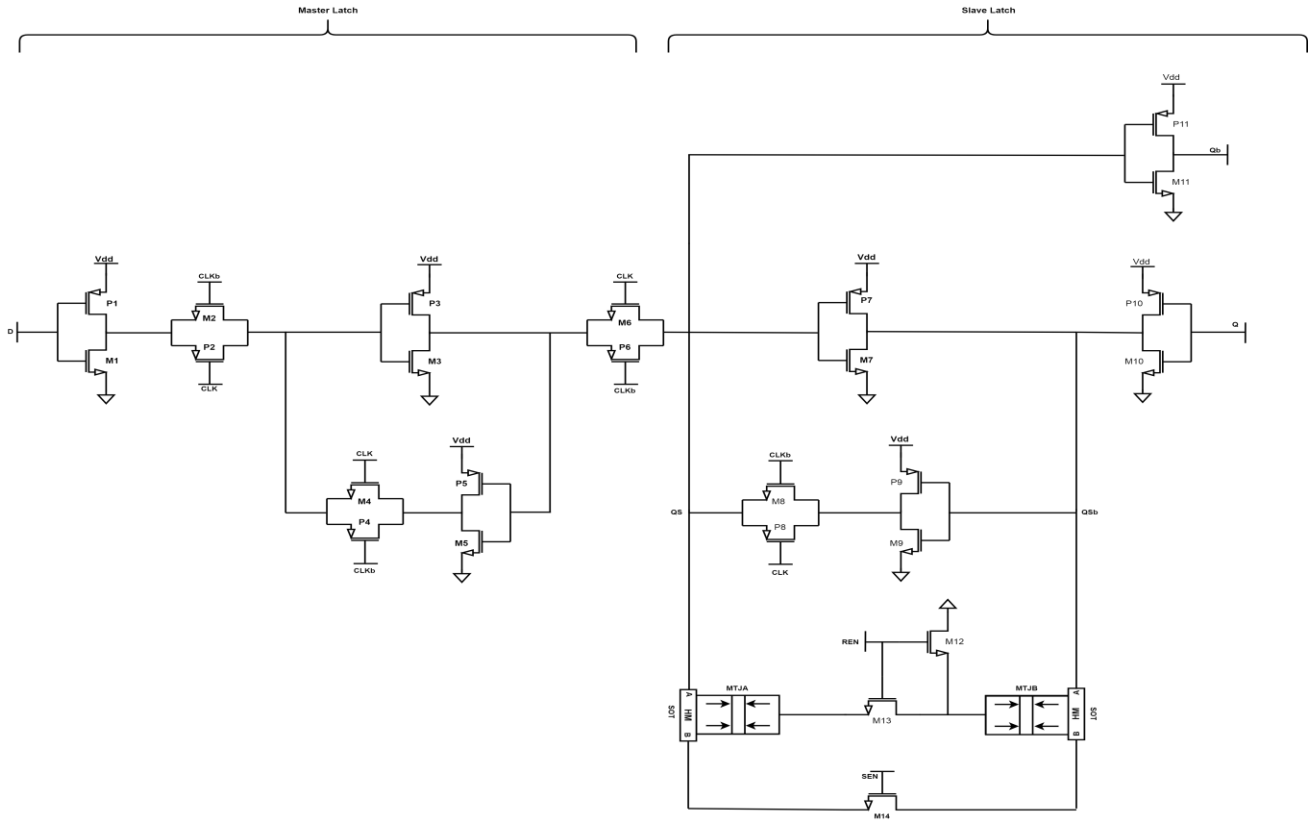

Fig. 5. SOT-MTJ based NVFF circuit

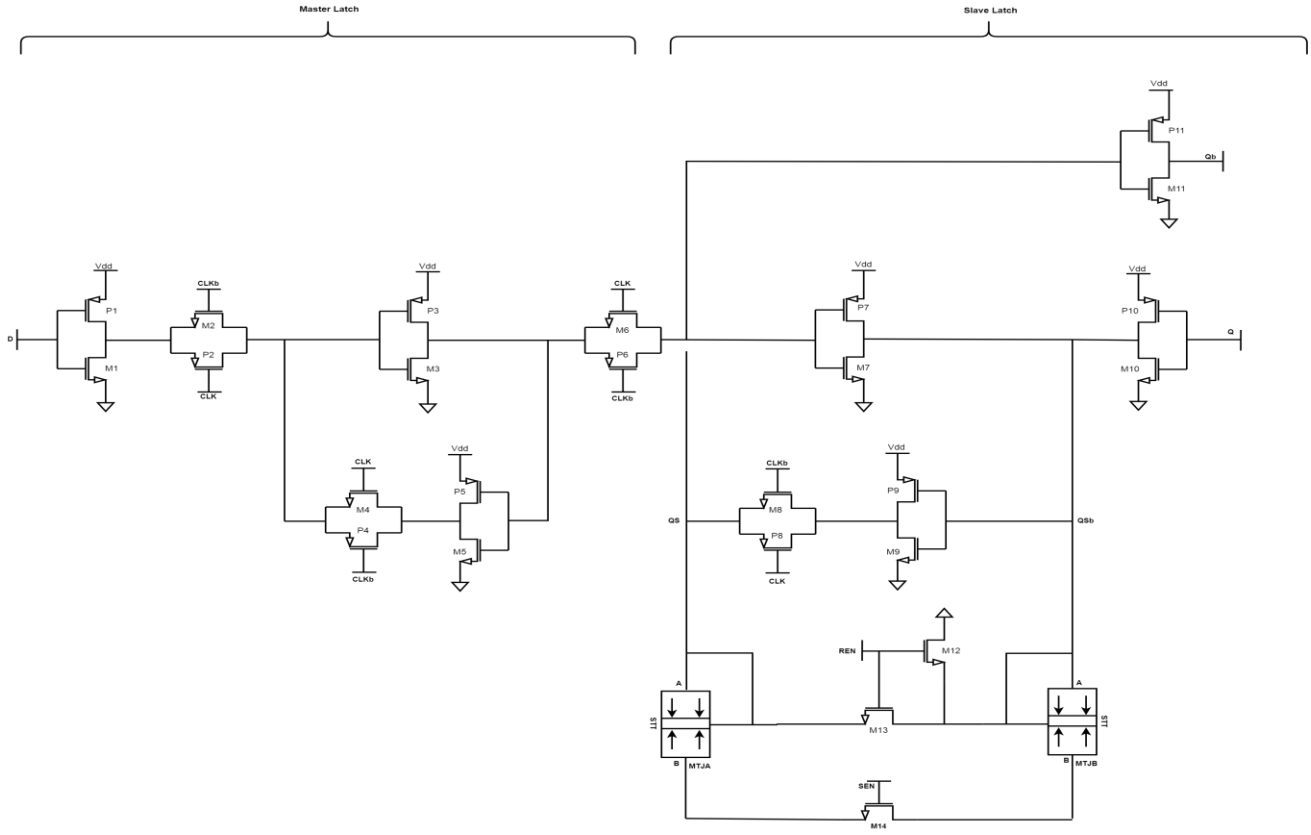

Fig. 6. STT-MTJ based NVFF circuit

After 62ns, once REN is active, NVFF enters the "Restoring mode" of operation. During this period, inverter pair regenerative feedback starts, and the values of MTJs are restored. As seen from the waveform, the output is restored during the 62ns window. Hence, it confirms the functional operation of a D-FF. M1 and m2 correspond to MTJ A and MTJ B spin directions on the z-axis, respectively. -1 and 1 denote parallel and anti-parallel states of MTJs, respectively. After restoring mode, NVFF again enters into the normal mode of operation. Regenerative feedback of MTJ produces Vdd or 0 depending on the resistance difference between two MTJs.

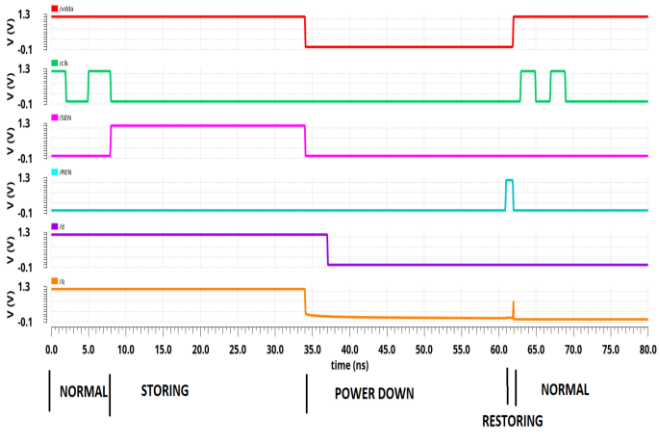

Fig. 7. VgSOT-MTJ Based NVFF Simulation

B. SOT-MTJ based NVFF Simulation

Fig. 8 shows the simulation result of SOT-MTJ based NVFF. Similar to the VGSOT-based simulation result, it can be seen that the FF operates in four modes. The values on MTJ get restored during the 62ns REN enable window. A performance comparison between VgSOT and STT-based NVFF has been done in section 5 below.

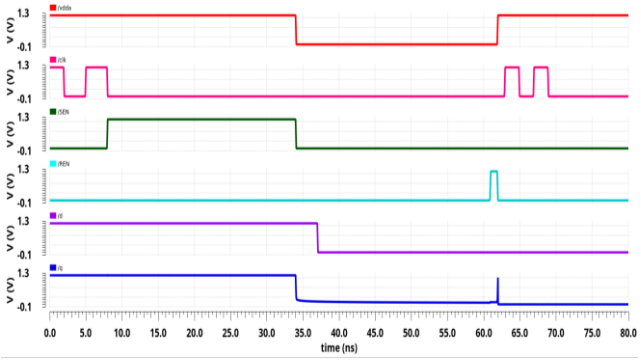

Fig. 8. SOT-MTJ Based NVFF Simulation

C. STT-MTJ based NVFF Simulation

Fig. 9 shows the STT-MTJ based NVFF waveform. Similar to VgSOT and SOT-MTJ, STT-MTJ based FF behaves similarly. However, we see a difference in the storing energy consumption and delay parameters between these three MTJ based FFs. The performance evaluation has been done in section 5.

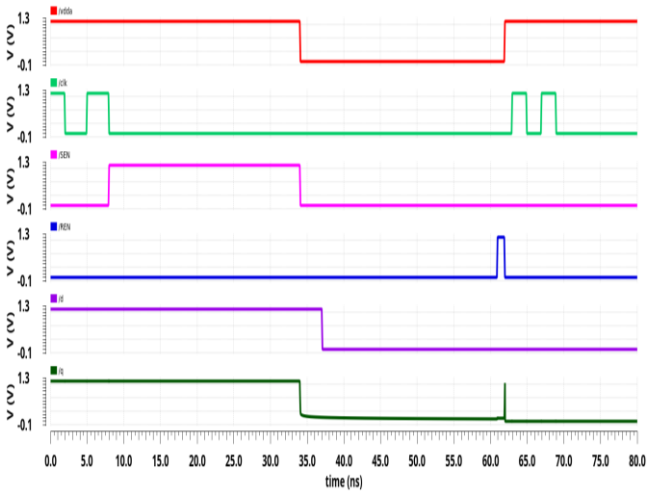

Fig. 9. STT-MTJ Based NVFF Simulation

V. PERFORMANCE EVALUATION

Energy consumption and delay performance parameters have been captured for storing and restoring modes of operations in three NVFFs. Fig. 10 and Table II describe the delay comparison between VgSOT-MTJ, SOT-MTJ and STT-MTJ NVFFs during storing and restoring modes. From Table II and Fig. 10, it can be inferred that VgSOT-MTJ based NVFFs are much faster than STT and SOT-MTJ based NVFFs. During storing mode of operation, VgSOT-MTJ based NVFF performs 40% better than SOT-MTJ NVFF and 58% better than STT-MTJ based NVFFs. During restoring mode, VgSOT-MTJ based NVFF performs 83% better than SOT-MTJ NVFF and 88% better than STT-MTJ based NVFFs.

Table II. NVFF Delay Comparison

Technology	Storing Operation (ns)	Restoring Operation (ps)
VgSOT-MTJ NVFF	3.01	2
SOT-MTJ NVFF	5	12
STT-MTJ NVFF	7	17.6

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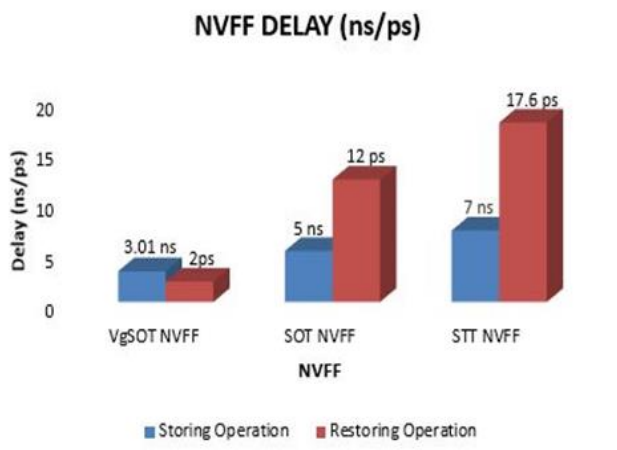

Fig. 10. Different NVFF circuit delay Comparison

Fig. 11 and Table III describe the energy consumption comparison between VgSOT-MTJ, SOT-MTJ, and STT-MTJ NVFFs during storing and restoring modes.

Table III. NVFF Delay Comparison

Technology	Storing Operation (ns)	Restoring Operation (ps)
VgSOT-MTJ NVFF	0.1	0.1
SOT-MTJ NVFF	0.66	0.35
STT-MTJ NVFF	1.2	0.56

From Table III and Fig. 11, it can be deduced that NVFF employing VgSOT-MTJ consumes less energy than STT and SOT-MTJ based NVFF. During storing mode of operation, VgSOT-MTJ based NVFF consumes 84% less energy than SOT-MTJ NVFF and 90 % less energy than STT-MTJ based NVFFs. During restoring mode, VgSOT-MTJ based NVFF consumes 70% and 80% less energy than SOT-MTJ NVFF and STT-MTJ, respectively.

Different technologies based on switching delay and energy consumption metrics have been presented in Table IV. From the results in Table IV, it can be deduced that the NVFFs implemented using VgSOT-MTJ perform an average of 40% and 80% better in terms of switching delay during storing and restoring mode, respectively. From an energy point of view, VgSOT-MTJ NVFFs perform an average of 85% and 70% better than others during storing and restoring modes, respectively.

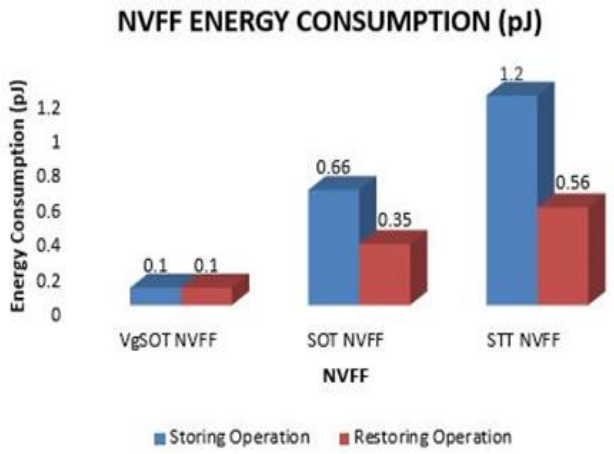

Fig. 11. Different NVFF circuit Energy Comparison

Fig. 12 and Fig. 13 show the delay variation between state-of-the-art NVFFs during storing and restoring modes.

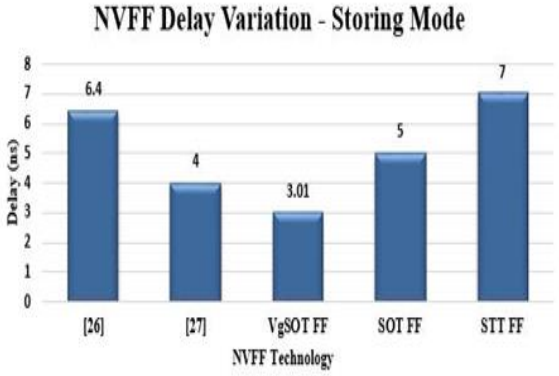

Fig. 12. Storing Mode delay variation for different NVFF technologies

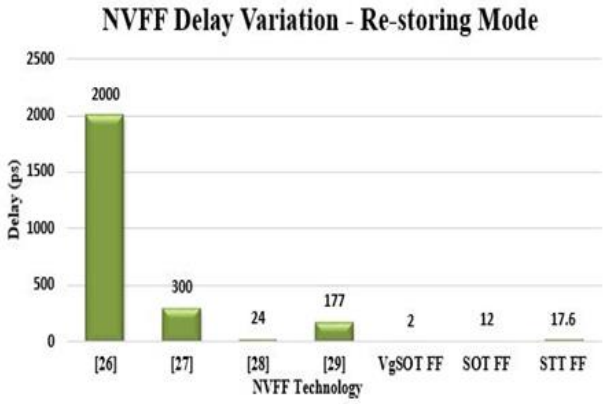

Fig. 13. Restoring Mode delay variation for Different NVFF technologies

Fig. 14 and Fig. 15 show the variation in energy consumption between state-of-the-art NVFFs during storing and restoring modes, respectively.

Table IV. Comparison with other NVFFs (normalized values for D-FF)

Parameter		[26]	[27]	[28]	[29]	VgSOT FF	SOT FF	STT FF
Tech Node	(nm)	65	45	10	45	45	45	45
Delay	Storing Mode	6.4 ns	4 ns	-	-	3.01 ns	5 ns	7 ns
	Restoring Mode	2 ns	0.3 ns	24 ps	177 ps	2 ps	12 ps	17.6 ps
Energy	Storing Mode (pJ)	0.5	0.2	-	-	0.1	0.66	1.2
	Restoring Mode (pJ)	0.2	0.006	0.23	2.36	0.1	0.35	0.56

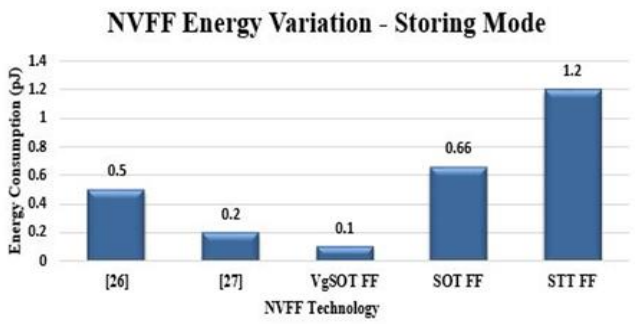

Fig. 14. Storing Mode Energy variation for different NVFF technologies

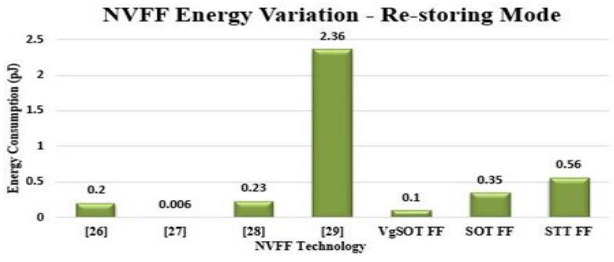

Fig. 15. Restoring Mode Energy variation for different NVFF technologies

Table V describes the comparative PVT-based temperature analysis for storing and re-storing modes delay for VgSOT, SOT, and STT, respectively. Fig. 16, 17, and 18 show the delay variation in two modes for the entire range of operating temperatures. Table V and Fig. 16-18 show minimum delay variation for three types of NVFF over the entire operating temperature range.

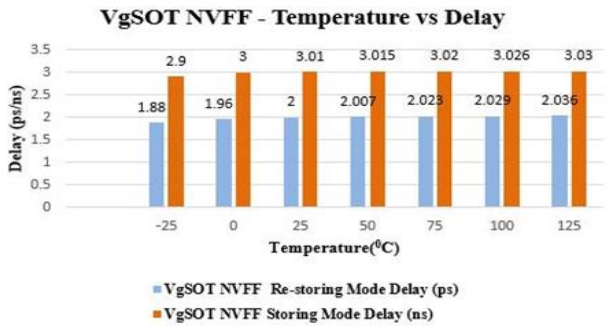

Fig. 16. VgSOT NVFF delay variation with Temperature

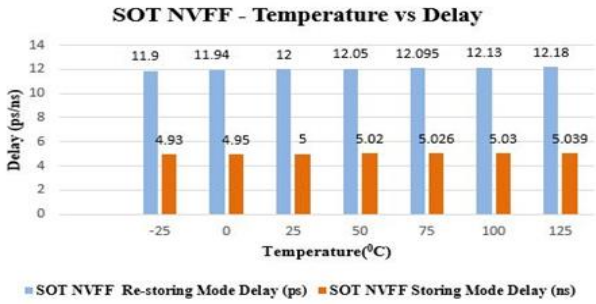

Fig. 17. SOT NVFF delay variation with Temperature

Table V. Comparative Temperature Analysis on Delay

Temperature(°C)	VgSOT FF Re-storing Mode Delay (ps)	VgSOT FF Storing Mode Delay (ns)	SOT FF Re-storing Mode Delay (ps)	SOT FF Storing Mode Delay (ns)	STT FF Re-storing Mode Delay (ps)	STT FF Storing Mode Delay (ns)
-25	1.88	2.9	11.9	4.93	17.21	6.904
0	1.96	3	11.94	4.95	17.57	6.912
25	2	3.01	12	5	17.6	7
50	2.007	3.015	12.05	5.02	17.684	7.04
75	2.023	3.02	12.095	5.026	17.746	7.066
100	2.029	3.026	12.13	5.03	17.865	7.09
125	2.036	3.03	12.18	5.039	17.99	7.105

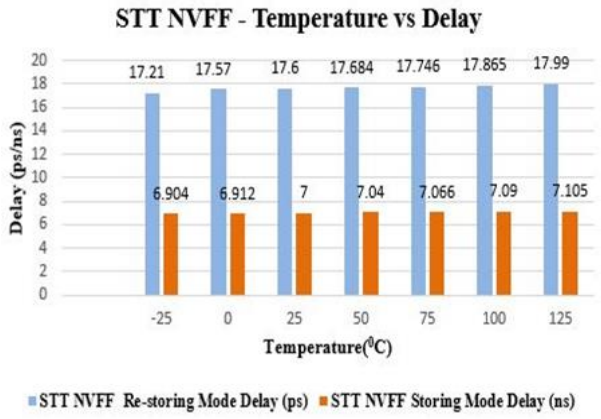

Fig. 18. STT NVFF delay variation with Temperature

Table VI shows the power consumption variation with temperature for NVFFs. It can be concluded that VgSOT NVFF performs better in terms of power consumption over already implemented NVMSFF as well as over SOT and STT-based implementations, as shown in Table VI.

Fig. 19 shows the power consumption variation for different NVFFs across the temperature range. Similar to delay, minimal variation is seen in power consumption across temperature ranges, making it suitable for various applications in the Silicon industry. At room temperature, VgSOT-based NVFF performs 57% better in terms of total power consumption over already implemented NVMSFF, as shown in Table VI.

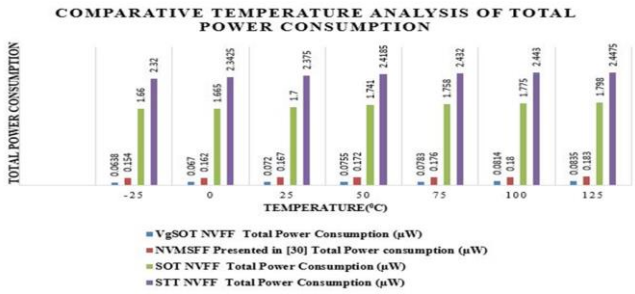

Fig. 19 Comparative temperature analysis of total power consumption

VI. VgSOT-MTJ NVFF LAYOUT

The proposed VgSOT-MTJ based NVFF layout has been presented in Fig. 20. The layout is made in Virtuoso layout suite XL. The VgSOT-based NVFF design consumes considerably less area than other state-of-the-art NVFF designs because the same current pulse is utilized to write two MTJs simultaneously. The area overhead in the VgSOT NVFF circuit includes 25 MOS Transistors and 2 MTJs.

Table VI. Total Power Consumption Variation with Temperature

Temperature(ºC)	VgSOT NVFF Total Power Consumption (µW)	Total Power consumption for NVMSFF presented in [30] (µW)	SOT NVFF Total Power Consumption (µW)	STT NVFF Total Power Consumption (µW)
-25	0.0638	0.154	1.66	2.32
0	0.067	0.162	1.665	2.3425
25	0.072	0.167	1.7	2.375
50	0.0755	0.172	1.741	2.4185
75	0.0783	0.176	1.758	2.432
100	0.0814	0.18	1.775	2.443
125	0.0835	0.183	1.798	2.4475

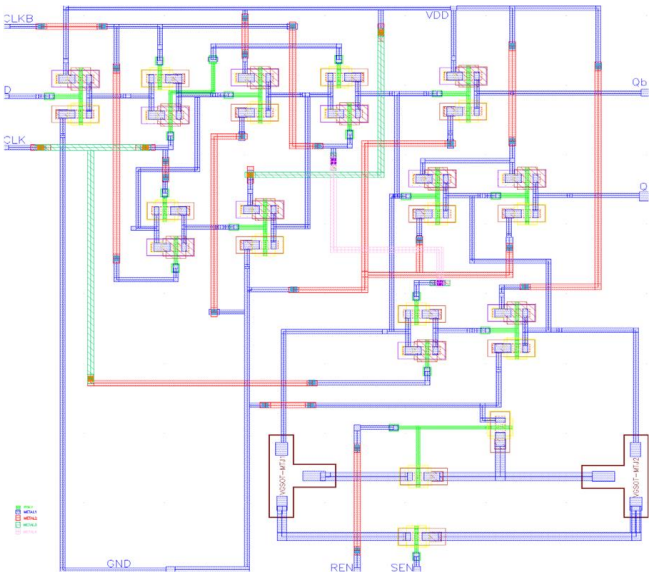

Fig. 20 VgSOT-MTJ based NVFF Layout

VII. CONCLUSION AND FUTURE SCOPE

In this paper, an energy-efficient VgSOT-MTJ non-volatile flip flop has been presented. As the same current is used to write both MTJs simultaneously in the NVFF circuit, the write current needed for data store operation has been reduced by 50%. Simulation results show that for the switching delay, VgSOT-MTJ based NVFF performs 40% and 58% better than SOT-MTJ NVFF and STT-MTJ based NVFFs, respectively, during storing mode and 83% and 88% better than SOT-MTJ and STT-MTJ based NVFFs during restoring mode. During the storing mode of operation in terms of energy consumption, VgSOT-MTJ based NVFF consumes 84% less energy than SOT-MTJ NVFF and 90 % less energy than STT-MTJ based NVFFs. During restoring mode, VgSOT-MTJ based NVFF consumes 70% and 80% less energy than SOT-MTJ NVFF and STT-MTJ, respectively. The challenge faced during this research involves the analysis of literature to find the right dataset of NVFFs for a better understanding of energy, power, and delay variation with technology nodes, operating voltage, and temperature.

Thus, non-volatile flip flops implemented with VgSOT technology can be used in fine-grained power gating applications. This technology is very prominent and allows any logic circuit to operate with high speed and low power dissipation as compared to SRAM FFs. Along with power saving and high speed, VgSOT-based NVFF also provides non-volatility and data security. Thus, these FFs can be used in FPGA computing and a low-energy memory cell in various SOC applications such as aviation and space, where data security is of prime importance.

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