A 915 MHz Closed-Loop Self-Regulated RF Energy Harvesting System for Batteryless Devices

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Abstract— Batteryless devices are essential for hard-to-reach applications such as implantable biomedical devices. Powering such devices is a difficult task, and energy harvesting from the environment is mandatory. Among the power sources available in urban areas, RF signals stand out. However, the RF power at the receiving antenna is not constant, and energy-harvesting circuits should provide a stable DC output voltage. In this paper, we present an RF energy harvesting-based power management system that provides a stable 0.4-V DC supply voltage to power low-voltage systems. A closed-loop impedance matching tuning system is used to automatically regulate the system DC output voltage by tuning the input impedance matching network. The proposed circuit is implemented at schematic level in a 65-nm standard CMOS process. The entire system power efficiency (PCE) is 48.28% at the input power level of −14.92 dBm. The proposed solution is demonstrated for powering low-voltage devices with a regulated output voltage of 0.4 V and 16 µW resistive load.

Index Terms— Energy-Harvesting; RF-DC converters; Rectifiers; Impedance matching.

I. INTRODUCTION

Powering electronic devices located in extreme environments, such as space, autonomous driving, biomedical implantable devices, and other hard-to-reach applications, is a difficult task [1]. Such applications typically rely on rechargeable batteries or compact capacitor-based devices with energy storage capability. In addition, there are electronic devices that must be powered directly without energy storage.

The energy used to operate these electronic devices can be harvested from energy sources available in the environment, such as radio waves, light, vibration, kinetic, piezoelectric, and thermal energy. This technique is called energy harvesting (EH). It aims to reduce and, in some cases, completely replace the use of batteries with harvested energy [2], [3], [4], [5]. This ability to remove the necessity of batteries in low-power applications makes energy harvesting a very attractive technique.

Among the energy sources available today, radio frequency energy harvesting (RF-EH) has emerged as a promising alternative for the production of batteryless low-power portable devices [6] [4]. This technology is ubiquitous and capable of reaching environments where other sources are not available, such as human body implantable electronics.

RF-based energy harvesting can capture energy from a wide range of frequencies from the RF spectrum, especially in urban environments due to the massive use of wireless communication [2].

In general, an RF-EH system is composed of an antenna, an input matching network (IMN), a rectifier, and the load, as shown in Fig. 1. The RF input signal is captured by the antenna, rectified, and is available at the output as a DC voltage. The IMN block provides matching between the impedance of the antenna and the rectifier to maximize power transfer.

This paper presents a brief literature review of RF-EH systems for low-voltage and low-power applications. Additionally, it proposes an RF-EH system integrated in a typical 65-nm CMOS process that captures a 915-MHz RF signal and converts it to a 0.4-V DC voltage to supply low-power, batteryless devices. A closed-loop control approach using an adaptive impedance matching network is used to regulate the output voltage. It is simple to implement and requires maximum power conversion efficiency (PCE) only at the signal maximum power transfer (MPT) bias point.

The remaining of this paper is organized as follows: Section II explains the background of state-of-the-art RF-EH systems; Section III describes the implementation of an RF rectifier with adaptive-impedance matching; Section IV presents a proposed RF-EH closed-loop voltage regulation system; Section V discusses simulation results; and Section VI provides concluding remarks.

II. LITERATURE REVIEW

In RF-based EH systems, the received energy may or may not be sufficient to power an electronic device [6]. If the energy collected and converted by the RF-EH is less than the value required by the device, it must be accumulated to the minimum value to allow the device to operate for some time. Recently, however, the trend has been toward batteryless devices, which are being introduced as a more sustainable concept based on reducing the use of batteries in electronic devices [7].

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A typical front-end block for RF energy harvesting for a batteryless application is depicted in Fig. 1.

The first stage of the RF-EH system performs the collection of the RF signal by means of a receiving antenna. The electrical model of this antenna is represented by an AC source with amplitude $V_{AMP}$, set to the frequency of interest and characteristic impedance $Z_0$.

The main block of the front-end circuit is the rectifier. Rectifiers can be implemented using diodes for AC-DC conversion. However, when dealing with RF, the variable nature and propagation losses of these devices at high frequency must be considered [8].

If the input impedance of the rectifier $Z_{RECT}$ is different from the impedance $Z_0$ of the antenna, a portion of the power that will be transmitted is reflected, reducing the efficiency of the RF-EH circuit. Therefore, an impedance input matching network (IMN) is necessary at the input of the front-end circuit to ensure maximum transfer of signal power to the final load.

According to [8], there is a trade-off between power conversion efficiency (PCE) and the sensitivity of the energy harvesting device, which turns more challenging the design of a rectifier for RF-EH.

To understand the rectification principle, some fundamental approaches are presented. In addition, the topologies of rectifiers based on CMOS transistors are also presented, as well as a literature review about impedance matching techniques adopted in RF-EH systems.

### A. Rectifier

Rectifiers can be classified in three basic topologies: half-wave, full-wave bridge, and charge pump.

The half-wave rectifier is the simplest configuration, having only one diode in its circuit. Its working principle basically consists of two phases. Figure 2a depicts its schematic. In the first phase, when the input current flows in the positive direction from the source, the diode is directly biased. This means that it allows current to flow through it and reach the connected load ($R_L$). In the second phase, when the input current flows in the negative direction, the diode is reversed-biased, preventing current from flowing back to the source.

The main characteristic of this rectifier topology is its simplicity. However, it is unsuitable for general applications. Since it allows current to pass only in one of the half-periods, the output voltage is discontinuous, and the maximum power of the AC voltage at the output is half of the input power.

In order to be able to transmit all the input power of the AC voltage and also transform the signal into continuous, topologies with multiple diodes must be used. The topology that meets this solution is called a bridge full-wave rectifier, as shown in Fig. 2b. In this topology, the signal at the output of the rectifier is continuous. When the input sine wave is positive, diodes $D_3$ and $D_2$ conduct, while $D_1$ and $D_4$ are blocked. When the wave is negative cycle, diodes $D_1$ and $D_4$ are conducting, while $D_3$ and $D_2$ are blocked, so the peak amplitude of the output voltage follows the peak amplitude of the input sine wave. However, a disadvantage of this topology is the higher voltage drop across the two conducting diodes in the current path, which causes high power losses.

A third rectifier solution is the so-called doubler or charge pump. In this topology, shown in Fig. 2c, the input signal is transmitted to the output in the same way as in the full-wave rectification, but with capacitors integrated in the circuit to store the voltage while the diodes are driven, and finally transmit twice the value of the input peak voltage to the output. This topology has better efficiency than the half-wave and full-wave topologies.

There are other configurations based on the three basic configurations presented earlier. We highlight the topologies shown in Fig. 3, which are suitable for RF. They are called Dickson-Greinacher, Greinacher, Dickson, and Full-Wave Dickson Variation. The differences between them are related to the levels of derivation to reduce parasitic effects and the resulting power conversion efficiency. In [9], a comparison is made between these topologies operating at 2.4 GHz, taking into account features that limit efficiency.

The use of conventional silicon diodes becomes inefficient for low input voltage ranges due to its threshold voltage ($V_T$) -- typically 0.7 V --, which results in a considerable conduction loss. An alternative to replace the silicon diode is the Schottky diode, which works well at high frequencies and has a lower $V_T$ (around 0.25 V or lower). However, the disadvantage of this device is the large number of steps required for its production. For large-scale productions, the Schottky diode becomes unsuitable due to the requirement of steps not normally available in traditional manufacturing processes, as well as the associated high cost.

Thus, another option to replace diodes in rectifiers is the implementation with CMOS (Complementary metal-oxide-semiconductor) transistors, which have a lower $V_T$ value (this value depends on the process adopted) and are efficient for low input powers. In addition, CMOS transistors also have a lower cost when produced on a large scale.

Figure 4 shows the full-wave rectifier in which the diodes are replaced by CMOS transistors in the well-known diode connection configuration. This would be a suitable option for RF-EH, but it is not very efficient. According to [8], this topology has a high turn-off voltage due to the transistors threshold voltage and also obtains a low PCE value for low input powers due to the forward voltage drop across the diodes. However, this topology is still advantageous for achieving high PCE for high input power.
A good alternative for low input power applications is a cross-coupled differential-drive (CCDD) configuration proposed by [10], shown in Fig. 5. According to [8], it achieves the maximum PCE at a low input power level. This topology is based on a differential-drive active gate bias mechanism, allowing a low on resistance and a low leakage reverse current into the diode-connected MOS transistors [6].

Figure 5 shows the two stages of operation of a CCDD. When the signal is in the positive semi-cycle, transistors $M_{P1}$ and $M_{N2}$ are in conduction, charging the capacitor $C_{Fly}$ connected to the negative input. The other transistors are reversely biased, reducing the leakage current. In the second stage, when the signal is in the negative half cycle, transistors $M_{P2}$ and $M_{N2}$ are conducting, while the others are reversely biased, discharging $C_{Fly}$ from the negative input to the load, and charging $C_{Fly}$ from the positive input. The threshold voltage $V_T$ of the transistors is still reduced when they are conducting due to the differential input.

Several works on literature adopt the CCDD configuration for RF-EH. In [3] the CCDD configuration is used without any modification in the design of an RF-EH unit that manages the power for operating over a wide input power range, from -24 to +15 dBm. The system has been designed considering the 180 nm CMOS process and the RF frequency of 403.5 MHz.

The work in [11] introduces a modification in the CCDD circuit via an adaptive body bias technique to decrease the $V_T$ of the transistor when PMOS is triggered. In addition, the technique aims to minimize the current flow in the reverse bias condition when PMOS is off by increasing its $V_T$. The design used the 180 nm CMOS process, 953 MHz RF frequency, and achieved a PCE of 78.2% for a sensitivity of -27.5 dBm and 100 kΩ load.

In [12], the CCDD circuit is also used without modification. A methodology based on output voltage maximization of transistor sizing in CCDD configuration for ultra-low voltage operation is demonstrated, as well as a comparison between one, three, and five rectifier stages with improved PCE performance and sensitivity. In this study, it is seen that the adoption of one rectifier stage is sufficient for conversion at ultra-low voltage operation with low input power. The technology used was 180-nm CMOS for an RF frequency of 915 MHz.

In the work described by [13], the CCDD rectifier is used in two input capacitor coupling configurations: shared-capacitor coupling (SCC) and individual-capacitor coupling (ICC). The CCDD rectifier demonstrates a wide dynamic
range (DR) and employs the self-biasing technique to reduce $V_T$. In addition, diode-connected MOSFETs are used to control the leakage reverse current and improve the direct current. The SCC-CCDD and ICC-CCDD rectifiers are fabricated in 130-nm CMOS and exhibit a DR of 13 and 14.5 dB, respectively, for a PCE greater than 40%. In an alternative analysis, the SCC-CCDD achieved a maximum PCE of 83.7% with a sensitivity of -19.2 dBm at 1 V, while the ICC-CCDD achieved a maximum PCE of 80.3% with a sensitivity of -18.7 dBm.

Other works show modified CCDD configurations to increase the power dynamic range (PDR), i.e., to obtain an optimal PCE even with varying sensitivity. In [14], a proposal for an advanced topology amalgamation technique to increase the power dynamic range (PDR) and significantly improve the PCE is presented. This work addresses adaptive DC counter deactivation in the last phase of the rectifier by means of a self-biasing configuration. The design was developed using 65-nm CMOS technology for two different frequencies. The first frequency is 900 MHz, operating at an ultra-low voltage of about 0.2 V, presenting a PDR of 21 dB. The second frequency is 1.8 GHz, operating at about 0.4 V, with a PDR of 15 dB. The peak PCE values are 79.77% and 51.3%, respectively, under a 100 kΩ load.

A proposal for a rectifier to increase the PDR by using a dual path with adaptive control circuits is presented by [15]. In this work, two rectifiers are designed: one modified CCDD and one fully NMOS. The circuit is implemented in a 180 nm CMOS process, considering an RF frequency of 2.45 GHz, achieving a sensitivity of -20.7 dBm for an output voltage of 1 V. Furthermore, the PCE range above 20% of the proposed RF-EH is kept between -22 dBm and 5 dBm, with a total range of 27 dB. Two peak PCEs, 57% and 62%, are observed for input powers of -15 dBm and 1.6 dBm, respectively.

Different implementations of the CCDD rectifiers for RF-EH are summarized in Tab. I. The choice of the basic topology and the possibility to modify its configuration depends on the specifications of each particular application. Furthermore, a trend towards designs operating at a low voltage of 0.4 V is observed in Table I and Figure 6, which compares the output voltage and the sensitivity of the selected papers. However, a low peak PCE value is still observed. There is also no approach using frequencies of 5.8 GHz or higher with fully CMOS topologies.

B. Impedance Matching Network

Having established that the rectifier block is capable of converting the RF signal to a DC voltage, it is clear that power conversion efficiency and sensitivity, which are parameters related to input power, are the most important performance characteristics to be analyzed and achieved in an RF-EH design. However, another challenge in this design is to ensure the maximum transfer of the RF power captured by the receiving antenna to the load.

A transmitting or receiving antenna has a characteristic impedance ($Z_0$), which is determined by its physical elements, size, shape, and design characteristics. In general, the antenna operates at resonance frequency and $Z_0$ usually is a real impedance. On the other hand, the device or system connected to the antenna, such as the rectifier in our case, also has its own characteristic impedance, which is measured after the entire circuit design is complete. However, to maximize power transfer between the antenna and the device, it is desirable that the antenna impedance matches the device impedance. If there is an impedance mismatch between the antenna and the device, some of the signal power will be reflected back to the antenna. This power reflection can result in a reduction in the efficiency and performance of the antenna, as well as the overall performance and efficiency of the RF-EH system.

To achieve impedance matching, different techniques and components can be used, including impedance transformers, transmission lines, LC circuits, and others. These elements are designed to match the impedance of the antenna to the impedance of the device. This results in maximizing power transfer and minimizing reflections.

According to [6], impedance matching can be represented by three basic configurations: L, T, and π, as illustrated in Fig. 7. Among these configurations, the L-network configuration is widely used in RF-EH applications because of its simplicity. It usually consists of only two passive components (an inductor and a capacitor), making it easy to adapt to design requirements. In addition, this configuration is versatile and can be used in different frequency ranges. The L-matching network can also be customized to meet the requirements of each design. The study conducted by [24] em-
Table I: State-of-the-art CCDD rectifiers topologies.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech. (nm)</th>
<th>Freq. (MHz)</th>
<th>N°</th>
<th>$R_L$ (kΩ)</th>
<th>$V_{OUT}$ (V)</th>
<th>Sens. (dBm)</th>
<th>Peak PCE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16] TCASII 2023</td>
<td>28</td>
<td>2450</td>
<td>2</td>
<td>*</td>
<td>0.4</td>
<td>-28.3</td>
<td>31.1</td>
</tr>
<tr>
<td>[8] Electronics 2023△</td>
<td>65</td>
<td>900</td>
<td>(3 + 2)$^\circ$</td>
<td>100</td>
<td>1</td>
<td>-21</td>
<td>88.7</td>
</tr>
<tr>
<td>[17] Sensors 2022</td>
<td>65</td>
<td>900</td>
<td>-</td>
<td>100</td>
<td>1</td>
<td>-18.8</td>
<td>73</td>
</tr>
<tr>
<td>[18] JSSC 2019</td>
<td>65</td>
<td>2450</td>
<td>1</td>
<td>*</td>
<td>0.4</td>
<td>-17.1</td>
<td>48.3</td>
</tr>
<tr>
<td>[19] JSSC 2021</td>
<td>65</td>
<td>2450</td>
<td>1</td>
<td>*</td>
<td>0.4</td>
<td>-26.7</td>
<td>32.3</td>
</tr>
<tr>
<td>[20] VLSI 2022</td>
<td>65</td>
<td>900</td>
<td>5</td>
<td>1000</td>
<td>1</td>
<td>-18.5</td>
<td>19.1</td>
</tr>
<tr>
<td>[13] TCASII 2021</td>
<td>130</td>
<td>900</td>
<td>3</td>
<td>100</td>
<td>-19.2/-18.7</td>
<td>83.7/80.3</td>
<td></td>
</tr>
<tr>
<td>[11] Access 2021</td>
<td>180</td>
<td>953</td>
<td>5</td>
<td>100</td>
<td>3.2</td>
<td>-27.5</td>
<td>78.2</td>
</tr>
<tr>
<td>[10] JSSC 2009</td>
<td>180</td>
<td>953</td>
<td>-</td>
<td>10</td>
<td>-12.5</td>
<td>67</td>
<td></td>
</tr>
<tr>
<td>[21] QJics 2022</td>
<td>180</td>
<td>1050</td>
<td>3</td>
<td>10</td>
<td>-10</td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>[22] ESSCIRC 2022</td>
<td>180</td>
<td>918</td>
<td>1-2-4</td>
<td>1000</td>
<td>1</td>
<td>-16</td>
<td>45</td>
</tr>
<tr>
<td>[3] TCASI 2021</td>
<td>180</td>
<td>403</td>
<td>1</td>
<td>*</td>
<td>0.4-2.2</td>
<td>-17.8</td>
<td>34</td>
</tr>
<tr>
<td>[23] JSSC 2019</td>
<td>180</td>
<td>915</td>
<td>12</td>
<td>*</td>
<td>0.4-2.2</td>
<td>-17.8</td>
<td>34</td>
</tr>
</tbody>
</table>

△ CCDD Hybrid Reconfigurable, * MPPT PMU, $^\circ$ 3 main + 2 auxiliary rectifiers

employed a three-stage tunable impedance matching method to maximize the power transfer from an RF source operating at a frequency of 953 MHz. The proposed scheme intended to eliminate the necessity of complex implementations, such as capacitor bank and large inductors. Through the utilization of this technique, a PCE of 51% was achieved with a sensitivity of $-12$ dBm.

C. Voltage Regulation

The output DC voltage level obtained by the RF to DC conversion is proportional to the power of the input RF signal. Since the RF signal power varies according to the distance between the RF transmitter and the RF-EH and the environment conditions, extra circuits must be added to regulate the output voltage level to the desired value in practical applications.

Figure 8 depicts some strategies presented in the literature that can be used to perform voltage regulation in an RF-EH system. The adoption of one of these voltage regulation techniques depends on the application of the RF-EH system.

The most commonly used strategy for voltage regulation is the addition of a low-dropout (LDO) linear voltage regulator after the rectifier, as illustrated in Fig. 8a [25] [26] [27]. The efficiency of this approach is limited due to the energy loss in the voltage drop element. Additionally, the rectifier output voltage must always be higher than the target output voltage plus the minimum voltage drop. This approach is therefore disadvantageous for ultra-low power batteryless applications since it requires RF signals with high power levels, reducing the system sensitivity.

The DC-DC converter-based approach, shown in Fig. 8b, provides higher conversion efficiency and stability to regulate the signal at lower RF-input power levels. In addition, the regulation is independent of the input power and it can be used either as a buck or as a boost converter. The disadvantage of this application is the complexity of implementation in CMOS processes since duty cycle tuning is required and the systems tend to occupy a large silicon area [3].

Finally, there is the closed-loop regulation approach using an adaptive input match network, as depicted in Fig. 8c and used in this work. In this strategy, the input matching is dynamically changed according to the RF input power level. It is the simplest approach for batteryless applications.
with very low power consumption since the maximum power transference should be satisfied only for reduced input power levels. As the energy can not be stored in batteryless applications, the IMN can work unmatched to the rectifier input impedance in order to reflect the excess of power to the antenna and to make the output DC voltage level at the desired value. In this case, higher converting efficiency is reached only with low power levels [28]. This approach is further discussed in the next section.

III. RF-EH VOLTAGE REGULATION USING ADAPTIVE-IMPEDANCE MATCHING

To illustrate the analysis of adaptive impedance matching for voltage regulation, this section describes the design and simulation results of an RF rectifier with three different adaptive impedance matching network implementations.

The rectifier circuit is based on the CCDD topology implemented in a 65-nm CMOS technology using low-VT transistors. The target input RF frequency is 915-MHz and the rectifier must provide a regulated voltage of 0.4 V in its output.

The methodology for sizing the transistors and capacitors is based on an iterative design with the objective of maximizing the output DC voltage level obtained with a fixed RF input voltage amplitude, as presented in [28]. With this approach, both the circuit sensitivity and PCE can be optimized.

As shown in Fig. 9, the implemented CCDD circuit has four transistors, two P-type (MP1 and MP2) and two N-type (MN1 and MN2). Still, in this topology two flying capacitors are considered, one in the positive half-cycle and the other in the negative half-cycle. Finally, a capacitor ($C_L$) and a resistance ($R_L$) are connected to the output to emulate the applied load.

After executing the sizing methodology for obtaining the maximum output voltage, the resulting width and length of the transistors are $L_N = L_P = 100 \, \text{nm}$, $W_N = 1 \, \mu\text{m}$ and $W_P = 6.18 \, \mu\text{m}$, with 14 fingers. The flying capacitor was designed to $C_{Fly} = 5.1 \, \text{pF}$ and the load was set to $R_L = 10 \, \text{k}\Omega$ and $C_L = 100 \, \text{pF}$.

After sizing the rectifier circuit, the input impedance ($Z\text{REC}$) of this circuit is obtained using harmonic balance (HB) analysis under steady-state conditions. This way, the $Z\text{REC}$ is represented with a complex value, as shown in eq. 1, in which $R\text{RECT}$ and $X\text{RECT}$ are the rectifier input resistance and reactance, respectively.

$$Z_{RECT} = R_{RECT} + jX_{RECT}$$

(1)

Using the HB analysis at Cadence Virtuoso tool we obtained $Z_{REC} = 289.40 - j915.47 \, \Omega$, which is different from the antenna characteristic impedance ($Z_0$), considered equal to $50 \, \Omega$ in this work. Therefore, in order to reduce this signal reflection, it is necessary to design an impedance matching system. To do this, the Smith chart technique [29] is used, and an L-C network strategy is implemented, as seen in Fig. 10. The L-C network values obtained are $L_M = 69 \, \text{nH}$ and $C_M = 243 \, \text{fF}$. As the obtained matching inductance presents a high value to be integrated, it will be considered off-chip in this design.

Next, using S-Parameters analysis, the $|S_{11}|$ parameter is simulated, as shown in Fig. 11, where a frequency range from 500 MHz to 1.4 GHz is considered. This analysis shows that the reflection coefficient reaches approximately -30 dB, with a good match at the operating frequency of 915 MHz.

To regulate the output voltage by using the adaptive matching network it can be adjusted on the fly. The IMN design is composed of series inductors and shunt capacitors. Due to the complexity of changing the magnetic element and also as it is an external device in this work, the use of the capacitor as a control element is the most suitable element for

Fig. 9: Schematic of the designed CCDD rectifier.

Fig. 10: Implemented L-C IMN.

Fig. 11: Simulated input RF reflection ($|S_{11}|$).
To implement this technique, it is necessary to analyze the tuning range of the matching capacitor (ideal capacitor CM, Fig. 10) can be controlled - considering different amplitude levels (50 mV to 110 mV) of the input RF signal - in which the output keeps a value of 0.4 V. Simulated values for $V_{\text{OUT}}$ as a function of $C_M$ are shown in Fig. 12 [29]. It is possible to notice that $C_M$ between 250 fF to 380 fF can be used to keep the output voltage around the desired 0.4 V, for input signals with voltage amplitudes ranging from 70 mV to 110 mV [29].

From these results, it can be seen that the ideal capacitor can be adapted to control the system in such a way that the output voltage is regulated to the fixed value of 0.4 V. For real applications, the variable capacitor can be implemented using discrete steps or a continuous variation range.

A discrete variable capacitor was implemented in [28] using a digital counter to change the values of a programmable capacitor and maintain a fixed rectifier output voltage level. In this implementation, a capacitor bank was used to generate the variable capacitance, as illustrated in Fig. 13. The main bottleneck of this implementation is the parasitic capacitance at the RF nodes and the resistance of the switches, which ultimately affects the tuning of the impedance matching network and reduces the efficiency at lower input power levels.

In [29] a MOS-varactor was used to implement the continuous variable capacitor. In this approach the voltage regulation consists of comparing the rectifier output voltage and tuning the varactor control terminal voltage ($V_C$) through negative feedback, thus adjusting the $C_{VM}$ capacitance, as shown in Fig. 14. Reduced silicon area is presented in this implementation strategy in comparison to the discrete ones.

Besides the varactor used as a variable capacitor to simplify the design of the regulation system, the range of capacitance variation is very reduced due to the limited controlling voltage range available in ULV applications (in this work from 0 to 0.4 V).

As the impedance match is desired only at the reduced input power level, it is possible to use a fixed value L-C network to implement the IMN and to add an extra element that is used only for higher power levels. Therefore, a third way of controlling rectifier output voltage is by using a pair of shunt transistors at the inputs of the rectifier, as shown in Fig 15. The gate of these transistors ($M_{C1}$ and $M_{C2}$) is...

Fig. 12: Analysis of the variation of matching capacitor $C_M$ in the output voltage for the adaptive control.

Fig. 13: Implementation of a variable capacitor with a 4-bit programmable capacitor bank.

Fig. 14: Implementation of a variable capacitor with varactors.

Fig. 15: Implementation of shunt transistors to deviate the excess of energy in the rectifier.

Fig. 16: Analysis of the capacitor matching control voltage by varying the amplitude of the input RF signal to achieve the output voltage of interest.
controlled by the feedback signal \(V_c\), in the same way as the MOS varactor-based topology. Therefore, \(V_c\) should be equal to 0 V for reduced input power levels in order to avoid affecting impedance matching. Moreover, at higher input power levels, the excess energy can be drained by these transistors, according to the \(V_c\) voltage, to keep the output level at 0.4 V.

Figure 16 shows the variation of the output DC voltage level according to the \(V_c\) voltage for input RF signal with amplitude in the range from 50 to 110 mV. It is possible to see that the voltage regulation is guaranteed for input amplitudes higher than 70 mV.

**IV. THE RF-EH CLOSED-LOOP VOLTAGE REGULATION SYSTEM**

The complete proposed RF-EH system is shown in Fig. 17. The implementation of the closed-loop system consists of negative feedback in which the comparator controls the voltage \(V_c\) to keep the output voltage level at 0.4 V. We considered a voltage reference of 240 mV (not shown in this work), thus a resistive voltage divider is used to convert the output DC voltage to the required level at the comparator input. In this case, \(R_1 = 134 \, k\Omega\) and \(R_2 = 200 \, k\Omega\). The comparator is implemented using a classic two-stage Miller OTA. We considered \(R_L = 10 \, k\Omega\) and \(C_L = 100 \, pF\) to emulate the load in the complete system.

The inductor of the IMN is considered to be off-chip due to the large value needed at the 915 MHz frequency. Thus, the capacitance of the ESD circuits \(C_{ESD}\) of 326.8 fF and Bond PAD \(C_{PAD}\) of 30.10 fF together to the bond wire inductance \(L_{BW}\) should be considered as part of the IMN. Considering the interface capacitance and inductance, the parasitic capacitances of the control transistors, and the quality factor of the inductors, the IMN capacitance is adjusted using the Smith chart to \(C_{IM}\) of 2 pF. The inductor of the IMN is implemented off-chip, in which \(L_{IMN}\) is composed by a bond wire \(L_{BW}\) of 4 nH and an external air-core inductor \(L_{EXT}\) of 49 nH. Their quality factor are also taken into account, the bond wire Q factor (QBW) is \(14\) [30] and the commercial inductor Q factor \(Q_{EXT}\) is \(54\) [31]. In terms of insertion losses, these Q factor values can be represented as series-resistors, which are evaluated as \(R_{BW}\) of 1.65 \(\Omega\) and \(R_{EXT}\) of 5.22 \(\Omega\).

The output voltage of the comparator controls the transistor gates, causing the matching impedance to be adjusted to keep the output voltage of the rectifier regulated to 0.4 V. To avoid instabilities at the circuit startup, a startup block is added to the system. It is basically a delay cell that makes the \(V_c\) voltage equal to 0 V for a period of time enough to generate the voltage level of 0.4 V.

The proposed RF-EH is based on the technique of optimizing the maximum power transfer at low input power levels, to guarantee the conversion of an ultra-low power input signal. Thus, the closed-loop regulation of the output voltage is based on impedance mismatch. When the input power is higher than that required by the load, the excess power is reflected back to the antenna.

**V. SIMULATION RESULTS AND DISCUSSION**

The presented RF-EH circuitry was simulated using the Spectre circuit simulator at typical corner considering a temperature of 27 °C.

A noiseless transient simulation was performed with a sinusoidal input signal with amplitude variation from 35 mV to 245 mV. The RF-EH output voltage is shown in Fig. 18. For comparison, the output voltage of the rectifier considering the proposed closed-loop control scheme is shown in conjunction with the output voltage of a rectifier in an open-loop configuration. As can be seen, the output voltage in the closed-loop version remains constant at 0.4 V for input voltages greater than 80 mV, while the output voltage in the open-loop version follows the variation of the input voltage.

Figure 19 shows the system output voltage versus the input signal power. The system requires an input power equal to or higher than \(-14.92\) dBm to provide a reliable (and stable) DC output voltage of 0.4 V. Also, the RF-EH and the rectifier efficiencies are verified according to the input power level, as depicted in Fig. 20. It can be seen that the rectifier peak PCE reached the value of 73.63% for an input signal power level of \(-14.92\) dBm, whereas when considering the complete closed-loop RF-EH system of Fig. 17 a PCE of 48.28% is achieved for the same input signal power level.

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Fig. 17: Complete ULV RF-EH system proposed in this work.
Fig. 18: RF-EH output voltage (with and without the closed loop) versus a varying amplitude RF input signal.

Fig. 19: Output voltage as a function of sensitivity for the closed-loop rectifier.

Fig. 20: Power conversion efficiency of the closed-loop RF-EH system (blue) and rectifier (red) as a function of sensitivity. The indicated points correspond to the beginning of the regulation region ($V_{OUT}=0.4$ V, see Fig. 19).

Table II: Performance comparison with other works from the literature

<table>
<thead>
<tr>
<th>Specification</th>
<th>This*</th>
<th>[3]*</th>
<th>[13]*</th>
<th>[23]*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech. (nm)</td>
<td>65</td>
<td>180</td>
<td>130</td>
<td>180</td>
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<tr>
<td>Freq. (MHz)</td>
<td>915</td>
<td>403.5</td>
<td>900</td>
<td>915</td>
</tr>
<tr>
<td>$V_{OUT}$ (V)</td>
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<td>1.8</td>
<td>1.1</td>
<td>0.8-2.2</td>
</tr>
<tr>
<td>Sens. (dBm)</td>
<td>-14.92</td>
<td>-24</td>
<td>-18.7</td>
<td>-17.8</td>
</tr>
<tr>
<td>PCE (%)</td>
<td>48.28</td>
<td>40.2</td>
<td>80.3</td>
<td>34.4**</td>
</tr>
<tr>
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<td>3</td>
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<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

*△ Schematic-level simulation data; * Measured data; ** Includes the antenna efficiency (93%); LRC - Load Regulation Capability.

pared with other works in literature, as shown in Table II. The work described in [3] presented better sensitivity, but with a smaller peak PCE. Additionally, it is possible to compare the performance of this work with two non-regulated RF-EH converters. The work in [13] presented higher PCEs, but for a $V_{OUT}$ of 1.1 V, using three-stage rectifiers. The circuit presented in [23] presented a lower peak PCE and the $V_{OUT}$ is in the range of 0.8 to 2.2 V.

It can be seen that the use of the closed-loop technique through impedance matching with a control transistor makes it a good candidate for low-voltage batteryless devices when low input power levels are required.

VI. CONCLUSION

This work has discussed the main strategies used in RF energy harvesting circuits to provide a clean and stable DC voltage. The widely used strategies involve an input matching network between the receiving antenna and the rectifier input, followed by a low dropout regulator or a DC-DC converter. However, simpler circuits can be designed with a closed-loop system consisting of only a configurable impedance matching network and a rectifier. This strategy is demonstrated in this work, and a controlled impedance matching network is explored to provide a fixed DC voltage of 0.4 V. The proposed circuit is designed in a standard 65-nm CMOS process and is capable of providing a 0.4-V output voltage from a 915-MHz RF input signal. The system is capable of powering a 16 $\mu$W load, considering a sensitivity of $-14.92$ dBm, and achieves a RF-EH PCE of 48.28%.

The proposed system can be adopted in many RF-power applications, including implantable biomedical systems.

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