Abstract—In this generation, high-speed communication has very demanding. In this respect, optical communication plays a crucial role in meeting the goal of high-speed communication. With the increasing demands of high-speed communication, huge data processing is also needed. Therefore, we have proposed a design of XOR and XNOR gates using five reflective semiconductor optical amplifiers (RSOA). Our proposed gates are dibit logic-based. To increase the reliability of the devise, we have incorporated this logic scheme. Here, we consider the logic state ‘0’ for the absence of pulse and logic state ‘1’ for the presence of pulse. The dibit logic ‘0 1’ and ‘1 0’ are similar as ‘0’ and ‘1’ in digital states, respectively. To check its practical feasibility, we have simulated the proposed design in Matlab software and also quality factor, contrast, and extinction ratios are calculated for this design.

Index Terms—Reflective semiconductor optical amplifier; Dibit logic; XOR gate; Soliton pulse.

I. INTRODUCTION

In this digital era, optical signal processing (OIP) creates a horizon as it shows some benefits, such as high speed, parallel processing, potentially improved security, and low energy consumption. OIP generates hope in the real-time domain rather than the electrical signal processing at large amount of data. In the recent past years, many successes have obtained in OIP. As a result, the number of fundamental OIP devices were obtained. The basic building blocks of the OIP are the logic operations that encourage researchers to design logic gates. They have a number of applications such as adder, subtractor, parity checker, multiplexer, demultiplexer, and encryption devices. In this regard, semiconductor optical amplifiers (SOA) and quantum-dot SOA (QD-SOA) is achieved great attention as optical amplifiers as well as to the OIP. In the case of implementation of QD-SOA, it faces some practical issues. Instead of SOA, reflective-SOA (RSOA) (Fig.1) shows diversified benefits such as high gain, low noise at low injection currents, and low power consumption. The rear facet of RSOA has an highly-reflecting and an anti-reflecting coating is placed at the front facet. Therefore, double amplification of the probe signal is produced in the active region. So researchers use this RSOA technology to develop all-optical logic gates. Now, some outstanding works are given here. Pal and Mukhopadhyay [1] proposed a new concept for the development of an XOR gate applying the squeeze state of light. Maroufi and Bahrepor [2] proposed a XOR gate of three input, using QCA technology. Mukhopadhyay et al. [3] described XOR and XNOR gate utilizing RSOAs and ADMs. They also utilize the dibit logic and frequency encoding scheme. Ktob et al. [4] reported a design of dual-RSOA-based XOR gate and numerically simulated with 120 Gb/s data rate. Maji and Mukherjee [5] proposed an Optical Asymmetric Demultiplexer-based XOR gate in which dual control tera hertz signals are applied. Jasm and Aldabali [6] proposed a design on XOR gate using the third-order Kerr nonlinearity. Here, they introduced the cross-phase and self-phase modulations. Alqukiah et al. [7] proposed the design of logic gates using SOA-based MZI and delay interferometer. The simulation of their design is performed with data rate of 160 Gb/s. Ktob et al. [8] proposed and simulated carrier reservoir SOA-based (CR-SOA) XOR logic gate at the rate 100 Gbps. Mohammadian et al. [9] proposed XOR gate using ring resonator with micro-electromechanical systems. Here, the main cause of changing the refractive index is photelastic effect and due to this 35 nm shifts is observed in resonance wavelength. Mukherjee [10] proposed a XOR and XNOR gates using QDSOA and frequency encoding scheme. They simulated the designs with 1 Tb/s data rate. Mukherjee [11] introduced a QDSOA-based XOR gate and analyzed without using MZI and filters. Raja et al. [12] proposed NOT and XOR gates using Dual SOA. They utilize ternary logic in their designs. To construct these gates, cross-polarization modulation property of SOA is utilized. Singh et al. [13] reported designs of XOR and XNOR gates using QCA technology, and they also extended their work in the three input systems. XOR gate with three input is one of the most crucial components for developing compressors. Using photonic crystal an all-optical XOR gate is developed by Anagha and Jeyachitra [14]. Although the device is exceptionally small dimension, it gives a high contrast ratio. Noonepalle et al. [15] proposed XOR and XNOR gate using T-shaped silicon-based 2-D photonic crystals (PhC) in an air background and finite-difference-time-domain (FDTD) method can help to verify their device performance.

From the literature survey, we have studied that Mukhopadhyay et al. [3] reported XOR and XNOR gate using seven ADMs and they used seven RSOAs as switching device. But our design is prepared using only five RSOAs, so their design is bulkier than our design. Due to the reduction of some components, the size and cost of our device are reduced, and we have also verified this devised design by simulation in the MATLAB software. With the help of this software, we have calculated the quality factor, bit-error rate (BER), contrast, and extinction ratios. The realization of this proposed design can be possible in Photonic Band Gap (PBG) technology. This approach is suitable to nanophotonic devices. The operational data rate is assumed for this simulation to be the inverse of bit period (T)=1000/(data rate) = 8 ps @ 125 Gb/s.
II. RSOA WORKS AS A SWITCH

The concept of cross-gain modulation is utilized to form the RSOA-based switch. It is used widely in 5G-based networks [16], wave division multiplexing (WDM) [17], and it is also very useful in passive optical networks (PON) [18]. If a high power control and a low power probe signals are introduced into the RSOA, due to the high power signal gain saturation, occur and this creates the gain compression in the RSOA. As a result, output becomes low. Without pump signal, the gain of RSOA is high (unsaturated gain, \( G_0 \)), as the probe signal becomes amplified and comes out that denotes the high state of the switch. Gain modulation produces due to the control signal that creates a variation in the power of the probe signal. Fig. 1 indicates the RSOA’s diagram. In the presence of control signal, it experiences gain compression (\( G(t) \)) which defined by the following equation\([19, 20]\),

\[
G(t) = e^{2h(t)}
\]  

(1)

\[
\frac{dh(t)}{dt} = \frac{g_0 L - h(t)}{\tau} - \frac{P_{in}(t)}{E_s}[\exp(h(t)) - 1]
\]  

(2)

Here, the input power is \( P_{in}(t) \) and the saturation energy is \( E_s \). The gain coefficient \( g_0 \) is related \([19]\) with the unsaturated gain by the Eq.3.

\[
G_0 = \exp(Lg_0 - L\alpha_d)
\]  

(3)

In this equation, the internal loss of RSOA is denoted by \( \alpha_d \) and \( L \) indicates the active length of the RSOA. With the help of Eqs. 2 and 3, we obtained the Eq. 4.

\[
h(t) = \ln[1 - \left(1 - \frac{1}{G_0}\right)e^{\frac{E_c(t)}{E_s}}]
\]  

(4)

Here, \( E_c(t) \) indicates the control pulse’s energy. We applied soliton pulse train for probe and pump signals as

\[
P(t) = \sum_{n=1}^{n=N} a_{nA,B}P_{soliton}sech^2\left(\frac{1.763(t - nT)}{\tau_{fwhm}}\right)
\]  

(5)

where Maximum power of soliton is defined as,

\[
P_{soliton} = \frac{1.763}{2\pi} \frac{A_{eff}X_0^3D}{n_2C^2\tau_{fwhm}}
\]  

. Table II represents all the parameter’s value and

\[
E_{cp}(t \to \infty) = P_{soliton} \times \tau_{fwhm} = E_c
\]

represents the total control pulse energy.

III. OPERATION OF PROPOSED XOR AND XNOR GATE

This paragraph explain the working procedure of our devised design. This design constitutes five RSOAs and also some extra components like beam splitter, combiner, mirror etc. To explain the operation, we used soliton pulses \([21, 22]\) as input signals.

Here, presence of soliton pulse takes as digital state ‘1’ and absence of the pulse takes as ‘0’. The dibit-based \([23]\) logic means when two bits are taken back-to-back, i.e., ’01’ and ‘10’. Here, dibit logic ‘01’ and ‘10’ are specify the digital state ‘0’ and ‘1’ respectively.

The logic of XOR gate is \( X = AB + \bar{AB} \) and for XNOR gate is \( Y = AB + \bar{AB} \). In Fig. 2. A \((A_1 \text{ and } A_2)\) and B \((B_1 \text{ and } B_2)\) act as the dibit inputs and X \((X_1 \text{ and } X_2)\) and Y \((Y_1 \text{ and } Y_2)\) represent the outputs of the XOR and XNOR gate.

The following cases properly explain the working procedure of our devised design.

Case1: In this case, \( A=0 \), and \( B=0 \) signals are applied that means 1st bit, \( A_1 = 0 \) and 2nd bit, \( A_2 = 1 \) and also for B i.e., 1st bit \( B_1 = 1 \) and 2nd bit, \( B_2 = 0 \). These combinations are injected into the RSOA1 and RSOA2. Without the probe signal, RSOA1’s and RSOA2’s outputs are low, i.e., ‘0’. The output of RSOA2 is injected into RSOA3 and RSOA4, which serve the purpose of pumping and probing signals, respectively. The output of RSOA1 is also injected into RSOA3 and RSOA4, which serve the purpose of probing and pumping signals, respectively. Without pump and probe signals, the output of RSOA3 and RSOA4 is ‘0’. One part of these outputs represent one of the dibit outputs of XOR and XNOR as \(X_1 \text{ and } Y_1\). Another part represents the pump signal of RSOA5 and also a continuous pulse (C) acts as a probe signal of RSOA5, hence output of RSOA5 is ‘1’. This output represents another dibit outputs of XOR and XNOR as \(X_2 \text{ and } Y_2\).

Case2: In this case, \( A=0 \), and \( B=1 \) signals are applied that means 1st bit, \( A_1 = 0 \) and 2nd bit, \( A_2 = 1 \) and also for B i.e., 1st bit \( B_1 = 1 \) and 2nd bit, \( B_2 = 0 \). These combinations are injected into the RSOA1 and RSOA2. Without the probe signal, RSOA1’s output is low, i.e., ‘0’, and without the pump signal, the probe signal in RSOA2 amplified, so its output is ‘1’. The output of RSOA2 is injected into RSOA3 and RSOA4, which serve the purpose of pumping and probing signals, respectively. The output of RSOA1 is also injected into RSOA3 and RSOA4, which serve the purpose of probing and pumping signals, respectively. Without pump and probe signals, the output of RSOA3 and RSOA4 is ‘0’. One part of these outputs represents one of the dibit outputs of XOR and XNOR as \(X_1 \text{ and } Y_2\). Another part represents the pump signal of RSOA5 and also a continuous pulse (C) acts as a probe signal of RSOA5, hence output of RSOA5 is ‘0’. This output represents another dibit outputs of XOR and XNOR as \(X_2 \text{ and } Y_1\). Therefore, the outputs of XOR and XNOR gate are \(X=1 \text{ and } Y=0\).
and \( Y = 0 \) (\( Y_1 = 0, Y_2 = 1 \)) respectively, for the inputs \( A = 0 \) and \( B = 1 \).

Case 3: In this case, \( A = 1 \), and \( B = 0 \) signals are applied that means 1st bit, \( A_1 = 1 \) and 2nd bit, \( A_2 = 0 \) and also for \( B \) i.e., 1st bit \( B_1 = 0 \) and 2nd bit, \( B_2 = 1 \). These combinations are injected into the RSOA1 and RSOA2. Without the probe signal, RSOA2’s output is low, i.e., ‘0’, and without the pump signal, the probe signal in RSOA1 amplified, so its output is ‘1’. The output of RSOA2 is injected into RSOA3 and RSOA4, which serve the purpose of pumping and probing signals, respectively. The output of RSOA1 is also injected into RSOA3 and RSOA4, which serve the purpose of probing and pumping signals, respectively. Without the probe signal, RSOA4’s output is low, i.e., ‘0’, and without the pump signal, the probe signal in RSOA3 amplified, so its output is ‘1’. One part of RSOA3’s output represents one of the dibit outputs of XOR and XNOR as \( X_1 \) and \( Y_1 \). Another part represents the pump signal of RSOA5 and also a continuous pulse (C) acts as a probe signal of RSOA5, hence output of RSOA5 is ‘0’. This output represents another dibit outputs of XOR and XNOR as \( X_2 \) and \( Y_2 \).

Case 4: In this case, \( A = 1 \), and \( B = 1 \) signals are applied that means 1st bit, \( A_1 = 1 \) and 2nd bit, \( A_2 = 0 \) and also for \( B \) i.e., 1st bit \( B_1 = 1 \) and 2nd bit, \( B_2 = 0 \). When these combinations are injected into the RSOA1 and RSOA2, the outputs are ‘1’. Because in both the cases, the probe signals are present whereas pump signals are absent, so the outputs of RSOA1 and RSOA2 are high. The output of RSOA2 is injected into RSOA3 and RSOA4, which serve the purpose of pumping and probing signals, respectively. The output of RSOA1 is also injected into RSOA3 and RSOA4, which serve the purpose of probing and pumping signals, respectively. With pump and probe signals, the output’s of RSOA3 and RSOA4 is low, i.e., ‘0’. One part of these outputs represent one of the dibit outputs of XOR and XNOR as \( X_1 \) and \( Y_2 \). Another part represents the pump signal of RSOA5 and also a continuous pulse (C) acts as a probe signal of RSOA5, hence output of RSOA5 is ‘1’. This output represents another dibit outputs of XOR and XNOR as \( X_2 \) and \( Y_1 \). Therefore, the outputs of XOR and XNOR gate are \( X = 0 \) (\( X_1 = 0, X_2 = 1 \)) and \( Y = 1 \) (\( Y_1 = 1, Y_2 = 0 \)) respectively, for the inputs \( A = 1 \) and \( B = 1 \).

### IV. Simulation of Proposed XOR and XNOR Gate

To construct the XOR and XNOR gate, we have used five RSOAs. Here, the input signals \( A_1, A_2, B_1, B_2 \) are the same, i.e., \( A = 0, B = 0 \), and \( A = 1, B = 1 \). The outputs of XOR and XNOR gate are \( X_1 = 1 \) and \( X_2 = 0 \), and \( Y_1 = 0 \) and \( Y_2 = 1 \). The filters tuned to the probe signal frequency. For the simulation of this design, we have used some parameters [24] for RSOA and soliton pulse. Matlab software is used to perform this numerical simulation. For this simulation, we take some parameters which is given in Table I.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>coefficient of non-linearity</td>
<td>( n_2 )</td>
<td>( 2.6 \times 10^{-20} m^2/W )</td>
</tr>
<tr>
<td>density of Carrier</td>
<td>( N_c )</td>
<td>( 10^{14} m^{-3} )</td>
</tr>
<tr>
<td>saturation Energy</td>
<td>( E_s )</td>
<td>480 fJ</td>
</tr>
<tr>
<td>confinement factor</td>
<td>( \Gamma )</td>
<td>0.48</td>
</tr>
<tr>
<td>signal’s Wavelength</td>
<td>( \lambda )</td>
<td>1550 nm</td>
</tr>
<tr>
<td>ASE factor</td>
<td>( N_{sp} )</td>
<td>2</td>
</tr>
<tr>
<td>internal loss of the waveguide</td>
<td>( \alpha_{D} )</td>
<td>2700 m(^{-1} )</td>
</tr>
<tr>
<td>optical bandwidth</td>
<td>( B_0 )</td>
<td>3 nm</td>
</tr>
<tr>
<td>length of the active medium</td>
<td>( L )</td>
<td>150 ( \mu )m</td>
</tr>
<tr>
<td>differential gain</td>
<td>( \alpha_{X} )</td>
<td>( 3.3 \times 10^{-20} m^2 )</td>
</tr>
<tr>
<td>active region’s width</td>
<td>( w )</td>
<td>1.5 ( \mu )m</td>
</tr>
<tr>
<td>depth of the active region</td>
<td>( d )</td>
<td>250 nm</td>
</tr>
<tr>
<td>bit Period</td>
<td>( \tau )</td>
<td>8 ps</td>
</tr>
<tr>
<td>energy of Control pulse</td>
<td>( E_c )</td>
<td>40 fJ</td>
</tr>
<tr>
<td>injection Current</td>
<td>( I )</td>
<td>400 mA</td>
</tr>
<tr>
<td>dispersion constant</td>
<td>( D )</td>
<td>1 ps/(nm km)</td>
</tr>
<tr>
<td>speed of light</td>
<td>( C )</td>
<td>( 3 \times 10^8 ) m/s</td>
</tr>
<tr>
<td>fiber effective area</td>
<td>( A_{eff} )</td>
<td>( 5 \times 10^{-13} m^2 )</td>
</tr>
</tbody>
</table>

### V. Results and Discussion

In this paragraph, we have applied the soliton pulse train to the proposed design as input signals 3 & 4 and the output signals are obtained using simulation. The inputs and output signals are given in Figs. 3, 4, 5 & 6. In 24 ps, we applied ‘1’ (with soliton pulse) in \( A_1 \) and ‘0’ (without soliton pulse)
Table II. Dibit-based truth table of XOR and XNOR gate.

<table>
<thead>
<tr>
<th>$A_1$</th>
<th>$A_2$</th>
<th>Digital state</th>
<th>$B_1$</th>
<th>$B_2$</th>
<th>Digital state</th>
<th>$X_1$</th>
<th>$X_2$</th>
<th>Digital state</th>
<th>$Y_1$</th>
<th>$Y_2$</th>
<th>Digital state</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Table III. Simulation results of proposed XOR and XNOR gate.

<table>
<thead>
<tr>
<th>Output signals</th>
<th>$Q$(dB)</th>
<th>$CR$(dB)</th>
<th>ER (dB)</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X_1$</td>
<td>30.57</td>
<td>45.41</td>
<td>21.97</td>
<td>$1.28 \times 10^{-123}$</td>
</tr>
<tr>
<td>$X_2$</td>
<td>23.57</td>
<td>39.48</td>
<td>21.97</td>
<td>$3.76 \times 10^{-123}$</td>
</tr>
<tr>
<td>$Y_1$</td>
<td>23.57</td>
<td>39.48</td>
<td>21.97</td>
<td>$3.76 \times 10^{-123}$</td>
</tr>
<tr>
<td>$Y_2$</td>
<td>30.57</td>
<td>45.41</td>
<td>21.97</td>
<td>$1.28 \times 10^{-205}$</td>
</tr>
</tbody>
</table>

Table IV. Comparative study of dibit-based XOR and XNOR gate.

<table>
<thead>
<tr>
<th>Work</th>
<th>Used logic</th>
<th>Number of Components</th>
<th>$Q$(dB)</th>
<th>$CR$(dB)</th>
<th>ER (dB)</th>
<th>BER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mukhopadhyay et al. [3]</td>
<td>Dibit-based</td>
<td>7 RSOA &amp; 7 ADM</td>
<td>Not Calculated</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed work</td>
<td>Dibit-based</td>
<td>5 RSOA only</td>
<td>30.57</td>
<td>45.41</td>
<td>21.97</td>
<td>$1.28 \times 10^{205}$</td>
</tr>
</tbody>
</table>

Fig. 3 Dibit input signal waveform (A)

Fig. 4 Dibit input signal waveform (B)

Fig. 5 Dibit output signal waveform of XOR gate

Fig. 6 Dibit output signal waveform of XNOR gate

In $A_2$ that indicates dibit input signal $A=1$, and ‘0’ (without soliton pulse) in $B_1$ and ‘1’ (with soliton pulse) in $B_2$ that implies $B=0$. Upon completion of simulation, we obtained $X_1=1$ and $X_2=0$, which indicate output $X=1$ for XOR gate and $Y_1=0$ and $Y_2=1$, which indicate output $Y=0$ for XNOR gate. In 52 ps, we applied ‘0’ (without soliton pulse) in $A_1$ and ‘1’ (with soliton pulse) in $A_2$ that indicates dibit input signal $A=0$, and ‘1’ (with soliton pulse) in $B_1$ and ‘0’ (without soliton pulse) in $B_2$ that indicates $B=1$. Upon completion simulation, we obtained $X_1=1$ and $X_2=0$, which indicate the output $X=1$ for XOR gate and $Y_1=0$ and $Y_2=1$, which indicate output $Y=0$ for XNOR gate. In 56 ps, we applied ‘1’ (with soliton pulse) in $A_1$ and ‘0’ (without soliton pulse) in $A_2$ that indicates dibit input signal $A=1$, and ‘1’ in $B_1$ and ‘0’ in $B_2$ that indicates $B=1$. Upon completion of simulation, we obtained $X_1=0$ and $X_2=1$, which indicate output $X=0$ for XOR gate and $Y_1=1$ and $Y_2=0$, which indicate output $Y=1$ for XNOR gate. From the aforementioned discussion, we say that the input and output graphs clearly represent the dibit-based truth table II of the XOR and XNOR gates.

For the proposed XOR and XNOR gates, we have calculated the quality factor ($Q$) [20, 25, 26], extinction ratio (ER) [20, 25, 26], contrast ratio (CR) [20, 25], and bit-error rate (BER) [20, 25] of the output signals, and these given in Table III. We have also done a comparative study with the proposed design. Mukhopadhyay et al. [3] reported the XOR and XNOR gates using seven ADMs, seven RSOAs,
and dibit logic and Q, ER, CR, and BER are not calculated in their design. In our proposed design, we have used only five RSOAs and no ADMs. We also have calculated the Q, ER, CR, and BER of the output signals. The input and output signals waveform are similar with the truth table (Table II) of the XOR and XNOR. We also have presented a comparative study in Table IV.

VI. Conclusion

The characteristics of photons have inspired scientists to develop logic gates in an all-optical realm. In this communication, we have introduced a dibit-based XOR and XNOR gate in a single circuit. Our design is prepared using only five RSOAs, so the design [3] is bulkier than our design. Due to the reduction in the components, the size and cost of our device are reduced, and we have also verified this devised design by simulation in the MATLAB software. The simulation results show that the suggested design yields the expected results. This design appears to be a complex and voluminous, but using photonic Band Gap (PBG), our device is optimized in nano-photonic devices. Delays are occurred due to RSOAs, circulator and beam splitter. But delay due to the circulator and beam splitter is optimized in nano-photonic devices. From the Table III, our devised design shows the low BER. In future, we will concentrate on designing the full adder, subtractor, parity generator, and comparator, etc.

References


