Abstract — Technology scaling greatly benefits discrete-time and N-path filters, making them perfect for Software-Defined Radio and wireless Standards designs. Both strategies enable wide-band and narrowband solutions, high selectivity and easy programmability with low power and high linearity. This paper presents a review of discrete-time and N-path based receivers. Their architecture similarities are examined, focusing on discrete-time receiver building blocks whose features and advances are detailed. An extensive literature review of the State-of-the-Art on these strategies is conducted.

Index Terms — Discrete-time receiver; Charge-Sharing Bandpass filter; N-path filter; Mixer-first receiver; CMOS

I. INTRODUCTION

Time-variant tunable N-path and discrete-time filters have been around since 1940’s [1-9]. Either using active voltage sampling [7-9], or passive sampling implementations [2-5], their applications were initially limited to low frequencies until the 2000’s. With the increased technology scaling and integration, these circuits quickly migrated to radio-frequency (RF) communications, achieving a much higher frequency range [10-28].

Both approaches benefit from technology scaling, with faster and smaller MOS switches and a reduction in power consumption for clock generation [20,27-29]. Furthermore, switched-capacitor based filters are generally much less affected by process, voltage, and temperature (PVT) variations [26,27].

By enabling center frequency tuning through simple sampling rate adjustment, both filters prove to be adequate for Software-Defined Radio (SDR) implementations or other re-configurable receivers (RX) [21,23,30,31], besides being well-suited for high-performance or low-power commercial standards [12,18-20,32-35]. However, the RX architectures in which they are typically used may differ. N-path based receivers usually benefit from the direct conversion (DC) IF architecture [11,14-16], perhaps with a few exceptions in low intermediate-frequency (IF) like [12,13,35]. On the other hand, discrete-time receivers (DT-RX) are used in super-heterodyne or high IF (HIF) architectures [20-22,25-28,32,36,37], and in direct conversion [18,19,31,38,39]. While DC-IF architectures lead to the absence of image issues, high-IF offers other interesting features like improved resilience to second-order intermodulation, DC offset, and flicker-noise.

This paper reviews the literature on discrete-time and N-path filter based receivers, attempting to better identify their design trade-offs. N-path concepts are briefly discussed in Section II, and for a detailed review on NPF design and advanced architectures, the reader is referred to [14,29,40,41]. On the other hand, the DT-RX fundamental concepts are presented in detail in Section III., starting from the basic concepts of charge sampling up to advanced architectures of band-pass filters and passive mixer translation. Section IV. presents the State-of-the-Art in DT-RX and N-path RX.

II. N-PATH FILTER

The concept of N-path filter (NPF) is presented in Fig. 1 [4,5]. Each of the identical N paths is implemented with two mixers and a linear time-invariant (LTI) filter with an h(t) impulse response. The mixers are driven by non-overlapped phase-shifted versions of p(t) and q(t) clocks. Two successive paths are time-shifted by T/N where T is the mixer’s LO clock period.

When p(t) is a simple baseband low-pass filter (LPF), the mixer translation effect results in an effective band-pass filter (BPF) around the mixing harmonics. Accompanied by the mixer translation, there is a beneficial increase in the quality factor (Q) of the overall filter.

A differential implementation of the NPF is shown in Fig. 2(a) for an RC LPF with q(t) = p(t). Since the resistor is a memory-less element, the circuit can also be simplified as a single-input 4-path filter shown in Fig. 2(b) with the output voltage V_{out} probed at the capacitor.

The transfer function $H_0(f)$ of the NPF in Fig. 2(b) is given by (1) [23], in which $D \cdot T_S$ is the duration of the

![Fig. 1 Architecture of an single-ended N-path filter.](image)
pulse and \( D \) is the duty-cycle of the multiphase clock with period \( T_S \).

\[
H_0(f) = \frac{N}{1 + jf/f_{rc}} \times \left( D + \frac{1 + e^{j\pi(1-2D)f/f_s}}{2\pi f_{rc}/f_S} \times \left( \frac{-e^{j\pi Df/f_s} + e^{-2\pi Df_{rc}/f_S}}{e^{j\pi f/f_s} + e^{-2\pi Df_{rc}/f_S}} \right) \times \left( 1 + jf/f_{rc} \right) \right) + (1 - ND) \quad (1)
\]

where \( f_{rc} = 1/(\pi RC) \) is the 3-dB bandwidth corner frequency of the RC filter and \( f_S = 1/T_S \) is the sampling frequency. The \( Q \)-factor of the implemented BPF is defined by \( f_S/f_{rc} \) and can be increased further for the same \( f_{rc} \) bandwidth by adjusting \( f_S \) or by reducing \( f_{rc} \).

Fig. 3 shows the simulated transfer function of the ideal 4-path filter at \( f_S = 1 \) GHz for \( D = 1/4 \), \( R=100 \Omega \) and \( C=50 \text{pF} \) [23, 29]. Due to the differential architecture, there are no peaks at the even harmonics of the transfer function, only at the odd harmonics. As discussed in [23, 42], the resistance of the designed switches has to be carefully considered in a practical implementation to avoid degradation of the transfer function, as observed in the figure. The switches of lower resistance would require wider devices, with a consequent increase in the power consumption of the clock generation.

By increasing the number of paths \( N \), the attenuation at the harmonics is reduced but the folding appears at a higher harmonic order \((N-1) \times f_S \) [23], offering a design trade-off. Besides, increasing \( N \) also has a strong impact in the power consumption of the clock buffers.

### III. Charge-Sharing Discrete-Time Filters

Charge sharing (CS) filters are based on current sampling introduced in [43–46]. The basic concept is illustrated in Fig. 4. After the reset of capacitor \( C \) at \( \phi_2 \), the current is integrated over the capacitor during the sampling time \( T_s = t_2 - t_1 \). This window-integrated sampling (WIS) process implements an intrinsic Sinc filter defined as (2) [44].

\[
|H_P(f)| = T_s \sin \left( \frac{\pi f T_s}{T_s} \right) = T_s \sin (f T_s) \quad (2)
\]

In the analysis of CS signal processing, the sampling rate is usually defined by the duration of the pulse \( T_s \) as opposed to the multiphase sampling time (also denoted by \( T_s \)) presented in the NPF analysis.

#### A. Infinite Impulse Response Filter

The simplest infinite-impulse response (IIR) filter is implemented with an additional switched-capacitor \( C_H \) to the passive sampling structure [47]. Now the voltage sampling (VS) structure is equivalent to a resistor \( R = 1/(f_SC_H) \). Whole architecture, \( C_H \) combining with \( C_S \), results in a first-order low-pass filter.

A CS version of the IIR filter is implemented in Fig. 6a, [24, 48–51]. In the circuit, the current \( i_{in} \) is integrated over \( C_S \) during \( T_s \) creating a charge packet \( q_{in}[n] \) defined by (3).

\[
q_{in}[n] = \int_{(n-1)T_s}^{nT_s} i_{in}(t) \, dt \quad (3)
\]
During $\phi_1$, the charge is also shared between $C_H$ and $C_S$ which forms a low pass filter with transfer function defined by (4) where $\alpha = C_H/(C_H + C_S)$. After reading $V_{out}$, the capacitor is reset to zero at $\phi_2$ to prepare for the next cycle reading. This process implements a first-order “lossy” IIR filter with the transfer function in z-domain given by (4).

$$H_{IIR}(z) = \frac{V_{out}(z)}{Q_{in}(z)} = \frac{1}{C_S} \left( 1 - \frac{1 - \alpha}{1 - \alpha z^{-1}} \right)$$

(4)

The effect of the WIS filter is observed in Fig. 6b, where the replicas folded to the baseband due to the aliasing are strongly attenuated by the WIS filter. This results in sinc anti-aliasing filtering [26]. Hence, an “analog-like” filtering with very small aliasing effects can be achieved with better performance than its voltage-sampling counterpart.

To further improve the stop-band rejection of the DT IIR low-pass filter, another approach was introduced in [51] that implements a sinc$^2(\pi f/fs)$ function by providing a pseudo-linear interpolation through an L-fold time-window interpolation technique. Moreover, by dynamically re-engaging the history capacitor in each stage, a higher-order filtering was achieved. By applying these two techniques to a 4th-order IIR LPF, the highest out-of-band rejection among analog filters was achieved.

B. Finite-Impulse Response Filter

Finite-impulse response (FIR) filters can also be implemented using the charge-sharing concept. Typically used in a multirate DT receiver as an anti-aliasing filter for the downsampling process, an N-tap FIR filter with uniform weights is shown in Fig. 7a [19, 30, 52]. Also known as a time-domain moving average filter, the circuit successively integrates $N$ current samples over the capacitor $C$, which is read and immediately reset, with a resulting decimation factor $N$. The implemented transfer function in the z-domain is presented in (5).

$$H_{FIR}(z) = \frac{1 - \frac{z^{-N}}{1 - z^{-1}}}{1} = 1 + z^{-1} + z^{-2} + \ldots + z^{-(N-1)}$$

(5)

Due to the 50% duty-cycle current samples in the circuit proposed in Fig. 7a, the WIS filter produces a null at $2 \times f_s$ as observed in Fig. 7b. The FIR TF has $(N-1)$ nulls, which can be explored in the DT signal processing to attenuate the close-in interferers [30, 53]. The stopband $f_{SB}$ for an attenuation $\alpha_{At}$ at the N-th null is defined by (6) [30].

$$f_{SB}^N \approx 2\alpha_{At}N f_s$$

(6)

An alternative full-rate implementation ($D = 100\%$) proposed in [30] has $N$ parallel FIR+IIR implementations, but with slightly complex clock generation and higher power consumption due to the increased number of switches.

C. CS Complex Band-Pass Filters

Complex band-pass filters (BPF) can also be implemented using the CS signal processing, enabling the development of intermediate frequency (IF) super-heterodyne receivers [26, 50, 54, 55]. In Fig. 8, a band-pass first-order IIR filter implementation is presented in its differential form. The $4/4$ CS BPF has 4 inputs and 4 rotating capacitors ($C_{R1}$ to $C_{R4}$) and in this topology, the charge over a specific $C_R$ is sequentially shared with the 4 inputs. This rotation implements a complex IIR filter where the charge input ($Q_{in} = Q_{in,1} + jQ_{in,Q}$) is transferred to a voltage output $V_{out} = V_{out,1} + jV_{out,Q}$. The transfer function in the z-domain is shown in (7) [26].

$$H(z) = \frac{1/(C_H + C_R)}{1 - [\alpha + j(1-\alpha)]z^{-1}}$$

(7)
where \( \alpha = C_H/(C_H + C_R) \). \( C_H \) and \( C_R \) are history and rotating capacitor respectively.

The complex IIR filter presents replicas at \( f_s + nf \) defined by the non-overlapping clocks \( \phi_1 \) to \( \phi_4 \), for an integer \( n \). Benefitting from the charge-sharing implementation, replicas are minimized by the built-in WIS filter (2), thus reducing the impact of the intrinsic discrete-time aliasing. This effect is observed in Fig. 9 which presents the combined transfer function of the 4/4 CS-BPF filter (dashed-black line) and the 4/4 filter combined with its WIS pulse shaping filter (black line). This plot is obtained from (7) with \( f_S = 1 \) GHz \( D=1/4 \) and 20-MHz center frequency (\( f_c \)).

By changing the number of inputs (\( M \)) and phases (\( N \)) of a CS-BPF, higher-order filters can be obtained [28, 49]. The general transfer function of the M/N CS BPF is presented in (8). Based on the same CS concept, all the solutions produce WIS nulls at the same harmonics. Fig. 9 shows 4/4, 4/8, 8/8, and 4/12 transfer function combinations.

\[
H(z) = \frac{k \left[ (1 - \alpha) z^{-1} \right]^{N/M-1}}{1 - \alpha z^{-1} \left[ (1 - \alpha) z^{-1} \right]^{N/M}}
\]

(8)

BPF center frequency (\( f_c \)) is easily programmed by changing the ratio between \( C_H \) and \( C_R \) for a specific \( f_s \) according to (9), as shown in [27, 54]

\[
f_c = \frac{f_s}{2\pi} \arctan \left[ \frac{(1 - \alpha) \sin(2\pi/N)}{\alpha + (1 - \alpha) \cos(2\pi/N)} \right]
\]

(9)

CS BPF have a constant \( Q \)-factor for each selected \( M \) and \( N \). As a consequence, with \( Q = f_s/Bw_{3\text{dB}} = 0.5 \) for the 4/4 CS BPF, an ideal 3-dB bandwidth of 40 MHz is achieved for a programmed \( f_c = 20 \) MHz, and \( Bw = 10 \) MHz for \( f_c = 5 \) MHz, as observed in Fig. 10. The 4/8 CS BPF has \( Q = 1.2 \) for ideal switches.

To summarize, \( Q \)-factor and selectivity of the BPF are defined by topology and center frequency. Nevertheless, modified BPFs can increase selectivity further through advanced strategies like adding a programmable feedback structure to the differential input [37, 49] or interleaved charge-sharing techniques [56], hence making the structure more flexible.

D. Advanced CS Strategies

By increasing the number of inputs and phases, a sharper complex BPF was achieved while adding complexity to the system and demanding higher clock generation power. Hence, techniques that enhance filter selectivity without increasing its complexity becomes an interesting topic of study.

Positive feedback is one way to boost selectivity of the CS BPF [37] without adding complexity. Besides, this technique allows for the control of the quality factor by changing loop-gain of the positive feedback, as depicted on figure 11a. Of course, when a positive feedback is used, the designer must be aware that instability becomes an issue if the loop-gain is too large. For the ideal TF, stability was verified with feedback gain \( \beta > -0.5 \) [37]. Fig. 11b shows how the positive feedback is implemented with two simple inverters.

Another way to overcome this challenge was introduced by [55]. A 4/4 complex CS BPF which achieves sharper filtering in comparison to the 4/8 CS BPF. A clock reusing technique is used in this architecture to provide local low pass filter in each arm alongside with the global complex CS band pass filter. Thus, leading to much steeper filtering while keeping the number of required phases and inputs (see Fig. 12a).

E. RF Sampling Mixer

Another important building block for the DT-RX is the RF sampling mixer. For this purpose, current sampling
(or charge sampling) is again the recommended choice in newer technologies since thermal noise folding is reduced by the charge sampling window [57, 58]. Besides, the sampling capacitor can be independently designed to minimize clock feedthrough with regards to the constant group delay [43, 44, 57].

Band-pass charge sampling was added to the RF mixer functionality in [46, 59], with additional FIR and IIR + FIR embedded filters, respectively. Thus, implementing high-Q filters and reducing the impact of folding at higher harmonics.

Passive quadrature charge sampling mixer was proposed in [60], also enabling its use in super-heterodyne RX architectures. When driven by 25% duty-cycle clocks, the sampling mixer show several advantages regarding cross-talk, flicker noise, linearity and image rejection [60–64]. These advantages come mainly from the improved clock strategy that eliminates the overlap between clock phases which is a problem in 50% duty-cycle quadrature mixers reducing cross-talk and increasing image rejection. A lower flicker noise corner is also observed due to the reduced DC current consumption and small voltage swing at the output contributes to better IIP2 and IIP3 results. The main drawback of the 25% duty-cycle mixer is the (current) conversion gain, estimated as $\sqrt{2}/\pi$ [62].

Design of quadrature RF sampling mixer is basically performed by sizing mixer switches for a trade-off between power, noise and linearity. Passive mixers also allow current flow in both directions, with a consequent transparency between input and output. The input impedance of a quadrature passive mixer was studied in detail in [13, 62, 65]. For the 25% duty-cycle current-driven passive mixer, its output load $Z_{BB}$ is frequency translated to $f_{LO}$, $2f_{LO}$, $3f_{LO}$, ... at $Z_{in}$ input, according to (10).

$$Z_{in}(\omega) \approx R_{sw} + \frac{1}{4} Z_{BB}(\omega) + \frac{2}{\pi^2} [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] + \frac{1}{\pi^2} [Z_{BB}(\omega - 2\omega_{LO}) + Z_{BB}(\omega + 2\omega_{LO})] + \frac{2}{9\pi^2} [Z_{BB}(\omega - 3\omega_{LO}) + Z_{BB}(\omega + 3\omega_{LO})] + \ldots$$

**F. Quadrature Sampling Mixer + CS-BPF**

By combining the quadrature sampling mixer with the 4/4 CS BPF as presented in [20, 26, 27, 37], the characteristics of both N-path filter and complex IIR filter are achieved.

To illustrate the NPF function, the current $i_{ref}$ in Fig. 13 is integrated over the capacitor $C_{R1}$ during $\phi_1$, with a similar process for $C_{R2}$ and so forth, resulting in a 4-Path filter equivalent circuit (see Fig. 2b).

Simultaneously, in $\phi_1$, the charges accumulated over the three other rotating capacitors $C_{R2}, C_{R3}, C_{R4}$ are shared with the respective history capacitors $C_{H2}, C_{H3}, C_{H4}$, implementing an IIR complex filter presented in Section C.

The normalized input impedance seen at the mixer + 4/4 CS BPF is compared with the ideal voltage transfer function of the 4-Path filter in Fig. 14. The input impedance was
obtained considering the transfer function presented in (7) and the transparency effect of the sampling mixer in the frequency domain (10), normalized by the baseband impedance \(Z_{BB}(\omega)/4\). A very similar behavior can be observed concerning the replicas since the NPF is also affected by the WIS filter. It should be noted that the input signal is translated by the mixer and the downconverted signal is improved by an additional Sinc filter, further attenuating the 3rd harmonic by \(20 \log_{10}(\text{sinc}(3/4)) \approx -10\) dB. Besides, the improved structure adds flexibility to the design process by enabling different IF’s with a consequent \(Q\)-factor increase.

As a consequence of the mixer transparency effect [65, 66, 68], its output impedance is translated back from baseband to RF and a higher programmable \(Q\)-factor is achieved at the mixer input with this BPF translation, according to (11).

\[
Q_{RF} = \frac{Q_{IF} f_{RF}}{f_c} \tag{11}
\]

where \(f_{RF}\) is RF center frequency and \(Q_{IF}\) is the constant \(Q\)-factor of the selected filter topology.

This effect is observed in Fig. 14, where IF is varied using (9) by changing the capacitor ratio with an improvement in channel selectivity and in wideband blocker protection.

It should be pointed out that even with an excellent wideband interference suppression, both the mixer + CS BPF and the NPF architectures still suffer from reciprocal mixing. This happens because the mixers are also affected by the phase noise and the local oscillator noise is consequently translated to the mixer input. Hence, this solution should be carefully evaluated together with the phase noise requirements of the receiver.

IV. DTRX AND N-PATH BASED RECEIVER IMPLEMENTATIONS

Table I presents state-of-the-art NPF based receivers. As observed in this search most of the NPF solutions use direct conversion (DC), mainly with a direct connection to the input in a mixer first topology. [12, 13, 16, 17, 33] implement low-IF or super-heterodyne (SH) RX using high-Q variations from the traditional NPF.

State-of-the-art DT-RX is presented in Table II. The versatility of the strategy enables a variety of receiver architecture implementations, DC, SH, Low-IF, and phase tracking. Charge sampling concept is adopted in several works, with low-noise transconductor amplifiers (LNTA) followed by sampling mixers with only a few low noise amplifiers (LNA) followed by voltage sampling mixers.

V. CONCLUSION

This paper presented a review of discrete-time and N-path based receivers. Both strategies enable Software-Defined Radio solutions, reconfigurable receivers, as well as the implementation of radio Standards like BLE, Wi-Fi, cellular, etc. A detailed discussion on switched-capacitor building blocks typically adopted in discrete-time receivers was presented after an overview of N-path fundamental concepts. Similarities between DT-RX and N-Path based receivers are explored. While N-path filters present intrinsic mixer first topologies, discrete-time filters offer flexibility of use, variable selectivity, and higher wide-band blocker protection.

ACKNOWLEDGMENTS

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REFERENCES

### Table I. State-of-the-Art in N-Path Receivers

<table>
<thead>
<tr>
<th>Work</th>
<th>Architecture</th>
<th>Tech.</th>
<th>Freq. (GHz)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>IIP3 (dBm)</th>
<th>IIP2 (dBm)</th>
<th>Power (mW)</th>
</tr>
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<tbody>
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<td>[11]</td>
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<td>6.5</td>
<td>11</td>
<td>65</td>
<td>67</td>
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<td>Low-IF Diff LNA</td>
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<td>78.4</td>
<td>3.3</td>
<td>3.1</td>
<td>&gt;45</td>
<td>71.5</td>
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<td>JSSC'11 SH Input Npath + programmable BPF</td>
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<td>2.8</td>
<td>-8.4</td>
<td>-</td>
<td>25.2</td>
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<td>[70]</td>
<td>JSSC'13 DC Active Npath filter</td>
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<td>25</td>
<td>3</td>
<td>12</td>
<td>-</td>
<td>57.4</td>
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<td>[15]</td>
<td>ISSCC'18 DC Diff LNA + harmonic rejection Npath</td>
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<td>0.2-1</td>
<td>36</td>
<td>5.4-6</td>
<td>9*</td>
<td>-</td>
<td>26-32</td>
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<td>[72]</td>
<td>JSSC'11 Low-IF</td>
<td>28 nm</td>
<td>0.1-2</td>
<td>16</td>
<td>4.1-10.3</td>
<td>35*</td>
<td>90*</td>
<td>34-96</td>
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<td>5-8.6</td>
<td>25*</td>
<td>-</td>
<td>80-97</td>
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<td>4.3-7.6</td>
<td>33.3</td>
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<td>JSSC'20 DC Bottom-plate NPF-mixer</td>
<td>22FD-SOI</td>
<td>0.6-1.3</td>
<td>9-14</td>
<td>5.9</td>
<td>25</td>
<td>66*</td>
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<td>[74]</td>
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<td>-</td>
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<td>30</td>
<td>23-49</td>
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<td>IWS'23 Low-IF Mixer first Npath</td>
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<td>46</td>
<td>2.2</td>
<td>16*</td>
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<td>14-18*</td>
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<td>TCAS'23 DC LNA+Active NPF</td>
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<td>0.2-1/2.4</td>
<td>44.5-50.5</td>
<td>4.4-5.7</td>
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<td>58*</td>
<td>8.7</td>
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</table>

* Out-of-band IIP3 ** BiCMOS

### Table II. State-of-the-Art in Discrete-Time Receivers

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<thead>
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<td>[18]</td>
<td>JSSC'04 DC LNTA+DT-RX</td>
<td>130 nm</td>
<td>2.4</td>
<td>-</td>
<td>-15</td>
<td>-</td>
<td>-15</td>
<td>61.5</td>
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<tr>
<td>[21]</td>
<td>CICC'05 DC LNA+TA+DT-RX</td>
<td>90 nm</td>
<td>0.8/0.9/1.1/1.9</td>
<td>2</td>
<td>25</td>
<td>46</td>
<td>60</td>
<td></td>
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<tr>
<td>[22]</td>
<td>JSSC'06 SH Noise Cancelling LNA + DT-RX</td>
<td>90 nm</td>
<td>0.8-6</td>
<td>10-60</td>
<td>5-5.5</td>
<td>4</td>
<td>60</td>
<td>88.5</td>
</tr>
<tr>
<td>[67]</td>
<td>JSSC'10 DC LNA+DTRX</td>
<td>65 nm</td>
<td>0.2-0.9</td>
<td>-0.5-2.5</td>
<td>18-20</td>
<td>10*</td>
<td>53*</td>
<td>19.2</td>
</tr>
<tr>
<td>[36]</td>
<td>RFIC'13 DC Gm+mixer+DTRX+Npath</td>
<td>65 nm</td>
<td>0.5-1.2</td>
<td>35</td>
<td>6.7</td>
<td>10</td>
<td>-</td>
<td>24.5</td>
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<tr>
<td>[26]</td>
<td>JSSC'14 SH LNTA + DT-RX</td>
<td>65 nm</td>
<td>1.8-2.5</td>
<td>82</td>
<td>3.2-4.5</td>
<td>-7</td>
<td>45/85</td>
<td>55-65</td>
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<td>[31]</td>
<td>JET'14 DC LNA+DT-RX</td>
<td>180 nm</td>
<td>2.4</td>
<td>23</td>
<td>17.6</td>
<td>-15</td>
<td>-</td>
<td>25.6</td>
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<tr>
<td>[39]</td>
<td>TVLSI'17 SH LNTA + DT-RX</td>
<td>65 nm</td>
<td>0.5-3</td>
<td>35</td>
<td>&lt;-10</td>
<td>11*</td>
<td>46</td>
<td>250-600*</td>
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<tr>
<td>[28]</td>
<td>JSSC'14 SH LNTA+DT-RX w/HR</td>
<td>28 nm</td>
<td>0.5-2.5</td>
<td>35</td>
<td>2.1-2.6</td>
<td>14</td>
<td>&gt; 50</td>
<td>22-40</td>
</tr>
<tr>
<td>[20]</td>
<td>JSSC'17 SH LNTA+DT-RX</td>
<td>28 nm</td>
<td>2.4</td>
<td>46</td>
<td>6.5</td>
<td>-19</td>
<td>-</td>
<td>2.75</td>
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<td>[27]</td>
<td>JSSC'18 SH LNTA+DT-RX</td>
<td>65 nm</td>
<td>0.4-2.9</td>
<td>83</td>
<td>2.9-4</td>
<td>-5</td>
<td>93</td>
<td>48-79</td>
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<tr>
<td>[38]</td>
<td>JSSC'18 DC filtering by aliasing active FIR</td>
<td>65 nm</td>
<td>0.1-1</td>
<td>23</td>
<td>6.5-8.5</td>
<td>21*</td>
<td>64*</td>
<td>100</td>
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<tr>
<td>[34]</td>
<td>IMS'18 SH LNTA + DT-RX</td>
<td>28 nm</td>
<td>2.4</td>
<td>34</td>
<td>7.9</td>
<td>-13.6</td>
<td>-</td>
<td>1</td>
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<td>[37]</td>
<td>TCAS'18 SH LNTA + DT-RX</td>
<td>65 nm</td>
<td>1.8-2.2</td>
<td>55</td>
<td>2.8-5.3</td>
<td>-8.3</td>
<td>20</td>
<td>39</td>
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<td>[32]</td>
<td>JSSC'21 Phase tracking DT-RX</td>
<td>28 nm</td>
<td>2.4</td>
<td>55</td>
<td>6.3</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
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<td>[78]</td>
<td>JSSC'22 Filtering by Aliasing using FIR</td>
<td>28 nm</td>
<td>0.1-1</td>
<td>12</td>
<td>7.8-12</td>
<td>11.5</td>
<td>-</td>
<td>16-27.5</td>
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<td>[25]</td>
<td>JSSC'23 SH HR mixer first w/FIR + BB LNA</td>
<td>45 nm SOI</td>
<td>0.25-2.5</td>
<td>35</td>
<td>3.5-5.5</td>
<td>13-27*</td>
<td>-</td>
<td>32.4-54</td>
</tr>
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</table>

* Out-of-band IIP3 + includes synthesizer
REFERENCES


