Parameter extraction using the transfer characteristics of vertically stacked Si nanosheet MOSFETs

Adelmo Ortiz-Conde¹, Vanessa C. P. Silva²,³, Anabela Veloso⁴, Paula G. D. Agopian²,³, Eddy Simoen⁵, Joao A. Martino², Francisco J. García-Sánchez

¹Department of Electronics and Circuits, Universidade Simón Bolívar, Caracas 1080, Venezuela, ²LSI/PSI/USP, Universidade de São Paulo, SP 05508-010, Brazil, ³Department of Electronic and Telecom. Eng., Universidade Estadual Paulista, São João da Boa Vista 13876-750, Brazil ⁴imec, B-3001 Leuven, Belgium ⁵Department of Solid-State Physics, Universiteit Gent, 9000 Ghent, Belgium  
e-mail: ortizc@usb.ve

Abstract—We present a critical assessment and discussion of the presence of parasitic source-and-drain series resistance and normal electric field-dependent mobility degradation in undoped Si nanosheet MOSFETs. A simple explicit Lambert W function-based closed-form model, continuously valid from sub-threshold to strong conduction, was used to clearly describe the transfer characteristics. The model was applied to experimental vertically stacked GAA undoped Si nanosheet MOSFETs using phenomenon-related model parameter values extracted from measured data through suitable numerical optimization procedures. The conducted analysis reveals and explains how these two effects produce analogous deleterious consequences on these devices’ transfer characteristics.

Index Terms—Lambert W function, mobility degradation, parasitic series resistance, nanosheet FETs MOSFETs.

I. INTRODUCTION

The unrelenting evolution of increasingly complex 3D transistor structures, as well as the enormous progress of advanced IC fabrication technologies, such as those that have enabled the commercial manufacture of FinFETs, has inspired the emergence of other innovative Gate-All-Around (GAA) device structures, such as nanowire FETs and lately vertically stacked NanoSheet MOSFETs [1], [2] as a promising strategy to further IC component miniaturization [3].

The purpose of this article is to analyze and discuss the effect of parasitic source-and-drain series resistance and normal electric field-dependent mobility degradation on the transfer characteristics of undoped Si nanosheet MOSFETs. For that purpose, we use a core model that can conveniently serve as a way to concisely describe the drain current as a function of gate voltage in the linear region of operation (at small applied drain voltage). This is a semiempirical core model that consists of a simple closed-form explicit mathematical expression with only essential parameters, and is continuously valid from weak to strong conduction.

We avoid the otherwise frequently used terms “depletion,” “weak inversion” and “strong inversion,” so as to be consistent with the fact that we are dealing here with nominally undoped MOSFET channels, in reference to which the use of those terms would not be adequate [4].

The Lambert W function [5] is the foundation of the model that will be used here. The nowadays ubiquitous W is a multivalued special mathematical function implicitly defined as the inverse function of the linear-exponential transcendental equation $x = y \exp(y)$, which can be solved for $y = W_k(x)$ only when $x \geq -1/e$, where $k$ represents the branch number [6]. $W$ was originally formulated by Leonard Euler in 1783 [7], and revived by Edward M. Wright in 1959 [8] and later rescued for practical use in 1996 by Robert M. Corless and coworkers [5], [9]. The $W$ function’s name “Lambert” commemorates Johann Heinrich Lambert’s Transcendental Equation of 1758, and the use of the symbol “$W$” acknowledges the pioneering work of Wright on the subject.

Soon after its revival, $W$ was introduced in 2000 into the field of electronics for purposes of modeling, analysis and design. It was first proposed at that time for explicitly describing nonideal junctions with parasitic series and shunt resistive losses [10], diodes in series with a resistor [11], and for bipolar transistor applications [12]. Three years later in 2003, the $W$ function was again used in electronics for the first time for MOSFET modeling, originally for explicitly describing the channel surface potential of undoped channel MOSFETs [13].

The $W$ function continued to be used in a growing number of occasions and situations related to MOSFET modeling. Among the many instances $W$ has been used ever since for this purpose are: ultrathin body nanoscale devices [14], Double Gate [15], [16], [17] and Surrounding Gate devices [18], polySi thin film transistors (TFTs) [19], undoped and lightly-doped symmetric Double Gate devices [20], GAA undoped polySi nanowire devices [21], for FDSOI MOSFET parameter extraction [22], for charge and capacitance modeling in tunnel FETs [23], MOSFET modeling at deep cryogenic temperatures [24], in the Generalized EKV Compact MOSFET Model [25], to describe the charge density in Transition Metal Dichalcogenide FETs [26], and lately also for nanosheet transistors [27].

II. TRANSFER CHARACTERISTICS IN THE LINEAR REGION

According to original formulations [13], the mathematical description of the phenomenological behavior of carrier charges per unit area, $Q_s$, in an undoped MOSFET channel may be described by a $W$ functional form:

$Q_s = 2\nu_{th} C_{ox} W_0 \left[ \frac{1}{\nu_{th}} \exp \left( \frac{V_{gs}-V_{fb}}{2\nu_{th}} \right) \right].$  

(1)
where $V_{GS}$ is the applied gate-to-source voltage, $V_{FB}$ is the flat-band voltage, given by the difference between the gate conductor and the semiconductor body work functions, and including any possible interface trap and other oxide charges, $v_{th} = k_{B}T/q$ is the thermal voltage, $C_{ox}$ is the gate-oxide capacitance per unit area, $\gamma$ is the so-called body factor and $W_0$ stands for the principal branch ($k=0$) of the $W$ function. This principal branch is chosen because we are dealing only with real numbers and the $W$ function’s argument in this case remains $\geq 0$ for any bias conditions considered [6].

A. The core model neglecting both mobility degradation and parasitic source-and-drain series resistance

Our premise for formulating this core model is that in the absence of significant depletion charge in the undoped channel of the nanosheet MOSFET, the drain current is directly proportional to $Q_z$. We also redefine a part of the argument of $W_0$ in (1) by letting

$$
\frac{\gamma}{2z_v} \exp \left( \frac{-V_{FB}}{n \nu_{th}} \right) = \exp \left( \frac{-V_T}{n \nu_{th}} \right),
$$

(2)

where $V_T$ represents a threshold voltage and $n$ is an empirical quality factor. We then introduce a transconductance term:

$$
g_0 = 2v_{th} \mu C_{ox} \frac{Z}{L},
$$

(3)

where $\mu$ represents the carrier mobility, $L$ is the effective channel length and $Z$ is the effective channel width of the entire nanosheet device.

Then, based on the phenomenology of (1), and using (2) and (3), we propose the following semiempirical abridged explicit mathematical description of the drain current of stacked undoped Si nanosheets, which we assume to be equal (symmetric) and thereby valid from below threshold to strong conduction well above threshold. It is also a convenient tool for analysis because of its conciseness, since it contains only three essential parameters, $I_0$ (or $g_0$), $n$ and $V_T$, to describe the relationship between the three terminal variables $I_D$, $V_{GS}$ and $V_{DS}$. Additionally, the values of those three essential parameters can be easily extracted from the devices’ measured transfer characteristics, as we shall see.

Solving (4) by directly applying the definition of $W$, and using (5), immediately yields the inverse equation that describes the gate voltage as a function of the drain current:

$$
\exp \left( \frac{V_{GT}}{n \nu_{th}} \right) = \frac{I_D}{g_0 V_{DS}} \exp \left( \frac{I_D}{g_0 V_{DS}} \right),
$$

(6)

where, for brevity we have used

$$
V_{GT} = V_{GS} - V_T.
$$

(7)

Taking logarithms of both sides of the gate voltage equation (6), it may be rewritten in a more meaningful form:

$$
\frac{V_{GT}}{n \nu_{th}} = \ln \left( \frac{I_D}{g_0 V_{DS}} \right) + \frac{I_D}{g_0 V_{DS}}.
$$

(8)

Either (6) or (8) provide a quick vision of the functional relationship between gate voltage and drain current, since they contain only elementary functions. However, examination of (8) readily suggests that it represents two mechanisms that occur in series. One of them, where $V_{GT}$ increases logarithmically with drain current, is dominant below threshold for values of $V_{GT} \ll 0$, while the other one, where $V_{GT}$ increases linearly with drain current, dominates above threshold for values of $V_{GT} \gg 0$.

Notice that (8) turns out to be more numerically manageable than (4) for the purpose of being fitted to measured transfer characteristics, as needs to be done to extract the model’s essential parameter values [29], [30].

B. The model including only parasitic source-and-drain resistance

Let $V_{gs}$ and $V_{ds}$ be the intrinsic (internal) gate and drain -to-source voltages, respectively. Recalling (5) we may define $g_0 = I_0/V_{DS}$ and proceed to rewrite the core model gate voltage equation (8), but now in terms of intrinsic (internal) variables:

$$
\frac{V_{gs}-V_T}{n \nu_{th}} = \ln \left( \frac{I_D}{g_0 V_{DS}} \right) + \frac{I_D}{g_0 V_{DS}}.
$$

(9)

Consider now that there is no mobility degradation, but there exists significant presence of parasitic resistive losses in series with both the source and the drain regions of the nanosheets, which we assume to be equal (symmetric) and lump them together, jointly calling them “the source-and-drain resistance,” to be denoted by $R$. Then the intrinsic gate and drain voltages, $V_{gs}$ and $V_{ds}$, may be described in terms of the extrinsic (externally applied to the terminals) gate and drain voltages $V_{GS}$ and $V_{DS}$, respectively [28]:

$$
V_{gs} = V_{GS} - \frac{R}{2} I_D,
$$

(10)

$$
V_{ds} = V_{DS} - R I_D.
$$

(11)

Substituting (10) and (11) into (9) yields

$$
\frac{V_{GT}}{n \nu_{th}} = \ln \left[ \frac{I_D}{g_0 (V_{DS}-R I_D)} \right] + I_D \left( \frac{R/2}{n \nu_{th}} + \frac{1}{g_0 (V_{DS}-R I_D)} \right),
$$

(12)
which is an equation comparable to (9) but with the resistive losses of $R$ properly subtracted from $V_G$ and $V_D$.

Exponentiation of both sides of (12) yields

$$\exp\left(\frac{V_G - \theta R/2}{n V_{th}}\right) = \frac{I_D}{g_0(V_D - RI_D)} \exp\left(\frac{-\theta R/2}{g_0 V_{th}}\right).$$  \hspace{1cm} (13)

Applying the definition of the $W$ function to (13) generates an exact expression for the drain current in terms of the extrinsic variables $V_{GS}$ and $V_D$ that includes the effect of significant parasitic source-and-drain resistance $R$:

$$I_D = g_0 (V_{DS} - RI_D) W \left\{ \exp\left[\varphi_{GS} / n V_{th}\right]\right\}. \hspace{1cm} (14)$$

Letting $R=0$ in (14) reverts this model to the core model (4). Unfortunately, because of the presence of $I_D$ inside the argument of the exponential in (14), this expression is clearly not explicit, in contrast to the core model (4) which is. This circumstance constitutes a handicap for the speedy use of model equation (14) in circuit simulation applications. However, if we are willing to tolerate some level of approximation, we could disregard the term $I_D R/2$ within the argument of the exponential in (14), which makes only a marginal contribution whenever $R$ is so small that $I_D R/2 \ll V_{GS}$. The result of doing so is an approximate but explicit equation of the drain current as a function of gate voltage,

$$I_D \approx \frac{V_{DS}}{g_0 W \left\{ \exp(V_G / n V_{th})\right\}}. \hspace{1cm} (15)$$

This approximate model (15) could be used for circuit simulation, but always with some caution, because it is not exact, since it only includes the effect of source-and-drain resistance $R$ on the applied drain voltage $V_{DS}$, neglecting it on the applied gate voltage $V_{GS}$. Notice again that letting $R=0$ in (15) directly reverts it to the core model (4).

Although (14) and (12) are exact inverses of each other, (12) offers two important advantages for numerical calculation over (14). They are: a) (12) is explicit, whereas (14) is implicit; and b) (12) contains only elementary functions, whereas (14) contains the non-elementary special $W$ function. These two attributes make (12) particularly attractive for fitting it to the measured transfer characteristics, a numerical task needed to extract the four $(3+1)$ model parameters $g_0$, $n$, $V_I$ and $R$.

C. The model including only mobility degradation

Consider now that the source-and-drain parasitic resistance in the stacked nanosheets is so small that it may be neglected altogether. Instead, let us assume that the normal electric field (perpendicular to the carriers’ flow) created by the applied excess gate bias $V_{GT}$ produces a significant decrease, or degradation, of the mobility [31]. And let, for simplicity, also assume that this mobility degradation may be sufficiently well described by a simple first order model of the type:

$$\mu = \frac{\mu_0}{1 + \theta V_{GT}}. \hspace{1cm} (16)$$

where $\mu_0$ is the value of the low (normal) field mobility and $\theta$ is the first order mobility degradation factor, with units of $V^{-1}$. Since we are dealing here with the transfer characteristics only at low values of drain-to-source voltage, there is no need to account for mobility degradation because of carrier velocity dependence or saturation due to longitudinal channel electric field. Having introduced the mobility degradation definition (16) requires to clearly restate the definition of $g_0$ accordingly, which now becomes:

$$g_0 = 2 v_{th} \mu_0 C_{ox} \frac{Z}{L}. \hspace{1cm} (17)$$

Following a reasoning parallel to that of (9), which was based on the ideas of [21], and using (16) and (17), we propose to describe the gate-to-source voltage at low drain-to-source voltage, by the following semi-empiric phenomenological continuous expression:

$$\frac{V_{GT}}{n V_{th}} = \ln\left(\frac{I_D}{I_{low}}\right) + \frac{I_D}{I_{as}} (1 + \theta V_{GT}) \hspace{1cm} (18)$$

where $I_{low}$ and $I_{as}$ are two different current constants for weak and strong conduction. As was the case before in (9), there are two normalized gate voltage terms in the right-hand-side of (18) that work in series. The first term increases logarithmically with drain current, dominating below threshold for values of $V_{GT} \ll 0$. Thus, the drain current in this region behaves exponentially as

$$I_D \rightarrow I_{low} \exp\left(\frac{V_{GT}}{n V_{th}}\right) \text{ for } V_{GT} \ll 0. \hspace{1cm} (19)$$

The second mechanism is the increase of gate voltage with drain current, in principle linearly, but not quite so, because of the presence of mobility degradation. This mechanism dominates above threshold for values of $V_{GT} \gg 0$. Thus, the drain current in this region behaves as

$$I_D \rightarrow I_{as} \frac{V_{GT}}{(1 + \theta V_{GT}) n V_{th}} \text{ for } V_{GT} \gg 0. \hspace{1cm} (20)$$

Collecting in the left-hand-side of (18) the two terms that contain $V_{GT}$ and then solving for $V_{GS}$ yields:

$$V_{GS} = V_T + \frac{\ln(I_D/I_{low}) + 1}{n V_{th} / I_{as} - \theta}, \hspace{1cm} (21)$$

which is an equation that may be conveniently used to extract the five model parameters ($I_{low}$, $I_{as}$, $\theta$, $n$, $V_T$) by fitting it to the measured transfer characteristics.

Exponentiation and multiplication of both sides of (18) by $(1 + \theta V_{GT}) I_{low} / I_{as}$ yields:

$$\left(1 + \theta V_{GT}\right) I_{low} I_{as} e^{V_{GT} / n V_{th}} = I_D I_{as} (1 + \theta V_{GT}) e^{V_{GT} / (1 + \theta V_{GT})}. \hspace{1cm} (22)$$
Applying the definition of the $W$ function to (22) produces the analytic solution for $I_D$ as an explicit function of the excess gate voltage $V_{GT}$:

$$I_D = \frac{I_0 w_o (1 + \theta V_{GT}) \exp\left(\frac{V_{GT}}{n V_{th}}\right)}{1 + \theta V_{GT}}$$  \quad (23)$$

For the case of $I_{Dw} = I_{DS} = I_D$, the above equation becomes:

$$I_D = \frac{I_0 w_o (1 + \theta V_{GT}) \exp\left(\frac{V_{GT}}{n V_{th}}\right)}{1 + \theta V_{GT}}$$  \quad (24)$$

and equation (21) simplifies to:

$$V_{GS} = V_T + \frac{I_0 (I_D / I_0)^{-1}}{I_0 / I_0 \cdot \frac{1}{n V_{th} / \theta}}$$  \quad (25)$$

Equations (24) and (25) describe the drain current by an exponential behavior in weak conduction below threshold, and asymptotically approaching a sub-linear behavior in strong conduction above threshold because of mobility degradation. It is worth mentioning that a first attempt to include mobility degradation in such a Lambert $W$ function-based model dates back to 2013 (equation (1) of [30]).

D. Similarity between source-and-drain resistance and mobility degradation effects

We recall that (15) was an approximate explicit equation of the drain current as a function of excess gate voltage, that partially includes the effect of $R$, valid for small values of $R$, i.e., for $I_D / R / 2 \ll V_{DS}$. It may be rewritten as:

$$I_D \approx \frac{g_0 W \exp\left(\frac{V_{GS}-V_T}{n V_{th}}\right)}{1 + g_0 W \exp\left(\frac{V_{GS}-V_T}{n V_{th}}\right)} V_{DS}$$  \quad (26)$$

We may notice that the numerator of (26) is nothing other than the core model drain current expression (4). We make a further approximation at this point by assuming operation in the strong conduction region. Under that assumption of $V_{GS} - V_T \gg 0$, the argument of the $W$ function becomes very large. And since $W_0(x \to \infty) \rightarrow \ln(x)$ [5], we may replace $W_0$ in the denominator of (24) by the natural logarithm. Thus, the drain current equation including the effect of $R$ may be approximately written as

$$I_D \approx \frac{g_0 W \exp\left(\frac{V_{GS}-V_T}{n V_{th}}\right)}{1 + g_0 W \exp\left(\frac{V_{GS}-V_T}{n V_{th}}\right)} V_{DS}$$  \quad (27)$$

The denominator of equation (27) now reminds us of a first order mobility degradation effect analogous to (16). Accordingly, we may define an "equivalent mobility degradation factor" $\theta_{eq}$, such that (27) becomes

$$I_D \approx \frac{g_0 W \exp\left(\frac{V_{GS}-V_T}{n V_{th}}\right)}{1 + \theta_{eq} (V_{GS}-V_T)} V_{DS}$$  \quad (28)$$

where

$$\theta_{eq} = \frac{g_0 R}{n V_{th}}$$  \quad (29)$$

This equivalence between $R$ and $\theta$ confirms that the presence of source-and-drain resistance and of mobility degradation produce approximately similar effects on the strong conduction region of the transfer characteristics at low drain voltages.

III. EXPERIMENTAL VALIDATION

Data was measured from GAA vertically stacked undoped Si Nano Sheet n-MOSFETs. They have 22 parallel fins per device and each fin corresponds to two vertically stacked silicon nanosheets. They were fabricated at IMEC, Belgium, on 300 nm bulk silicon wafers, with a metal gate-stack composed of two layers of TiN and an Al-based effective work function (EWF) metal layer with a total thickness of 7.5nm, yielding an estimated metal Effective Work Function of EWF=4.35eV. The high-$k$ gate dielectric is composed of an SiO$_2$ interfacial layer (IL) covered by HfO$_2$ with an Equivalent Oxide Thickness of EOT=9.9nm. Each nanosheet has a width ($W_{fin}$) of about 15 nm and a height ($h_{fin}$) of about 11–11.5nm, with an effective channel width per fin of about ($W_{eff} = 2 \times 2 \times W_{fin} + 2 \times h_{fin}$) =104 nm, which considering the 22 fins give a total $W_{eff}$=2.288μm. In-situ highly doped Si epitaxy was used for the n-type source and drain regions, followed by a high temperature short time anneal for junction activation. Devices with two channel lengths of 28 and 70nm were used for this study. Figs. 1 A and B show TEM cross section images of the devices, and their schematic cross section, respectively. Additional details about these devices and their fabrication process can be found in [32] - [36]. Fig. 2 presents measured output characteristics for devices of both channel lengths.

![Fig. 1](image1.png) A) TEM cross section image. B) Schematic cross section of vertically stacked nanosheet MOSFET.

![Fig. 2](image2.png) Measured output characteristics of two stacked nanosheet devices with different channel lengths.
A. Parameter extraction

Transfer characteristics were measured at small drain voltages for devices of two channel lengths. They are presented in Fig. 3 for $L=28\text{nm}$ and in Fig. 4 for $L=70\text{nm}$. The parameter values of the two models, the one with only series resistance and the other with only mobility degradation, were extracted by lateral fitting [29] of (12) and (25), respectively, to the experimental data measured at five values of $V_{DS}$ from 20 to 100mV in 20mV increments. Data with $V_{GS}<0.1\text{V}$ were excluded from the fitting process to avoid the unwanted measured leakage current.

B. Parameter dependence on drain bias

Three of the extracted parameter values of either of the two models ($g_0$, $n$, $R$ or $g_0$, $n$, $\theta$) seem to be fairly independent of drain bias, but not the threshold voltage parameter $V_T$, which shows significant positive linear dependence on $V_{DS}$.

Such behavior may be simply modelled for small magnitudes of $V_{DS}$ by the following equation:

$$V_T = V_{T0} + \alpha V_{DS}, \quad (30)$$

where $V_{T0}$ represents the threshold voltage at $V_{DS} = 0$ and $\alpha$ is a dimensionless proportionality constant coefficient, which accounts for (a) “drain-induced-barrier-lowering” (DIBL) [37]-[39], (b) “drain-induced charge enhancement” (DICE) [40] and (c) the intrinsic triode region dependance. This last effect may be realized by analogy to the drain current of SOI MOSFETs in strong inversion and triode region [41], [42]:

$$I_D = K(V_{GS} - V_{TA} - \alpha \frac{V_{DS}}{2})V_{DS}, \quad (31)$$

where parameter $\alpha$ is the body factor [41],[42], whose value is typically close to 1, and $K$ represents the usual conductance parameter. The above equation may be rewritten as:

$$I_D = K(V_{GS} - V_{T0} - \alpha \frac{V_{DS}}{2})V_{DS}, \quad (32)$$

where

$$V_{TA} = V_{T0} + \alpha \frac{V_{DS}}{2} \quad (33)$$

is the apparent threshold voltage that will be obtained using standard extraction methods [30]. Therefore, if both DIBL and DICE were to be neglected, we would expect $\alpha = +\alpha/2$.

C. Parameter dependence on silicon thickness

Models that are based on the Lambert $W$ function have been recently labeled as “log-linear” models, in accordance with the kind of log-linear (or linear-exponential) transcendental equations $W$ is the solution of [43]. It has been suggested that such kinds of models may produce some inconsistent results related to the silicon thicknesses of double-gate (DG) type of MOSFETs [43]. In order to elucidate whether this may be also the case for the presently studied undoped Si GAA Nano Sheet n-MOSFETs, we conducted TCAD simulations of these GAA devices for two silicon thicknesses ($h_{ns}= 11$ and 20 nm). Figure 5 shows their simulated transfer characteristics, together with the corresponding model playbacks calculated using drain current equation (24). A drain voltage of 50 mV was assumed in the TCAD simulations, which are described in [35,36]. For easier numerical computation, the presently proposed model parameters were extracted by fitting the voltage equation (25) to the data (lateral fitting), instead of using (24). The resulting extracted values are: $V_{T0} = 0.218$ and 0.211V, $n=1.03$ and 1.04, $I_{D0}=11.7$ and 16.0 $\mu$A, and $\theta=1.88$ and 1.50V$^{-1}$, for thicknesses of $h_{ns}= 11$ and 20nm, respectively. The ratio of the two extracted $I_{D0}$ parameter values is consistent with that of the two nanosheet’s inner perimeter lengths. With these parameter values the present simple model seems to represent very well the TCAD simulated transfer characteristics of these GAA nanosheet single devices for both silicon thicknesses, as Fig. 5 indicates.
IV. DISCUSSION

Figs. 3 and 4 also show, drawn on top of the measured data symbols, both transfer characteristics model playbacks, simulated using the extracted parameters. Either model’s playbacks reproduce equally well the measured transfer characteristics. This represents clear evidence that series resistance and mobility degradation produce similar effects on the transfer characteristics for small drain bias, similarly to what was reported at strong conduction conditions [28], [31].

The five (3+2) parameter values for both models extracted by fitting (12) and (25), are shown in Tables I and II. The extracted parameter values allow a rough numerical appraisal of the adequacy of our original semiempirical formulation defined by (2), which we rewrite now as:

\[ V_{FB} = V_T + n \cdot V_{th} \cdot \ln \left( \frac{\gamma}{2 \cdot e^{\theta/V_{th}}} \right) \],

where the factor \( \gamma \) is given by [13]:

\[ \gamma = \sqrt{\frac{\alpha \cdot \varepsilon_{Si} \cdot n_i}{\varepsilon_{SiO2} / EOT}} \].

For example, if we assume \( T=300K \left( V_T = 25.87 \text{mV} \right) \), and use the standard values for \( n_i, \varepsilon_{Si} \), and \( \varepsilon_{SiO2} \), plus the value of the equivalent oxide thickness EOT=0.9nm and the extracted values of the empiric ideality factor \( n=1.280 \) and of the threshold voltage \( V_T\approx0.229V \) corresponding to the model of the 28nm long device that considers only series resistance, we can calculate the device’s flat-band voltage using (34), which results to be \( V_{FB} \approx 0.229-0.482 = -0.253V \).

Now, considering that the flat-band voltage in the absence of interface and oxide traps is defined as:

\[ V_{FB} = EWF_{net} - WF_{Si} = EWF_{net} - \left( \chi_{Si} + \frac{\varepsilon_{Si}}{2} \right) \],

and assuming that the electron affinity of the crystalline silicon surface to be \( \chi_{Si} =4.05 \text{eV} \), then the work-function of intrinsic silicon nominally would be \( WF_{Si} = 4.05+0.55 =4.6 \text{eV} \). Now using (35) we can calculate the approximate value of the effective work-function of the gate composite as \( EWF_{net} \approx 4.346 \text{eV} \), which in this case matches well with the otherwise previously estimated value of \( 4.35 \text{eV} \).

Notice that if \( V_{FB}=0 \), as it would be the case if the device’s gate instead were a so-called “mid-gap” metal, i.e. one with a work-function equal to that of intrinsic silicon, according to (34) the threshold voltage would be \( V_T \approx 0.482 \text{V} \), as roughly expected.

Considering the extracted values of \( n \) shown in Tables I and II, the corresponding Subthreshold Swings of the 28 and 70nm long devices are SS\approx77 and 60mV/decade, respectively, which is a sign of short channel effects (SCEs) [39].

A last comment concerning the use of the Lambert \( W \) function to describe MOSFET phenomena: Recently Robert Corless reminded us that the Lambert \( W \) function “is implicitly elementary” and that it should be viewed more as an answer rather than as a question, much in the same way the natural logarithm is the answer to the question of what is the inverse of the exponential function [44]. Furthermore, \( W \) has become nowadays a standard mathematical function implemented in all major technical computing systems. Values of the real branches of \( W \) can be readily computed because of the availability of efficient numerical algorithms [45] as well as numerous approximate analytical expressions [46]. Therefore, the use of the Lambert \( W \) function today in compact modeling is not any more of a burden than using elementary functions such as the logarithm or the exponential.

V. CONCLUSION

We have analyzed and discussed the effect of mobility degradation and parasitic source-and-drain series resistance on the transfer characteristics of vertically stacked GAA undoped Si nanosheet MOSFETs. A simple model based on the Lambert \( W \) function was used to typify the phenomenology of the transfer characteristics of these undoped nanoscale
devices continuously from sub-threshold to strong conduction. The model was applied to experimental devices with channel lengths of 28 and 70nm. Model parameter values were extracted by lateral fitting of the model’s equations to the actual experimental transfer characteristics measured at small values of drain-to-source voltage. Analysis of results indicates that mobility degradation and parasitic source-and-drain series resistance produce analogous consequences on the transfer characteristics of vertically stacked GAA undoped Si nanosheet MOSFETs.

### REFERENCES


