Abstract—Statistical techniques are regularly used to predict the performance of electronic systems. Process variations which account for the uncertainties in material parameters at the time of fabrication adversely affect the yield of analog integrated circuits. The statistical analysis of variations in key output parameters of an analog circuit due to variations in the fabrication parameters for yield prediction is an essential step in analog chip fabrication. In this work, we use a rigorous statistical approach to examine the performance of a typical analog circuit. We have designed a two stage CMOS differential amplifier configuration at 65 nm technology using ACM model parameters to examine the yield under process variations. We employ three different Monte Carlo models (uniform, gaussian, worst-case) to examine the statistical variation in key performance parameters of the designed CMOS differential amplifier. Variations in key differential amplifier parameters, maximum gain, gain margin and phase margin have been reported under 10% variations in typical process parameters. Maximum variability is observed in case of the worst-case distribution while the minimum variability is found in case of Gaussian distribution. The results show significant impact of process variation on the yield of the designed CMOS differential amplifier. In the case of gaussian distribution, the standard deviation for gain margin(dB), phase margin (degrees) and maximum gain(dB) is found to be 11, 25 and 24 respectively.

Index Terms—Monte Carlo Analysis, Differential Amplifier, Process Variations, CMOS, ACM model

I. INTRODUCTION

Analog electronic circuits are essential part of the current mixed signal VLSI technology. Various analog ICs that function as comparators, ADC/DACs, differential amplifiers, op-amps, oscillators, phase locked loops, filters, frequency dividers, charge pumps etc. are being rapidly miniaturized and improved in terms of their key performance parameters [1]–[5]. CMOS differential amplifier circuit is considered as an indispensable part of all modern signal processing, instrumentation, and measurement circuits. Accuracy and efficiency of differential amplifier plays a crucial role in many specific applications like biomedical signal processing circuits which deals with weaker signals. All amplifying circuits use different active elements which perform the signal amplification process. Bulk MOSFET is one of the most used active components along with the complementary logic technique to realize CMOS differential amplifiers due its high energy efficiency, high integration density, compatibility with other technologies, better performance and robustness [6]–[8]. Conventional design of CMOS differential amplifier consists of dual input which amplifies the differential voltage applied between the input terminals and produces a very high gain balanced output. Fig.1 shows a standard CMOS differential amplifier configuration [9].

Fig. 1 A standard single stage CMOS differential amplifier

Among the various techniques, DC tail current source is used generally for biasing the differential amplifier to achieve constant tail current [10]. Such a design also provides high input resistance, a good bandwidth range and high CMRR. High CMRR and high input resistance make this circuit a very important part of any analog integrated circuit. CMOS differential-amplifier with current mirror load has been designed using new automated design methodology at 180 nm technology [11]. Various design techniques based on bipolar transistor, bulk-driven MOSFET, floating gate etc. have been proposed for application of low voltage and low power implementation [12]–[14]. Approaches such as tunicate swarm algorithm and seeker optimization algorithm have been recently used for optimal transistor sizing of amplifiers circuits [15], [16]. In the following sections, we discuss about the impact of process variations and Monte Carlo analysis in a two stage CMOS differential amplifier which has been design using ACM (Advanced Compact MOSFET) model. In section III, the design and simulation approach is presented followed by the results and discussions section and finally the conclusion section.

II. PROCESS VARIATION AND MONTE CARLO ANALYSIS

Due to continuous downscaling in the MOSFET structures, several reliability issues have crept in, making the study of analog circuits more complex and all-consuming. Reliability can be classified into two key types, static or
dynamic [17], [18]. Static reliability is independent of time and becomes worse if we move from higher to lower geometric dimensions. The process of lithography becomes more complex at lower technology nodes. Reliability of analog circuits is affected by variation in process parameters like the threshold voltage, thickness of oxide, doping concentration etc. PVT (process, voltage, temperature) variations are inevitable in chips fabrication due to rapid VLSI scaling. Due to this rapid scaling, chip parameter precision is difficult to achieve [19], [20]. Inter-die and intra-die process variations vary widely and play a key role in ultra-low power VLSI circuit designs [21]. A number of approaches including machine learning techniques have been followed for yield estimation through simulations for analog circuit design [22]–[25]. Process variations which are a major issue in CMOS circuits, can be accurately examined using Monte-Carlo simulations [26], [27]. Monte-Carlo analysis is used to find out the effect of process variation in MOSFET parameters on circuit performance. Process variation in CMOS analog devices have been examined in a number of studies [28], [29]. Statistical models can tackle the issue of process variations in a more accurate manner [30]. The most important factors affecting VLSI chips are process variations and leakage which must be addressed for higher yield [31]. A gain of 60 dB at low frequency is obtained from a novel voltage amplifier [32]. This amplifier circuit is reported to show low variability in response with PVT variations.

To start with, we examine the key MOSFET parameters at 65 nm technology node required for the design of CMOS differential amplifiers. We consider two standard CMOS differential amplifier configurations and design the circuit using ACM model parameters [33], [34]. ACM model parameters used in the design and simulation are being listed below in Table I [35]. The two stage CMOS differential amplifier circuit designed at 65 nm technology node is then examined for the variability in the circuit parameters. Further, Table I shows the ACM model and device parameter values used in the design of the CMOS differential amplifier.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_0) (normalized current) (μA)</td>
<td>0.936</td>
<td>0.237</td>
</tr>
<tr>
<td>(C_{ox}) (oxide capacitance) (F/m²)</td>
<td>1.9×10⁻¹²</td>
<td>1.8×10⁻¹²</td>
</tr>
<tr>
<td>(V_T) (threshold voltage) (V)</td>
<td>0.313</td>
<td>0.2944</td>
</tr>
<tr>
<td>(\mu_c) (mobility) (m²/V-s)</td>
<td>0.37</td>
<td>0.006</td>
</tr>
</tbody>
</table>

III. DESIGN AND SIMULATION

Generally, amplifiers consist of multiple stages which are connected in a cascade form to provide sufficient gain. In this paper, we have designed and analysed typical single and two stage CMOS amplifiers at 65 nm technology. Fig. 2 shows a typical two stage CMOS differential amplifier. First stage of the amplifier is an input stage which consists of a differential configuration. First stage is responsible for providing a high input impedance and high CMRR. Second stage is used to improve the gain of the amplifier. It consists of a common source MOSFET \(M_2\) and \(M_5\) as a current source load. The role of capacitor \(C_C\) is to provide frequency compensation for the differential amplifier by providing negative feedback path. There is a capacitor at load which contributes as a pole in the transfer function. This pole provides -20 dB/decade slope leading to the possibility that the circuit becomes unstable, and oscillations start. To prevent oscillations or to make the system stable, it is preferable to provide negative feedback. A reference current for the differential amplifier is provided by the current mirror circuit. Current mirror structure is used to provide a constant current biasing to the analog circuits. Current mirror structure makes the output current stable and independent of other parameters. As per the 65 nm process technology the VDD was set to 1.2 V in the considered design.

Various models have been used for the design of MOS analog circuits including the surface-potential-based MOSFET models [36]–[39] and inversion charge-based models [40], [41]. For smaller channel length MOSFETs, conventional methods are not sufficient enough for efficient extraction of the key parameters due to effects such as short-channel effects and channel length modulation [42], [43].

![Fig. 2 A typical two stage CMOS differential amplifier](image)

It has been found that parameters extracted for MOSFET using conventional method for some desired operations are dissimilar with the circuit parameters extracted at the time of simulation [44], [45]. Calculations using ACM models are found to be very successful in calculation of design parameters for a typical standard CMOS differential amplifier as they are not specific to the region of operation [35], [46]. ACM model parameters have been derived and used to design a folded-cascade operational amplifier [47]. For smaller channel length MOSFET, by including modified equations of current, a more accurate model has been presented and thus the ACM model provides more accurate values of parameters. In this paper we have used this advanced compact MOSFET (ACM) model to calculate design parameters where \(I_F\) represent the inversion level and can be calculated by taking ratio of \(I_D\) (drain current) and \(I_0\) (normalized current). The value of \(I_F\) depends on the nature of inversion. For medium inversion we can take a value of \(I_F\) between 1 and 100.

ACM model which is a charge-based physical model and based on the gradual-channel approximation (GCA) and the charge-sheet approximation (CSA) provides a comprehensive characterization of a MOSFET device using only small set of parameters [48]. The structural source-drain symmetry is maintained with all the parameters such as the carrier mobility, junction depth, gate oxide thickness having relevant physical significance. The ACM model involves the calculation of surface potential \(\phi_{sa}\) at inversion.
charge density = 0, Slope factor (n), Pinch-off voltage $V_p$ and the inversion charge density $Q'$ leading to surface potential, drain current, total charge and ac parameters of the MOSFET [49].

In Fig. 2, two stages of the CMOS differential amplifier are connected in a cascaded manner. So, the total gain is the multiplication of gain of the individual stages. To determine the relation of frequency response and gain we can consider a small signal model of the CMOS amplifier for the calculation of design parameters. The value of $C_L$ for the current design has been taken as 25 pF. The gain of the amplifier is given as $A_v = A_{v1} \times A_{v2} = [gm_{1,4} \times (ro_4)|ro_3)] \times [gm_2 \times (ro_6)|ro_5])$. The transfer function of gain consists of two poles and one zero as per the equations given below.

$$P_1 = \frac{1}{[(ro_4)|ro_3)] \times [gm_2 \times (ro_6)|ro_5]) (1)$$

$$P_2 = gm_2/C_L (2)$$

$$Z_0 = gm_2/C_C (3)$$

$P_1$ is the dominant pole. So, by adjusting value of $C_C$ we can adjust gain crossover frequency, $GM$ and $PM$ of the amplifier. It will provide -20 dB/decade slope to the gain. Location of zero should be larger than second pole otherwise phase margin will be lesser.

$C_C = 0.04 \times C_L (4)$

We determine the W/L size of MOSFETs ($\theta_t = 26mV$) using the equations given below.

$$\frac{W/L_{1,4}}{W/L_{1,4}} = \frac{\theta_m}{\mu \times Cox \times \theta_t \times ((1+1f)^{0.5} - 1) (5)}$$

$$\frac{W/L_{2,3}}{W/L_{2,3}} = \frac{\theta_m}{\mu \times Cox \times \theta_t \times ((1+1f)^{0.5} - 1) (6)}$$

$$\frac{W/L_{5,6}}{W/L_{5,6}} = \frac{\theta_m}{\mu \times Cox \times \theta_t \times ((1+1f)^{0.5} - 1) (7)}$$

$$\frac{W/L_B}{W/L_B} = \frac{I(M8)}{I(M5)} (8)$$

$$\frac{W/L_G}{W/L_G} = \frac{\theta_m}{\mu \times Cox \times \theta_t \times ((1+1f)^{0.5} - 1) (9)}$$

Table II shows the calculated W/L ratios and the selected inversion level of the MOSFETs in the designed two stage CMOS differential amplifier at 65 nm technology.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W (µm)</th>
<th>W/L (L=130 nm)</th>
<th>if</th>
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<tbody>
<tr>
<td>M2=M3</td>
<td>2.022</td>
<td>15.56</td>
<td>2</td>
</tr>
<tr>
<td>M1=M4</td>
<td>0.308</td>
<td>2.371</td>
<td>2</td>
</tr>
<tr>
<td>M5=M6</td>
<td>0.155</td>
<td>1.197</td>
<td>5</td>
</tr>
<tr>
<td>M7</td>
<td>88.53</td>
<td>68.00</td>
<td>2</td>
</tr>
<tr>
<td>M8</td>
<td>3.361</td>
<td>25.855</td>
<td>5</td>
</tr>
</tbody>
</table>

IV. RESULTS AND DISCUSSIONS

In this section, the AC analysis of the CMOS differential circuits (single stage and two stage), AC analysis - Monte Carlo simulation with 1000 cases, Monte Carlo histogram of phase margin, gain margin and maximum gain (two stage) have been presented and discussed.

A. AC Analysis

Fig. 3 shows the AC analysis of the CMOS differential amplifier circuits where the gain (dB) and the phase (degrees) has been plotted against the frequency (Hz). In case of the single stage CMOS differential amplifier low frequency peak gain is observed to be 30.7 dB while for the two stage CMOS differential amplifier low frequency peak gain is 62.8 dB. A high gain band width product (GBW) of 3 MHz and phase margin of 62° as per the design specifications is obtained in the case of two stage CMOS differential amplifier. Table III shows the comparison of key parameters with the existing designs in literature for CMOS differential amplifier with various design specifications. The purpose of this comparison table is to showcase the different parameters that are typically considered when designing a differential amplifier and are essential in ensuring that the amplifier functions effectively and meets the required performance standards.
Table III. Comparison of key amplifier parameters with the existing designs in the literature.

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Differential gain (dB)</td>
<td>30.7</td>
<td>62.8</td>
<td>55.9</td>
<td>63 (70)</td>
<td>68</td>
<td>55.2</td>
</tr>
<tr>
<td>Common mode gain (dB)</td>
<td>-40</td>
<td>-7.9</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>70.7</td>
<td>70.8</td>
<td>63</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Slew Rate (V/µs)</td>
<td>0.153</td>
<td>3.0</td>
<td>656</td>
<td>10</td>
<td>0.484</td>
<td>158.2</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>91</td>
<td>62</td>
<td>61</td>
<td>75</td>
<td>68</td>
<td>84.1</td>
</tr>
<tr>
<td>Gain Margin (dB)</td>
<td>37.81</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1.2</td>
<td>1.2</td>
<td>1.0</td>
<td>1.0</td>
<td>3.3</td>
<td>1.2</td>
</tr>
<tr>
<td>Node (nm)</td>
<td>65</td>
<td>65</td>
<td>45</td>
<td>350</td>
<td>350</td>
<td>65</td>
</tr>
</tbody>
</table>

B. Monte Carlo Analysis

Process variability in CMOS circuits is implemented through Monte Carlo analysis which uses the nominal and extreme device parameter variations systematically. These parameter variations can be represented through worst-case, uniform or Gaussian distribution [54]. In case of uniform distribution, the process parameters are equally placed across the tolerance range (mean-tolerance) to (mean + tolerance). Process parameters change smoothly around the mean value in case of Gaussian distribution while in case of the worst-case distribution all the parameters are the extreme of the tolerance ranges (mean-tolerance), (mean+ tolerance). The device parameters are pushed to their extreme limits to observe their impact on the output, in case of worst-case analysis and is of great aid before the manufacturing has started [55]. A two-level Monte Carlo methodology which uses six BSIM model parameters has been presented for yield prediction [56]. As discussed earlier in section III, the ACM model is used for the design parameters of CMOS differential amplifier while the BSIM4 model is used for modelling the MOSFETs which is a widely used and well-established model for simulating MOSFET devices.

The key BSIM4 parameters responsible for process variation such as the length variation (xl), gate oxide thickness (tox) and channel doping concentration (ndep) have been listed by Hao Cai et al. [57]. Various MOS parameters such as channel length and gate oxide thickness with a variation of 10% are assumed to be key parameters for PVT studies of bulk CMOS at 32 nm node [58]. In the present work five process parameters namely, toxp (physical gate equivalent oxide thickness), xl (channel length offset due to mask/etch effect), xj (S/D junction depth), ngate (poly Si gate doping concentration) and ndep (channel doping concentration) as given in Level 54 BSIM 4.0 model from Predictive technology model (PTM) [59] varied by 10% have been used to perform the Monte Carlo analysis using the Micro-Cap 12 from Spectrum Software which is a SPICE compatible circuit simulator [60].

The statistical representation of the performance parameters aids in making decisions on the cost, manufacturability, and reliability of the designed circuit. Fig. 4 shows the AC analysis of the CMOS differential circuit - Monte Carlo simulation with 1000 cases. Three different distributions (a) uniform distribution, (b) Gaussian distribution (c) worst case show unique variations in the AC analysis. Monte Carlo simulation generates a batch of circuits with variable component tolerances based on the selected distribution. After each run of a circuit, the performance parameters are extracted and stored. As observed for Fig 4., the effect of process variation in the gain plot is higher at lower frequencies and begins to subside at higher frequencies. The effect of process variation in the phase plot is lower at lower frequencies. This variation of frequencies reduces at around the frequency 500 kHz and then increases again.

As observed from Fig. 5, The maximum gain in the range 60-72 dB is observed in 5.6 % cases of the Gaussian distribution. Worst-case gives the maximum gain in this
range for only 3% of the cases. In case of the Gaussian distribution the maximum number of cases (30.2%) lie in the range 12-24 dB. For uniform and worst-case distribution, the maximum number of cases lie in the range 0-12 dB (24.7%) and -12-0 dB (19.7%) respectively.

(a) Uniform distribution

(b) Gaussian distribution

(c) Worst case

As observed from Fig. 6, the maximum gain margin in the range 64-68 dB is observed in 0.8% cases of the worst-case and uniform distribution. Gaussian distribution gives the gain margin in the range 60-64 dB for only 0.1% of the cases. In case of the Gaussian distribution the maximum number of cases, 54.7% lie in the range 32-36 dB. In case of the uniform and worst-case distributions, the maximum number of cases, 51.5% and 38.5% also lie in the range 32-36 dB.

As observed from Fig. 7, The maximum phase margin in the range 168-180 degrees is observed in 1.1% cases of the Worst-case and 0.7% cases of the uniform distribution. Gaussian distribution gives the gain margin in this range for only 0.2% of the cases. In case of the Gaussian distribution the maximum number of cases, 31% lie in the range 84-96 dB. In case of the uniform and worst-case distributions, the maximum number of cases, 24% and 24.9% also lie in the range 84-96 dB.
Table IV shows the variability in circuit parameters for uniform, Gaussian, and worst-case distributions. Maximum variability is observed in case of the worst-case distribution where standard deviation (σ) for gain margin, phase margin and maximum gain is found to be 11, 25 and 24 respectively, while the minimum variability is found in case of Gaussian distribution where the standard deviation for gain margin (dB), phase margin (degrees) and maximum gain (dB) is found to be 11, 25 and 24 respectively. The mean values of the parameters are relatively consistent across all the three models. The standard deviation, although is highest in the worst-case scenario model, but is comparable to the uniform and Gaussian models suggesting that the current design of the CMOS differential amplifiers through ACM model is robust and capable of delivering consistent performance in the face of process variations.

V. CONCLUSION

Statistical techniques are regularly used to examine the performance of a system. In this work, we use a rigorous statistical approach to examine the performance of a typical analog circuit. A two-stage typical CMOS differential amplifier has been designed using ACM model parameters to examine the variability in the performance parameters due to variations in the process parameters. Process variability in CMOS circuits is implemented through Monte Carlo analysis which uses the nominal and extreme device parameter variations systematically. These parameter variations have been examined through worst-case, uniform or Gaussian distributions. Variations in maximum gain (dB), gain margin (dB) and phase margin (degrees) have been reported under typical process parameter variations of the BSIM4 model. Maximum variability is observed in case of the Worst-case distribution while the minimum variability is found in case of Gaussian distribution. A good yield prediction is possible even with an extreme variation in the process parameters at 65 nm technology node. The statistical representation of the performance parameters in this work will aid in making an initial decision on the cost, manufacturability, and reliability of the designed circuit.

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REFERENCES


